WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

an active pattern including:

a lower pattern extending in a first direction; and

a plurality of sheet patterns spaced apart from the lower pattern in a second direction perpendicular to the first direction, wherein the lower pattern comprises a semiconductor material;

a plurality of gate structures on the lower pattern and spaced apart from each other in the first direction, wherein each of the plurality of gate structures includes a gate electrode and a gate insulating film;

a source/drain recess between adjacent ones of the gate structures, wherein a bottom of the source/drain recess is in the lower pattern;

a bottom insulating liner in the bottom of the source/drain recess; and

a source/drain pattern in the source/drain recess and on top of the bottom insulating liner,

wherein a vertical distance between a topmost portion of the bottom insulating liner and a bottommost portion of the bottom of the source/drain recess is equal to or smaller than a vertical distance between an upper surface of the lower pattern and the bottommost portion of the bottom of the source/drain recess,

wherein the gate structures include a first inner gate structure between the lower pattern and a bottommost one of the sheet patterns, and a second inner gate structure between adjacent ones of the sheet patterns,

wherein the first and second inner gate structures each include the gate electrode and the gate insulating film, and

wherein the source/drain pattern is in contact with the gate insulating film of the first and second inner gate structures.

2. The semiconductor device of claim 1, wherein a thickness of the bottom insulating liner increases and then decreases as a distance between the bottom insulating liner and a first gate structure of the gate structures increases in the first direction.

3. The semiconductor device of claim 1 or claim 2, wherein an upper surface of the bottom insulating liner has a concave shape and is in contact with a bottom surface of the source/drain pattern.

4. The semiconductor device of any one of claims 1 to 3, wherein the bottom insulating liner is not overlapped by any of the sheet patterns in the second direction.

5. The semiconductor device of any one of claims 1 to 4,

wherein the bottom insulating liner includes a first sub-bottom insulating liner and a second sub-bottom insulating liner, and

wherein the first sub-bottom insulating liner is between the second sub-bottom insulating liner and the lower pattern.

6. The semiconductor device of any one of claims 1 to 5, wherein the bottom insulating liner is in contact with an entirety of a recessed surface of the lower pattern.

7. The semiconductor device of any one of claims 1 to 6,

wherein the gate insulating film includes a gate interfacial insulating film and a gate high dielectric constant insulating film on the upper surface of the lower pattern,

wherein the gate interfacial insulating film is between the gate high dielectric constant insulating film and the source/drain pattern, and

wherein a thickness of the gate interfacial insulating film is smaller than a thickness of the gate high dielectric constant insulating film.

8. A semiconductor device comprising:

an active pattern including:

a lower pattern extending in a first direction; and

a plurality of sheet patterns spaced apart from the lower pattern in a second direction perpendicular to the first direction;

a plurality of gate structures on the lower pattern and spaced apart from each other in the first direction, wherein each of the plurality of gate structures includes a gate electrode and a gate insulating film;

a source/drain recess between adjacent ones of the gate structures, wherein a bottom of the source/drain recess is in the lower pattern;

a bottom insulating liner in the bottom of the source/drain recess; and

a source/drain pattern in the source/drain recess and on top of the bottom insulating liner,

wherein a vertical distance between a topmost portion of the bottom insulating liner and a bottommost portion of the bottom of the source/drain recess is equal to or smaller than a vertical distance between an upper surface of the lower pattern and the bottommost portion of the bottom of the source/drain recess,

wherein the bottom insulating liner is not overlapped by any of the sheet patterns in the second direction,

wherein each of the gate structures includes a first inner gate structure between the lower pattern and a bottommost one of the sheet patterns, and a second inner gate structure between adjacent ones of the sheet patterns,

wherein the first and second inner gate structures each include the gate electrode and the gate insulating film, and

wherein the source/drain pattern is in contact with the gate insulating film of the first and second inner gate structures.

9. The semiconductor device of claim 8, wherein a thickness of the bottom insulating liner increases and then decreases as a distance between the bottom insulating liner and a first gate structure of the gate structures increases in the first direction.

10. The semiconductor device of claim 8 or claim 9, wherein an upper surface of the bottom insulating liner has a concave shape.

11. A semiconductor device comprising:

a first active pattern including:

a first lower pattern extending in a first direction; and

a plurality of first sheet patterns spaced apart from the first lower pattern in a second direction perpendicular to the first direction;

a second active pattern including:

a second lower pattern extending in the first direction; and

a plurality of second sheet patterns spaced apart from the second lower pattern in the second direction;

a plurality of first gate structures on the first lower pattern and spaced apart from each other in the first direction, wherein each of a plurality of the first gate structures includes a first gate electrode and a first gate insulating film;

a plurality of second gate structures on the second lower pattern and spaced apart from each other in the first direction, wherein each of a plurality of the second gate structures includes a second gate electrode and a second gate insulating film;

a first source/drain recess between adjacent ones of the first gate structures, wherein a bottom of the first source/drain recess is in the first lower pattern;

a second source/drain recess between adjacent ones of the second gate structures, wherein a bottom of the second source/drain recess is in the second lower pattern;

a bottom insulating liner in the bottom of the first source/drain recess;

a first source/drain pattern comprising n-type impurities and in the first source/drain recess; and

a second source/drain pattern comprising p-type impurities and in the second source/drain recess, wherein the second source/drain pattern is in contact with the second lower pattern,

wherein a vertical distance between a topmost portion of the bottom insulating liner and a bottommost portion of the bottom of the first source/drain recess is equal to or smaller than a vertical distance between an upper surface of the first lower pattern and the bottommost portion of the bottom of the first source/drain recess,

wherein the first gate structures include a first inner gate structure between the first lower pattern and a bottommost one of the first sheet patterns, and a second inner gate structure between adjacent ones of the first sheet patterns,

wherein each of the first and second inner gate structures includes the first gate electrode and the first gate insulating film,

wherein the first source/drain pattern is in contact with the first gate insulating film of the first and second inner gate structures.