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PATENT SPECIFICATION

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(54) IMPROVEMENTS IN OR RELATING TO ELECTRONIC TIMEPIECES

(71) We, KABUSHIKI KAISHA DAINI SEIKOSHA, a Japanese company, of 31-1, 6-chome, Kameido, Koto-ku, Tokyo, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement:—

This invention relates to electronic timepieces and has for its main object to provide improved electronic timepieces operable at will to display ordinary time (i.e. time of day) or chronograph time digitally.

Many electronic timepieces as at present in common use and providing a digital display of time produce a time display in accordance with the 12-hour clock system i.e. they display time digitally up to 12 hours. This is often regarded as convenient to users and it is in fact quite convenient for most ordinary usage, but it has the disadvantage that the display does not distinguish between A.M. and P.M. This can be a nuisance in some circumstances, for example when a watch is used to check the time for the purpose of complying with a time given in a railway or other transport timetable since such timetables commonly list times by the 24-hour clock.

Many electronic timepieces at present in common use and which can be used at will digitally to display time of day in the ordinary way or to display chronograph (stop watch) elapsed time, are arranged to give a chronograph or stop watch display going up to only 12 hours. This is a serious limitation on utility since the maximum stop watch time which can be displayed is only 12 hours whereas a chronograph which could display chronograph time up to 24 hours would be considerably more useful.

As will be seen later, the invention provides improved timepieces utilisable at will as ordinary timekeepers or as chronographs, giving a chronograph display going up to 24 hours and (preferably) a display of

ordinary time also going up to 24 hours (since this has the advantage of distinguishing between A.M. and P.M.) but, if preferred, the timepiece can be constructed to give this display up to 12 hours only. As will be seen later the same digital display device is used both for time of day and chronograph time display and, in consequence, a larger and clearer display can be obtained than if separate display devices were used for displaying time of day and chronograph time — an important matter in the case of a wrist watch where the space available to accommodate display devices is so limited.

According to this invention there is provided an electronic timepiece operable at will to display either time of day or chronograph time digitally comprising a relatively high frequency time standard oscillator including a frequency determining vibrator; a multi-stage frequency divider connected to divide down the frequency of the output from said oscillator to a lower time standard frequency; two counting systems each including a seconds counter, a minutes counter and an hours counter, at least one of said systems including an hours counter counting up to 24 hours; manually operable chronograph control circuit means for feeding said lower time standard frequency to said one system and simultaneously resetting the counters therein, starting counting thereby and subsequently stopping counting thereby; a plurality of selecting gate circuits for selecting the seconds, minutes and hours counts in said one system or the seconds, minutes and hours counts in the other system for display by a digital display device; and manually operable display selecting control circuit means for controlling said gate circuits to determine the selection effected thereby so as to display at will either chronograph time up to 24 hours or time of day.

The manually operable chronograph

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control means may include a manually operable switch successive operations of which cause the resetting of the counters in said one system, the start of counting thereby and the termination of counting thereby.

The manually operable display selecting control means may include a manually operable switch successive operations of which cause change of the selection effected by the gate circuits.

Preferably each of the two counting systems may include an hours counter counting up to 24 hours but this is not essential and only the hours counter in the chronograph counter system may be a 24-hours counter, the counter in the other counter system being a 12-hours counter.

The invention is illustrated in and further explained in connection with the accompanying drawings, in which:—

Figure 1 which is provided for purposes of preliminary explanation only is a simplified block diagram of a conventional electronic timepiece for displaying time of day only;

Figure 2 is a circuit diagram of a 24-hour counter which is not per se part of this invention but could be used in carrying out the invention or in the known timepiece of Figure 1.

Figure 3 is a wave form diagram explanatory of the operation of the circuit of Figure 2.

Figure 4 is a simplified block diagram of an embodiment of the invention.

Figure 5 is a circuit diagram of a control circuit used in the embodiment of Figure 4;

Figure 6 is a wave form diagram explanatory of the operation of the circuit of Figure 5;

Figure 7 is a circuit diagram of a display selecting circuit used in the embodiment of Figure 4;

Figure 8 is a wave form diagram explanatory of the operation of the circuit of Figure 7;

Figure 9 is a circuit diagram of a gate circuit used in the embodiment of Figure 4; and

Figure 10 is a simplified block diagram of a second embodiment of the invention.

Like references denote like parts in the different Figures.

Referring to Figure 1, this represents a known electronic watch digitally displaying time of day only and comprising a relatively high frequency time standard oscillator the frequency of which is determined by a quartz crystal or other vibrator of highly accurate frequency. The output from the oscillator 1 is fed to a multi-stage frequency divider 2 which produces therefrom a lower time standard frequency of desired value—in the present example of 1Hz. This frequency is fed to a counter system 3

comprising a count-to-60 seconds counter 4, followed by a count-to-60 minutes counter 5 followed by a count-to-24 hours counter 6.

The count contents of the three counters 4, 5 and 6 are passed to a decoder-driver 7 of any convenient form which produces therefrom signals in a form suitable for operating a digital display 8 which displays time in hours, minutes and seconds and which may be, for example, a liquid crystal or light emitting diode display comprising a plurality of seven segment numeric display elements each of which is capable of selectively displaying, under the control of the signals from the decoder-driver 7, any numeral from 0 to 9.

The watch represented in Figure 1 is also provided with counted time adjustment means as known per se for correcting the time count in the counters 4, 5, 6 (to correct the time displayed to bring it into accord with the correct time e.g. as given by a broadcast time signal) but this is not shown in Figure 1.

Figure 2 is a circuit diagram of a form of 24-hours hours counter which could be used in carrying out this invention as for the hours counter 6 of Figure 1. It is a 6-bit counter having 6 flip-flops (FF) 9 to 14. The clock terminals C9 and C11 of the flip-flops 9 and 11 are connected to receive the one hour pulses from the counter 5 which pulses are also applied to one input of a two-input NOR gate 19.

Output from the output terminal Q9 of FF 9 is fed to one input of a two-input NOR gate 15 the output from which is applied to the data input terminal D 9 of FF 9 and is also applied to a first output terminal 6A constituting one of the count content output terminals of the counter 6. Output from the inverted output terminal $\bar{Q}9$ of FF 9 is applied to the clock terminal C10 of FF 10 and also to one input terminal of a two-input NOR gate 16 the output terminal of which is connected to the data input terminal D11 of FF 11.

The output terminal Q10 of FF 10 is connected to a second count output terminal 6B of the counter 6 and the inverted output terminal $\bar{Q}10$ of FF 10 is connected to its data input terminal D10 and also to the remaining input of the NOR gate 16.

Output terminal Q11 of FF 11 is connected to a third count output terminal 6C and also to the remaining input of NOR gate 15. The inverted output terminal $\bar{Q}11$ of FF 11 is connected to the clock terminal C12 of FF 12 and also to one input of a two-input NOR gate 17.

The output terminal Q12 of FF 12 is connected to a fourth count output terminal 6D and its inverted output terminal $\bar{Q}12$ is connected to the data input terminal D12 of

FF 12 and also to the clock terminal C13 of FF 13.

Output terminal Q13 of FF 13 is connected to a fifth count output terminal 6E and its inverted output terminal Q13 is connected to its data input terminal D13 and also to the clock terminal C14 of FF14.

The output terminal Q14 of FF 14 is connected to a sixth count output terminal 6F and its inverted output terminal Q14 is connected to its data input terminal D14 and also the remaining input terminal of NOR gate 17.

The output from NOR gate 17 is connected to one input of a two-input NOR gate 18 the output from which is applied to the remaining input of NOR gate 19.

The output terminal of NOR gate 19 is connected to the remaining input of NOR gate 18 and also to reset terminals R of the flip flops 9 to 14. Each of these flip-flops 9 to 14 changes over its output at the leading edge of a signal input to its clock terminal.

The operation of the hours counter 6 will be explained with reference to Figure 3.

In Figure 3, each wave form is identified by the reference used in Figure 2 for the point at which it occurs with a suffix *a* added. The wave form 5*a* in Figure 3 is the 1-hour pulse wave form from counter 5. It has a pulse repetition period of 1 hour and a pulse width of 0.5 sec. For obvious reasons of difficulty of drawing, this pulse width is shown greatly exaggerated in Figure 3.

Prior to the application of a 1-hour pulse from the minutes counter 5 to the hours counter 6, or after 12 o'clock and before 1 o'clock, the Q outputs of FF 9 and FF 11 are logic "0", and therefore the output from NOR gate 15 input to the data terminal D9 of FF 9 is "1". When a first pulse comes in from the minutes counter 5 the output of FF 9 becomes "1", the inverted output therefrom changes to "0" and the output from NOR gate 15 becomes "0". At the leading edge of the pulse from counter 5, the inverted output of FF 10 is "1", the output of NOR gate 16 is "0" and the output of FF 10 remains "0".

At the next step, when a second pulse comes in from the minutes counter 5, the output of NOR gate 15 is "0" and therefore the output of FF 9 becomes "0" and its inverted output becomes "1". This changes the output of FF 10 to "1" and its inverted output is "0". When said second pulse comes in, the data terminal D11 of FF 11 is "0", the output of NOR gate 16 is "0" and the output of FF 11 remains "0".

When a third pulse comes in from the minutes counter 5, the output of FF 9 changes to "1" and the output of NOR gate 15 changes to "0". Thus, data input terminal D11 of FF 11 and the output of NOR gate 16

change to "1" but the output of FF 11 remains unchanged.

When a fourth pulse comes in from the minutes counter 5, the output of FF 9 is changed to "0" and the inverted output thereof is changed to "1". As a result the output from FF 10 is changed to "0" and the output of FF 11 changes for the first time from "0" to "1".

When a fifth pulse comes in from the minutes counter 5 the outputs from the flip-flops 9 and 10 are not changed, but the output of FF 11 is changed to "0". Accordingly, at this time, the inverted output of FF 11 is changed from "0" to "1" and the output of FF 12 changes from "0" to "1" for the first time.

For the next successive 6th to 23rd 1-hour pulses from the minutes counter 5, the flip-flops 9 to 11 repeat the above described cycle of operations, FF 12 changing its output when the output from FF 11 changes from "0" to "1" and FF 13 changing its output when the inverted output of FF 12 is changed from "0" to "1".

FF 14 changes its output when the inverted output of FF 13 changes from logic "0" to "1". It will be seen, therefore, that, between the arrivals of the 23rd and 24th pulses — the output of FF 9 is "1", that of FF 10 is "1", that of FF 11 is "0", those of FF 12 and FF 13 are "0", that of FF 14 is "1", that of NOR gate 15 is "0", that of NOR gate 16 is "1", that of NOR gate 17 is "0", that of NOR gate 18 is "1", and that of NOR gate 19 is "0".

When the 24th pulse comes in from the minutes counter 5, the inverted output Q11 of FF 11 is changed to "0", but the inverted output of FF 14 remains "0", and therefore the output of NOR gate 17 becomes "1", and the output of NOR gate 18 is changed to "0". Accordingly, at the leading edge of the 24th pulse, the output of NOR gate 19 becomes "1", and this output resets all the flip-flops 9 to 14. When now, the next pulse (the 25th pulse) comes in from counter 5 the output of NOR gate 19 becomes "0" once more, the reset condition of the flip-flops 9 to 14 is released and the whole cycle of operations repeats. In this way, the input pulses from counter 5 are counted and the count content (from 0 to 23 inclusive) appears at the output terminals 6A to 6F, the unit hour count portion appearing on the terminals 6A to 6D and the ten hour count portion appearing on the terminals 6E to 6F.

It will be observed that the count contents appearing on the output terminals 6A to 6D are not in the normal BCD code, but they are in a code which is readily convertible (by the decoder-driver 7 of Figure 1) into signals which will operate the numeric display 8.

As will now be seen, the conventional timepiece illustrated in Figures 1 to 3 will display time digitally in hours, minutes and seconds, with the hours shown in accordance with a 24-hour clock so that there is no question of having to distinguish between A.M. and P.M. This is generally convenient especially to a user requiring to know the time for the purpose of complying with a time given in a railway or other transport timetable, since these timetables are usually in accordance with the 24-hour clock.

Reference is now directed to Figure 4 which is a block diagram of one embodiment of this invention and shows a timepiece which will digitally display either time of day or chronograph time. The timepiece represented in Figure 4 includes an oscillator 1, a frequency divider 2, and a counter system 3 comprising a seconds counter 4, a minutes counter 5 and an hours counter 6. These are all as in Figure 1. Associated with the counting system comprising the counters 4, 5 and 6 is a known counted time adjustment means 70 for correcting the time count in said counters to bring the count into accord with the correct time as given, for example, by a broadcast time signal. There is also a decoder-driver 7 and a digital display 8. The counter system 3 is for counting time of day. There is also a second counter system 81 for counting chronograph (stop-watch) time. This includes a chronograph control circuit 91, a count-to-60 seconds counter 101, a count-to-60 minutes counter 111 and a count-to-24 hours counter 121. The hours counter 121 like the hours counter 6 is as shown in Figure 2 and as already described.

The BCD coded count contents outputs from the seconds counters 4 and 101 are fed to a gate circuit 141 which can select one or the other for transmission to the decoder-driver 7. Similarly the contents of the minutes counter 5 or 111 are selectable by a gate circuit 151 for transmission to the decoder-driver 7 and the contents of the hours counter 6 or 121 are selectable by a third gate circuit 161 for transmission to the decoder-driver 7. The circuitry of these gate circuits 141, 151 and 161 will be described later herein. They are controlled together, to determine whether they select the counts from the counting system in block 3 or from the counting system in block 81, by a display selecting circuit 131, the circuitry of which will also be described later herein.

The chronograph control circuit 91, when operated for chronograph working, supplies the 1Hz time signal from the divider 2 to the seconds counter 101, resets the counters 101, 111 and 121 of the counting system in block 81, starts these counters counting and finally terminates the counting, these

functions being achieved, as will be seen later, by successive operations of a switch included in said control circuit.

Figure 5 is a circuit diagram of the control circuit 91 of Figure 4. 302 is a manually operable push button switch for operating the chronograph manually. The contact 302A of this switch is connected to the high potential terminal 312 of the supply voltage source (not shown). The other contact 302B is connected through a known anti-chatter circuit 322 (for preventing the undesired effects of switch chatter in the switch 302) to the respective clock terminals C332, C342 and C352 of three flip-flops 332, 342 and 352 and also to one terminal of an inverter 362. Output terminal Q332 of FF 332 is connected to the data terminal D342 of FF 342 and to one input of a three-input NOR gate 372 and also to one output terminal 91A of the control circuit 91. The output signal from this terminal 91A is used to reset the counters 101, 111 and 112 shown in Figure 4.

Output terminal Q342 of FF 342 is connected to the data terminal D352 of FF 352 and to a second input of the NOR gate 372 and also to one input of a two-input AND gate 382. Output terminal Q352 of FF 352 is connected to the data terminal D332 of FF 332 and to the remaining input of NOR gate 372. The 1Hz output from the frequency divider 2 (Figure 4) is applied to the remaining input of the AND gate 382 the output of which is connected to the second output terminal 91B of the control circuit 91. Signals from this output terminal 91B are counted by the counter system comprising the counters 101, 111 and 121 (Figure 4).

The output of NOR gate 372 is connected to one input of a two-input NOR gate 392 the output of which is connected to one input terminal of a two-input NOR gate 402. The second input of this NOR gate is connected to the output side of the inverter 362 and its output is connected to the remaining input of gate 392 and also to the set terminal S332 of FF 332.

The operation of the control circuit 91 will be explained hereinbelow with reference to wave form Figure 6 in which Figure the wave forms (except the 1Hz wave form from divider 2) are identified by the references used in Figure 5 for the points at which they occur, with an added suffix a.

Initially, when power is applied, the outputs of FF 332, 342 and 352 are all "0" and the output of NOR gate 372 is "1". Before switch 302 is operated, the output from the anti-chatter circuit 322 is "0", the input to NOR gate 402 through inverter 362 is "1" and the output of NOR gate 402 is "0". When the switch 302 is operated one pulse is fed out from the anti-chatter circuit 322 and at the same time, the output of NOR gate

402 is changed to "1", FF 332 is set and the output thereof is changed to "1". This output appears at terminal 91A and resets the counters 101, 111 and 121 (Figure 4).
 5 When switch 302 is operated a second time the output of FF 332 is changed to "0" and that of FF 342 is changed to "1". Accordingly a 1Hz signal appears at the output of AND gate 382 and is fed from
 10 terminal 91B to be counted by the seconds, minutes and hours counters 101, 111 and 121 (Figure 4) the reset condition of which is released by the change in the output of FF 342.

15 When the switch 302 is operated a third time the output of FF 342 becomes "0", the 1Hz output from AND gate 382 no longer appears, and the output of FF 352 becomes "1".

20 On the operation of the switch 302 for the fourth time the output of NOR gate 372 remains "0". However, since the data terminal D332 of FF 332, that is to say the output of FF 352, is "1", the output of FF 332 is changed to "1" and this output resets the counters 101, 111 and 112. Further
 25 successive operations of the switch 302 produce a repetition of the above described successive actions. In this way successive operations of the switch 302 in the control circuit 91 cause the outputs of the flip-flops 332 to 352 to change in order as described. When the output of FF 332 is "1", the
 30 counters 101, 111 and 121 are reset. For whatever period of time the output of FF 342 is "1", the said counters count the 1Hz signals. When the output of FF 352 is changed to "1" the time count is finished.

40 Figure 7 is a circuit diagram of the display selecting circuit 131 of Figure 4. 413 is a manually operated switch the contact 413A of which is connected to the high potential supply terminal 312 and the other contact 413B of which is connected through an anti-chatter circuit 433 to the clock terminal C443 of FF 443 the output terminal Q443 of which is connected to a first output terminal 131A of the selecting circuit 131 and the
 45 inverted output terminal Q443 is connected to the second output terminal 131B thereof.

50 The operation of the display selecting circuit 131 will now be explained with reference to Figure 8, the wave forms in which are identified by the references used in Figure 7 for the points at which they occur with an added suffix *a*.

55 Initially, when power is supplied, the output of FF 443 is "0". Upon operation of switch 413 a chatter-free switching signal pulse as shown in line 433a of Figure 8 is applied to the clock terminal C443 of Figure 8. The pulses produced by successive operations of the switch, with switch chatter thereon, are represented in line 413Ba of Figure 8. On application of the first pulse,
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due to the first operation of switch 413, the output of FF 443 is changed to "1" and its inverted output is changed to "0". On the next operation of switch 413, the output of FF 443 is changed to "0" and its inverted output is changed to "1". Thus, by successive operations of switch 413, the opposite signals which appear at the respective output terminals 131A and 131B are changed over. The signals at terminals 131A and 131B are used to control the display selecting gate circuits 141, 151 and 161 (shown in Figure 4).

Figure 9 is a circuit diagram of the gate circuit 141 of Figure 4. The other gate circuits 151 and 161 are similar except that, as will be apparent later, the gate circuit 161 has fewer transmission gates than the other gate circuits. The input terminals 131A and 131B of Figure 9 are electrically the same as the output terminals similarly referenced, of Figure 7.

Input terminal 113A is connected to the input side of an inverter 454 and also to the N channel gate electrodes of seven transmission gates (called TG hereinafter) 464 to 524. The output side of this inverter 454 is connected to the P channel gate electrodes of the said seven TGs 464 to 524.

The input terminal 131B is connected to the input side of an inverter 534 and also to the N channel gate electrodes of seven more TGs 544 to 604. The output side of the inverter 534 is connected to the P channel gate electrodes of the said seven TGs 544 to 604. The seven bit outputs representing the count in the seconds counter 4 (see also Figure 4) are respectively applied as inputs to the seven TGs 464 and 524 and the seven bit outputs representing the count in the seconds counter 101 are similarly respectively applied as inputs to the seven TGs 544 to 604. The output terminals of the TGs are connected together in corresponding pairs, 464 to 544; 474 to 554; 484 to 564
 100 and so on, and the common connection of each pair is connected to a corresponding different one of seven output terminals 141C to 141J.

When a "1" selecting signal is applied at terminal 131A and a "0" signal is applied to terminal 131B the TGs 464 to 524 conduct, i.e. are ON, and the TGs 544 to 604 are OFF and the count contents of the seconds counter 4 is passed to the output terminals through the TGs 464 to 524. On the other hand, when a "0" signal is applied to terminal 131A and a "1" signal is applied to terminal 131B, the count contents of the seconds counter 101 are transmitted to the output terminals 141C to 141J through TGs 544 to 604. Thus, if at any time the count contents of counter 4 are being passed to the terminals 141C to 141J, an operation of the switch 413 of Figure 7 will substitute the
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count in counter 101 and the next operation of switch 413 will restore, at those terminals, the count in counter 4. The terminals 141C to 141J are the bit input terminals to the decoder-driver 7 (Figure 4).

The gate circuit 151 is similar to the gate circuit 141 and the gate circuit 161 is again similar except that it has fewer transmission gates because it has only to select between the six-bit output from the 24-hours counter 6 and the six-bit output from the 24-hours counter 121 (see Figures 2 and 4).

As will now be appreciated the watch illustrated and described with reference to Figures 2 and 4 to 9 is a combined time of day indicator and chronograph in which either function can be selected at will and in which, whether in use as a time of day indicator or as a chronograph, time is displayed in hours, minutes and seconds, with hours up to and including 23, on one and the same display device. It has the same advantages when used to display time of day as the watch shown in Figure 1 and the additional advantage, when used as a chronograph, that elapsed (stop watch) time up to 24 hours can be counted and displayed.

The fact that the same display device is used to display ordinary time or chronograph time has the advantage that a clearer display of time, with larger numerals, is obtained than would be the case if separate display devices for ordinary time and for chronograph elapsed time were used and had to be accommodated in the same timepiece.

Figure 10 is a block diagram of a second embodiment of the invention. This is also a combined time of day indicator and chronograph. Like Figure 4 it has a time standard relatively high frequency oscillator 1 followed by a frequency divider 2 providing a desired relatively low frequency time standard output, in the present example of 1Hz. This is fed to a time counting system 3 comprising a count-to-60 seconds counter 4, a count-to-60 minutes counter 5 and an hour counter 6 which is, in this case, a count-to-12 counter. 70 is again a time count correcting means for bringing the count, when required, into accord with correct time. The 1Hz signal is fed also to a chronograph system 81 comprising a control circuit 91, a count-to-60 seconds counter 101, a count-to-60 minutes counter 111 and a count-to-24 hours counter 121.

The BCD count output from the seconds counter 4 in system 3 is supplied to a gate circuit 141 as also is the count output from the seconds counter 101. The gate circuit 141 is controlled by a display selecting control circuit 131 so that it selects, under the control of said control circuit, either the

count from the seconds counter 4 or that from the seconds counter 101, for passage on to the decoder-driver 7 driving the display 8. Similarly the count in the minutes counter 5 or the count in the minutes counter 111 is selectable for display by the gate circuit 151 under the control of the control circuit 131 and the count in the up-to-12 hours counter 6 or that in the hours counter 121 is selectable for display by the gate circuit 161 also controlled by the control circuit 131. The three gate circuits 141, 151 and 161 are controlled together by the said control circuit 131 so that either the counts in the three counters in system 3 or the counts in the three counters in system 81 are passed on to the decoder-driver 7 for display by the digital display device 8. 91 is the chronograph control circuit and 70 is a time correction circuit for setting the counts in the counters 4, 5 and 6 to be in accordance with correct time whenever it is required to do this. Except for the hours counter 6, which is an up-to-12 hours counter instead of an up-to-24 hours counter, the embodiment of Figure 10 is like that of Figure 4, two control circuits (91 and 131) and the three gate circuits (141, 151 and 161) serving corresponding purposes to those of the similarly referenced parts in Figure 4 so that it is unnecessary to describe them in detail again. The essential difference between the embodiments of Figures 4 and 10 is that, with Figure 4 both the time of day display and the chronograph display are up to 24 hours displays whereas, with Figure 10, only the chronograph display is up to 24 hours, the time of day display being a 12-hour display which some users may prefer. The advantage of being able to measure a long chronograph or stop watch elapsed time — up to 24 hours — is, however, still retained by the embodiment of Figure 10.

Attention is directed to our co-pending Application Nos. 46170/76, 46800/76 and 46802/76 which claim related subject matter.

WHAT WE CLAIM IS:—

1. An electronic timepiece operable at will either to display time of day or chronograph time digitally comprising a relatively high frequency time standard oscillator including a frequency determining vibrator; a multi-stage frequency divider connected to divide down the frequency of the output from said oscillator to a lower time standard frequency; two counting systems each including a seconds counter, a minutes counter and an hours counter, at least one of said systems including an hours counter counting up to 24 hours; manually operable chronograph control circuit means for feeding said lower time standard



count in counter 101 and the next operation of switch 413 will restore, at those terminals, the count in counter 4. The terminals 141C to 141J are the bit input terminals to the decoder-driver 7 (Figure 4).

The gate circuit 151 is similar to the gate circuit 141 and the gate circuit 161 is again similar except that it has fewer transmission gates because it has only to select between the six-bit output from the 24-hours counter 6 and the six-bit output from the 24-hours counter 121 (see Figures 2 and 4).

As will now be appreciated the watch illustrated and described with reference to Figures 2 and 4 to 9 is a combined time of day indicator and chronograph in which either function can be selected at will and in which, whether in use as a time of day indicator or as a chronograph, time is displayed in hours, minutes and seconds, with hours up to and including 23, on one and the same display device. It has the same advantages when used to display time of day as the watch shown in Figure 1 and the additional advantage, when used as a chronograph, that elapsed (stop watch) time up to 24 hours can be counted and displayed.

The fact that the same display device is used to display ordinary time or chronograph time has the advantage that a clearer display of time, with larger numerals, is obtained than would be the case if separate display devices for ordinary time and for chronograph elapsed time were used and had to be accommodated in the same timepiece.

Figure 10 is a block diagram of a second embodiment of the invention. This is also a combined time of day indicator and chronograph. Like Figure 4 it has a time standard relatively high frequency oscillator 1 followed by a frequency divider 2 providing a desired relatively low frequency time standard output, in the present example of 1Hz. This is fed to a time counting system 3 comprising a count-to-60 seconds counter 4, a count-to-60 minutes counter 5 and an hour counter 6 which is, in this case, a count-to-12 counter. 70 is again a time count correcting means for bringing the count, when required, into accord with correct time. The 1Hz signal is fed also to a chronograph system 81 comprising a control circuit 91, a count-to-60 seconds counter 101, a count-to-60 minutes counter 111 and a count-to-24 hours counter 121.

The BCD count output from the seconds counter 4 in system 3 is supplied to a gate circuit 141 as also is the count output from the seconds counter 101. The gate circuit 141 is controlled by a display selecting control circuit 131 so that it selects, under the control of said control circuit, either the

count from the seconds counter 4 or that from the seconds counter 101, for passage on to the decoder-driver 7 driving the display 8. Similarly the count in the minutes counter 5 or the count in the minutes counter 111 is selectable for display by the gate circuit 151 under the control of the control circuit 131 and the count in the up-to-12 hours counter 6 or that in the hours counter 121 is selectable for display by the gate circuit 161 also controlled by the control circuit 131. The three gate circuits 141, 151 and 161 are controlled together by the said control circuit 131 so that either the counts in the three counters in system 3 or the counts in the three counters in system 81 are passed on to the decoder-driver 7 for display by the digital display device 8. 91 is the chronograph control circuit and 70 is a time correction circuit for setting the counts in the counters 4, 5 and 6 to be in accordance with correct time whenever it is required to do this. Except for the hours counter 6', which is an up-to-12 hours counter instead of an up-to-24 hours counter, the embodiment of Figure 10 is like that of Figure 4, two control circuits (91 and 131) and the three gate circuits (141, 151 and 161) serving corresponding purposes to those of the similarly referenced parts in Figure 4 so that it is unnecessary to describe them in detail again. The essential difference between the embodiments of Figures 4 and 10 is that, with Figure 4 both the time of day display and the chronograph display are up to 24 hours displays whereas, with Figure 10, only the chronograph display is up to 24 hours, the time of day display being a 12-hour display which some users may prefer. The advantage of being able to measure a long chronograph or stop watch elapsed time — up to 24 hours — is, however, still retained by the embodiment of Figure 10.

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WHAT WE CLAIM IS:—

1. An electronic timepiece operable at will either to display time of day or chronograph time digitally comprising a relatively high frequency time standard oscillator including a frequency determining vibrator; a multi-stage frequency divider connected to divide down the frequency of the output from said oscillator to a lower time standard frequency; two counting systems each including a seconds counter, a minutes counter and an hours counter, at least one of said systems including an hours counter counting up to 24 hours; manually operable chronograph control circuit means for feeding said lower time standard



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- frequency to said one system and simultaneously resetting the counters therein, starting counting thereby and subsequently stopping counting thereby; a plurality of selecting gate circuits for selecting the seconds, minutes and hours counts in said one system or the seconds, minutes and hours counts in the other system for display by a digital display device; and manually operable display selecting control circuit means for controlling said gate circuits to determine the selection effected thereby so as to display at will chronograph time up to 24 hours or time of day.
2. A timepiece as claimed in claim 1 wherein said vibrator is a piezo-electric crystal vibrator.
3. A timepiece as claimed in claim 1 or 2 wherein the manually operable chronograph control means include a manually operable switch successive operations of which cause the re-setting of the counters in said one system, the start of counting thereby and the termination of counting thereby.
4. A timepiece as claimed in claim 1, 2 or 3 wherein the manually operable display selecting control means include a manually operable switch successive operations of which cause change of the selection effected by the gate circuits.
5. A timepiece as claimed in any of claims 1 to 4 in which each of the two counting systems includes an hours counter counting up to 24.
6. A timepiece as claimed in any of claims 1 to 4 in which said one system includes an hours counter counting up to 24 and the other system includes an hours counter counting up to 12.
7. A timepiece as claimed in any of the preceding claims and including at least one hours counter substantially as herein described with reference to Figure 2 of the accompanying drawings.
8. A timepiece as claimed in any of claims 1 to 6 and including a manually operable chronograph control circuit substantially as herein described with reference to Figure 5 of the accompanying drawings.
9. A timepiece as claimed in any of claims 1 to 6 and including a plurality of gate circuits substantially as herein described with reference to Figure 9 of the accompanying drawings.
10. A timepiece as claimed in any of claims 1 to 6 or in claim 9 and including a manually operable display selecting control circuit substantially as herein described with reference to Figure 7 of the accompanying drawings.
11. Timepieces as claimed in any of the preceding claims and substantially as herein described with reference to Figure 4 or Figure 10 of the accompanying drawings.

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