WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:

a semiconductor substrate including a memory cell region and contact regions;

a first stacked structure on the semiconductor substrate;

a second stacked structure disposed between the semiconductor substrate and the first stacked structure;

a plurality of cell plugs extending in a vertical direction crossing a top surface of the semiconductor substrate and arranged in the first stacked structure and the second stacked structure in the memory cell region; and

a plurality of supports extending in the vertical direction and arranged in the first stacked structure in the contact region,

wherein the second stacked structure is arranged in a different level from the plurality of supports,

wherein the plurality of supports pass through the first stacked structure and each of the supports includes a vertical portion extending in the vertical direction and an insulation portion surrounding a sidewall of the vertical portion,

wherein the insulation portion includes a first portion which is disposed at one side of the vertical portion and a second portion which is disposed at another side of the vertical portion,

and, wherein a length of the first portion is longer than a length of the second portion.

2. The semiconductor memory device of claim 1, wherein the first stacked structure includes a plurality of interlayer insulating layers and a plurality of conductive layers stacked alternately with each other, and

wherein the insulation portion is arranged between the plurality of conductive layers and the vertical portion.

3. The semiconductor memory device of claim 1, wherein the plurality of supports include polysilicon extending in the vertical direction and a silicon oxide surrounding a sidewall of the polysilicon.

4. The semiconductor memory device of claim 3, wherein the silicon oxide is arranged between the polysilicon and the first stacked structure.

5. The semiconductor memory device of claim 1, wherein the plurality of supports include a semiconductor material and an oxide of the semiconductor material.

6. The semiconductor memory device of claim 1, wherein the first stacked structure is formed to have a stepped structure in the contact region, and

wherein the supports pass through the stepped structure of the first stacked structure.

7. A semiconductor memory device, comprising:

a semiconductor substrate including a peripheral circuit structure;

a first stacked structure including a plurality of first interlayer insulating layers and a plurality of first conductive layers stacked alternately with each other in a vertical direction crossing a top surface of the semiconductor substrate;

a second stacked structure arranged between the first stacked structure and the semiconductor substrate and including a plurality of second interlayer insulating layers and a plurality of second conductive layers stacked alternately with each other in the vertical direction;

a cell plug arranged in the first stacked structure and the second stacked structure;

a first support arranged in the first stacked structure and having a smaller length than the cell plug in the vertical direction; and

a connection structure arranged between the second stacked structure and the peripheral circuit structure,

wherein the first support pass through the first stacked structure and the first support includes a vertical portion

extending in the vertical direction and an insulation portion surrounding a sidewall of the vertical portion,

wherein the insulation portion includes a first portion which is disposed at one side of the vertical portion and a second portion which is disposed at another side of the vertical portion, wherein a length of the first portion is longer than a length of the second portion.

8. The semiconductor memory device of claim 7, wherein the first stacked structure includes a stepped structure,

wherein the second stacked structure is formed to open an area between the stepped structure of the first stacked structure and the semiconductor substrate, and

wherein the first support passes through the stepped structure of the first stacked structure.

9. The semiconductor memory device of claim 7, further comprising a second support passing through the first stacked structure and the second stacked structure,

wherein the first support has a smaller length than the second support in the vertical direction.

10. The semiconductor memory device of claim 9, wherein the second support includes a same material as the cell plug.

11. The semiconductor memory device of claim 7, wherein the first support includes a vertical portion extending in the vertical direction and an insulation portion arranged between the vertical portion and the plurality of first conductive layers, and

wherein the insulation portion includes a different material from the vertical portion.

12. A method of manufacturing a semiconductor memory device, the method comprising:

forming a first preliminary stacked structure including a plurality of first material layers and a plurality of second material layers stacked alternately with each other in a first direction;

forming a first support passing through the first preliminary stacked structure;

forming a second preliminary stacked structure including a plurality of third material layers and a plurality of fourth material layers stacked alternately with each other in the first direction on the first preliminary stacked structure, the second preliminary stacked structure exposing the first support;

forming a gap-filling insulating layer covering the first support;

forming a cell plug passing through the first preliminary stacked structure and the second preliminary stacked structure;

forming a slit passing through the first preliminary stacked structure and the second preliminary stacked structure;

removing the plurality of second material layers and the plurality of fourth material layers through the slit to form a plurality of first openings from which the plurality of second material layers are removed and a plurality of second openings from which the plurality of fourth material layers are removed;

oxidizing a sidewall of the first support through the plurality of first openings; and

forming a conductive layer in each of the plurality of first openings and the plurality of second openings,

wherein the plurality of supports pass through the first stacked structure and each of the supports includes a vertical portion extending in the vertical direction and an insulation portion surrounding a sidewall of the vertical portion,

wherein the insulation portion includes a first portion which is disposed at one side of the vertical portion and a second portion which is disposed at another side of the vertical portion,

and, wherein a length of the first portion is longer than a length of the second portion.

13. The method of claim 12, wherein the first support includes a material having an etch selectivity with respect to the plurality of first material layers and the plurality of second

material layers.

14. The method of claim 13, wherein the first support includes polysilicon.

15. The method of claim 13, wherein a second support passing through the first preliminary stacked structure and the second preliminary stacked structure is formed during the forming of the cell plug.

16. The method of claim 15, wherein the second preliminary stacked structure includes an end portion having a stepped structure, and

wherein the second support passes through the stepped structure of the second preliminary stacked structure.

17. The method of claim 13, wherein the first preliminary stacked structure includes an end portion having a stepped structure, and

wherein the first support passes through the stepped structure of the first preliminary stacked structure.

18. The method of claim 13, wherein the first preliminary stacked structure is formed on a first substrate, and

the first substrate is removed after the conductive layer is formed.

19. The method of claim 18, further comprising, before the first substrate is removed:

forming a bit line coupled to the cell plug;

forming a first connection structure connected to the bit line;

providing a second substrate including a peripheral circuit structure and a second connection structure connected to the peripheral circuit structure; and

bonding the first connection structure and the second connection structure to each other.