What is claimed is:

1. A method for forming a transistor, comprising:

forming a transistor body, including:

forming a fin of amorphous semiconductor material on a crystalline substrate, the fin having a cross-sectional thickness in at least one direction less than a minimum feature size; and

performing a solid phase epitaxy (SPE) process to crystallize the amorphous semiconductor material using the crystalline substrate to seed the crystalline growth, the transistor body being formed in the crystallized semiconductor pillar between a first source/drain region and a second source/drain region;

forming a surrounding gate insulator around the semiconductor pillar; and

forming a surrounding gate around and separated from the semiconductor pillar by the surrounding gate insulator.

2. The method of claim 1, wherein the fin has a cross-sectional thickness in a first direction corresponding to a minimum feature length and a cross-sectional thickness in a second direction orthogonal to the first direction less than the minimum feature length.

3. The method of claim 1, wherein forming a fin of amorphous semiconductor material on a crystalline substrate includes forming a pillar of amorphous silicon on a crystalline silicon substrate.

4. The method of claim 1, wherein forming the surrounding gate insulator includes forming a silicon oxide.

5. The method of claim 1, wherein forming a surrounding gate includes forming a polysilicon gate.

6. The method of claim 1, further comprising recessing the surrounding gate such that the surrounding gate has a height less than a height of the fin.

7. The method of claim 1, further comprising forming the first source/drain region at a first end of the fin and forming the second source/drain region at a second end of the fin.

8. The method of claim 1, wherein the first source/drain region is beneath the second source/drain region, and a channel region is vertically oriented between the first and second source/drain regions.

9. A method for forming a transistor, comprising:

forming a silicon nitride layer on a silicon wafer;

etching a hole in the silicon nitride, the hole extending through the silicon nitride layer to the silicon wafer and being defined by the sides of the silicon nitride layer;

forming amorphous silicon sidewall spacers on the sides of the silicon nitride that define the hole;

removing the silicon nitride layer, leaving the amorphous silicon sidewall spacers on the silicon wafer;

crystallizing the sidewall spacers;

masking and etching the sidewall spacers to form at least one silicon fin from the sidewall spacers, the silicon fin being positioned over a doped region to function as a first source/drain region for the transistor;

forming a surrounding gate insulator around the silicon fin;

forming a surrounding gate around and separated from the silicon fin by the surrounding gate insulator; and

forming a second source/drain region in a top portion of the silicon fin.

10. The method of claim 9, wherein the height of the silicon fin is less than the minimum feature size.

11. The method of claim 9, wherein the fin has a cross-sectional thickness in a first direction corresponding to a minimum feature length and a cross-sectional thickness in a second direction orthogonal to the first direction less than the minimum feature length.

12. The method of claim 9, wherein forming a surrounding gate insulator around the silicon fins includes performing a thermal oxidation process.

13. The method of claim 9, further comprising patterning and implanting the doped region to function as the first source/drain region before forming the amorphous silicon sidewall spacers.

14. The method of claim 9, wherein forming the surrounding gate includes forming a metal gate.

15. The method of claim 9, wherein forming the surrounding gate includes forming a polysilicon gate.

16. A method for forming an array of transistors, comprising:

forming buried source/drain regions in a silicon wafer;

etching a plurality of holes in a silicon nitride layer on the silicon wafer, the holes extending through the silicon nitride to the silicon wafer, each hole being defined by edges of the silicon nitride layer;

forming amorphous silicon sidewall spacers on the sides of the silicon nitride that define the holes;

removing the silicon nitride layer, leaving the amorphous silicon sidewall spacers on the silicon wafer in a plurality of rectangular tracks;

crystallizing the sidewall spacers;

masking and etching the sidewall spacers to form a plurality of silicon fins from the sidewall spacers, the silicon fins being positioned over the buried source/drain regions;

forming a surrounding gate insulator around each of the silicon fins;

forming a surrounding gate around and separated from each of the silicon fins by the surrounding gate insulator; and

forming a second source/drain region in a top portion of the silicon fins.

17. The method of claim 16, further comprising forming at least one gate line adjacent to and in contact with the surrounding gates for at least two transistors.

18. The method of claim 17, wherein forming at least one gate line includes forming two gate lines adjacent to and in contact with the surrounding gate, the two gate lines being on opposing silicon fins.

19. The method of claim 17, wherein forming at least one gate line includes forming the at least one gate line to contact the surrounding gates in a row of transistors.

20. The method of claim 17, wherein forming at least one gate line includes forming the at least one gate line to contact the surrounding gates in a column of transistors.

21. A transistor, comprising:

a crystalline substrate;

a crystalline semiconductor fin on the substrate, the semiconductor fin having a cross-sectional dimension that is less than a minimum feature size, wherein the fin provides a vertically-oriented channel between a lower source/drain region and an upper source/drain region;

a gate insulator formed around the fin; and

a surrounding gate formed around and separated from the fin by the gate insulator.

22. The transistor of claim 21, wherein the crystalline substrate is a silicon wafer.

23. The transistor of claim 21, wherein the gate insulator includes silicon oxide.

24. The transistor of claim 21, wherein the gate includes polysilicon.

25. The transistor of claim 21, wherein the gate includes metal.

26. A transistor, comprising:

a crystalline silicon substrate;

a first source/drain region formed in the crystalline silicon substrate;

a crystalline silicon fin on the substrate and over the first source/drain region, the silicon fin having a cross-sectional dimension that is less than a minimum feature size;

a second source/drain region formed in a top portion of the fin to define a vertically-oriented channel region in the fin between the first and second source/drain regions;

a gate insulator formed around the fin; and

a surrounding gate formed around and separated from the fin by the gate insulator.

27. The transistor of claim 26, wherein the gate insulator includes a silicon oxide.

28. The transistor of claim 26, wherein the silicon oxide gate insulator is a thermally-grown silicon oxide.

29. The transistor of claim 26, wherein the surrounding gate includes a polysilicon surrounding gate.

30. The transistor of claim 26, wherein the surrounding gate includes a metal surrounding gate.

31. A semiconductor structure, comprising:

an array of transistors arranged in columns and rows, each transistor including a first source/drain region, a second source/drain region above the first source/drain region, and a vertically-oriented channel region between the first and second source/drain regions, the channel region being formed in a crystalline semiconductor fin having a cross-sectional thickness that is less than a minimum feature size, each transistor further including a gate insulator formed around the fin and a surrounding gate formed around and separated from the fin by the gate insulator;

the columns of fin structures having a center-to-center spacing of approximately two minimum feature sizes; and

the rows of fins structures having a center-to-center spacing of approximately one minimum feature size.

32. The structure of claim 31, wherein a first row and an adjacent second row has a center-to-center spacing of the minimum feature size less the thickness of the fin structures, and the second row and an adjacent third row has a center-to-center spacing of the minimum feature size plus the thickness of the fin structures.

33. The structure of claim 31, wherein the fin structure has a long side and a short side, the structure further comprising at least one gate line adjacent to the long side.

34. The structure of claim 31, wherein the fin structure has a long side and a short side, the structure further comprising at least one gate line adjacent to the short side.

35. A semiconductor structure, comprising:

a crystalline substrate; and

a semiconductor fin structure formed on the substrate in contact with a first source/drain region, the semiconductor fin having a thickness cross-sectional dimension less than a minimum feature size, the semiconductor pillar having a crystallized bottom portion and an amorphous top portion indicative of a partially-completed solid phase epitaxy (SPE) process.

36. The structure of claim 35, wherein the substrate includes a silicon wafer, and the semiconductor fin structure including silicon.

37. The structure of claim 35, wherein the semiconductor fin structure is one of a plurality of semiconductor fin structures formed in an array of columns and rows, the fins having a center-to-center spacing of approximately two minimum feature sizes between the columns of fin structures.

38. The structure of claim 35, wherein the semiconductor fin structure is one of a plurality of semiconductor fin structures formed in an array of columns and rows, the fins having a center-to-center spacing of approximately one minimum feature size between the rows of fin structures.

39. The structure of claim 35, wherein the semiconductor fin structure is one of a plurality of semiconductor fin structures formed in an array of columns and rows, a first row and an adjacent second row has a center-to-center spacing of a minimum feature size interval (NF) less the thickness of the fin structures, and the second row and an adjacent third row has a center-to-center spacing of the minimum feature size interval (NF) plus the thickness of the fin structures.

What is claimed is:

1. A method for forming a transistor, comprising: forming a transistor body, including: forming a fin of amorphous semiconductor material on a substantially planar surface of a crystalline substrate, the fin formed on the surface having a cross-sectional thickness in at least one direction less than a minimum feature size, wherein the at least one direction is substantially parallel to the surface of the substrate; and performing a solid phase epitaxy (SPE) process to crystallize the amorphous semiconductor material using the crystalline substrate to seed the crystalline growth from the substrate in a direction away from the substrate to transform the fin of amorphous semiconductor material into a crystallized fin, the transistor body being formed in the crystallized fin between a first source/drain region and a second source/drain region; forming a surrounding gate insulator around the crystallized fin; and forming a surrounding gate around and separated from the crystallized fin by the surrounding gate insulator.

2. The method of claim 1, wherein the fin has a cross-sectional thickness in a first direction corresponding to a minimum feature length and a cross-sectional thickness in a second direction orthogonal to the first direction less than the minimum feature length, wherein both the first direction and the second direction are substantially parallel to the surface of the substrate.

3. The method of claim 1, wherein forming a fin of amorphous semiconductor material on a crystalline substrate includes forming a pillar of amorphous silicon on a crystalline silicon substrate.

4. The method of claim 1, wherein forming the surrounding gate insulator includes forming a silicon oxide.

5. The method of claim 1, wherein forming a surrounding gate includes forming a polysilicon gate.

6. A method for forming a transistor, comprising: forming a transistor body, including: forming a fin of amorphous semiconductor material on a crystalline substrate, the fin having a cross-sectional thickness in at least one direction less than a minimum feature size; and performing a solid phase epitaxy (SPE) process to crystallize the amorphous semiconductor material using the crystalline substrate to seed the crystalline growth to transform the fin of amorphous semiconductor material into a crystallized fin, the transistor body being formed in the crystallized fin between a first source/drain region and a second source/drain region; forming a surrounding gate insulator around the crystallized fin; forming a surrounding gate around and separated from the crystallized fin by the surrounding gate insulator; and recessing the surrounding gate such that the surrounding gate has a height less than a height of the fin.

7. The method of claim 1, further comprising forming the first source/drain region at a first end of the fin and forming the second source/drain region at a second end of the fin.

8. The method of claim 1, wherein the first source/drain region is beneath the second source/drain region, and a channel region is vertically oriented between the first and second source/drain regions.

9. A method for forming a transistor, comprising: forming a silicon nitride layer on a silicon wafer; etching a hole in the silicon nitride, the hole extending through the silicon nitride layer to the silicon wafer and being defined by the sides of the silicon nitride layer; forming amorphous silicon sidewall spacers on the sides of the silicon nitride that define the hole; removing the silicon nitride layer, leaving the amorphous silicon sidewall spacers on the silicon wafer; crystallizing the sidewall spacers; masking and etching the sidewall spacers to form at least one silicon fin from the sidewall spacers, the silicon fin being positioned over a doped region to function as a first source/drain region for the transistor; forming a surrounding gate insulator around the silicon fin; forming a surrounding gate around and separated from the silicon fin by the surrounding gate insulator; and forming a second source/drain region in a top portion of the silicon fin.

10. The method of claim 9, wherein the height of the silicon fin is less than the minimum feature size.

11. The method of claim 9, wherein the fin has a cross-sectional thickness in a first direction corresponding to a minimum feature length and a cross-sectional thickness in a second direction orthogonal to the first direction less than the minimum feature length.

12. The method of claim 9, wherein forming a surrounding gate insulator around the silicon fins includes performing a thermal oxidation process.

13. The method of claim 9, further comprising patterning and implanting the doped region to function as the first source/drain region before forming the amorphous silicon sidewall spacers.

14. The method of claim 9, wherein forming the surrounding gate includes forming a metal gate.

15. The method of claim 9, wherein forming the surrounding gate includes forming a polysilicon gate.

16. A method for forming an array of transistors, comprising: forming buried source/drain regions in a silicon wafer; etching a plurality of holes in a silicon nitride layer on the silicon wafer, the holes extending through the silicon nitride to the silicon wafer, each hole being defined by edges of the silicon nitride layer; forming amorphous silicon sidewall spacers on the sides of the silicon nitride that define the holes; removing the silicon nitride layer, leaving the amorphous silicon sidewall spacers on the silicon wafer in a plurality of rectangular tracks; crystallizing the sidewall spacers; masking and etching the sidewall spacers to form a plurality of silicon fins from the sidewall spacers, the silicon fins being positioned over the buried source/drain regions; forming a surrounding gate insulator around each of the silicon fins; forming a surrounding gate around and separated from each of the silicon fins by the surrounding gate insulator; and forming a second source/drain region in a top portion of the silicon fins.

17. The method of claim 16, further comprising forming at least one gate line adjacent to and in contact with the surrounding gates for at least two transistors.

18. The method of claim 17, wherein forming at least one gate line includes forming two gate lines adjacent to and in contact with the surrounding gate, the two gate lines being on opposing silicon fins.

19. The method of claim 17, wherein forming at least one gate line includes forming the at least one gate line to contact the surrounding gates in a row of transistors.

20. The method of claim 17, wherein forming at least one gate line includes forming the at least one gate line to contact the surrounding gates in a column of transistors.