

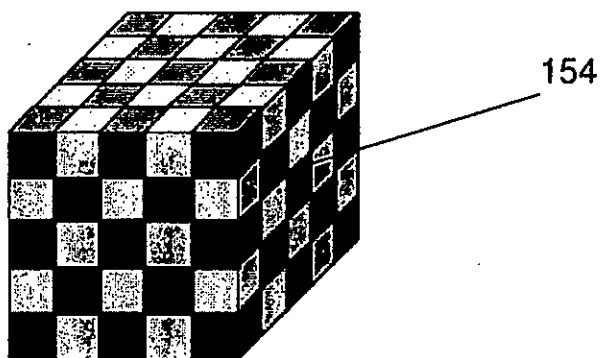
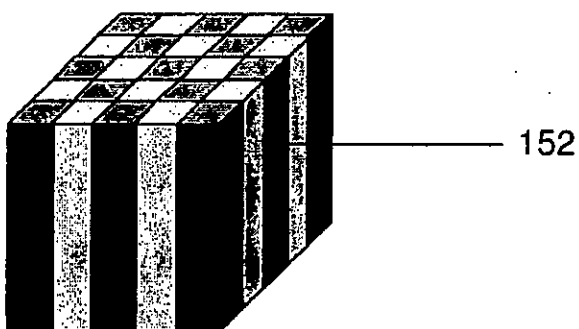
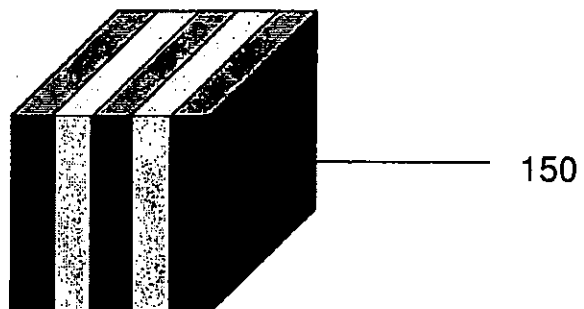


Figure 1A

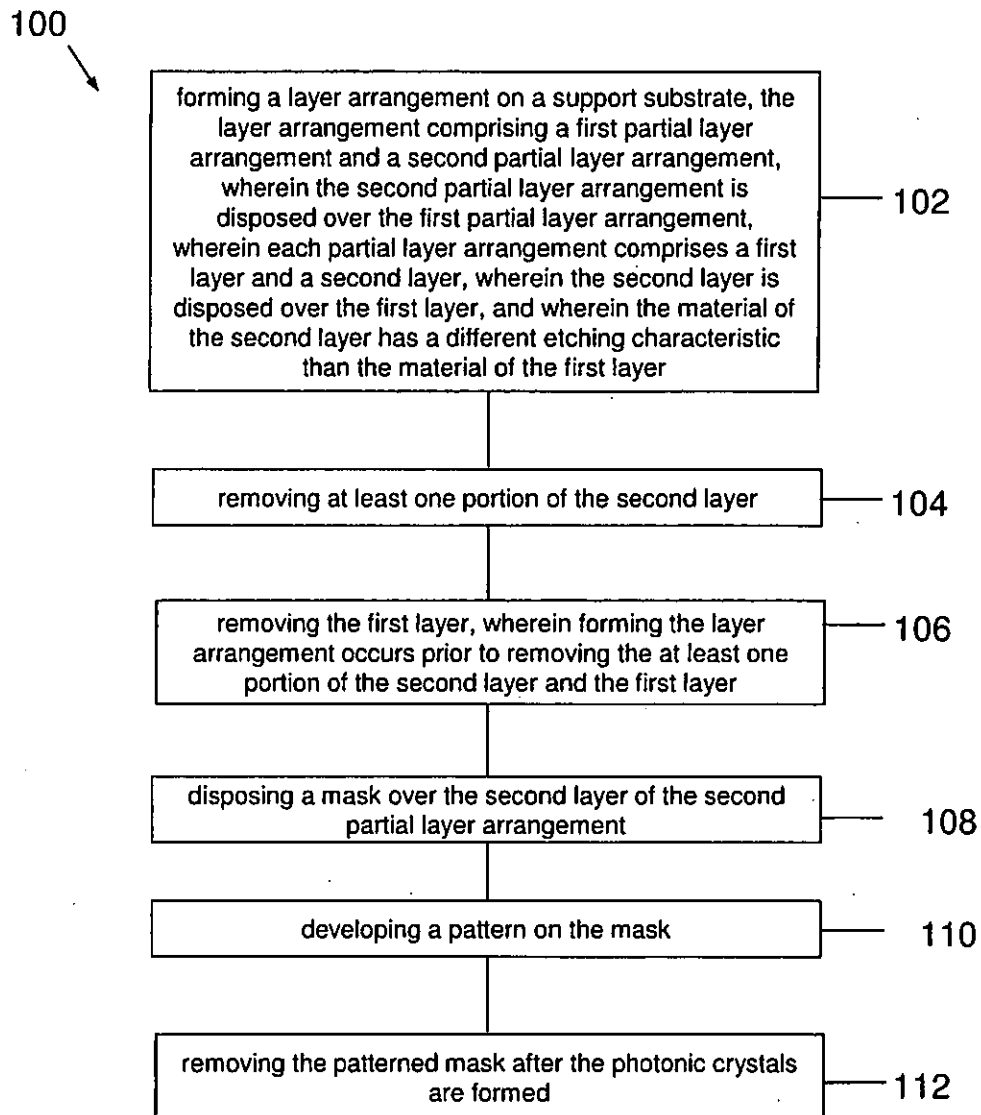


Figure 1B

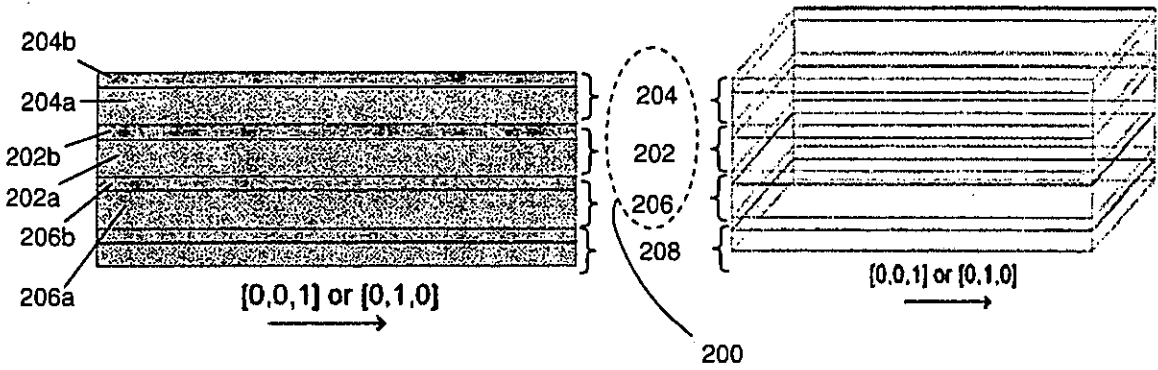


Figure 2A

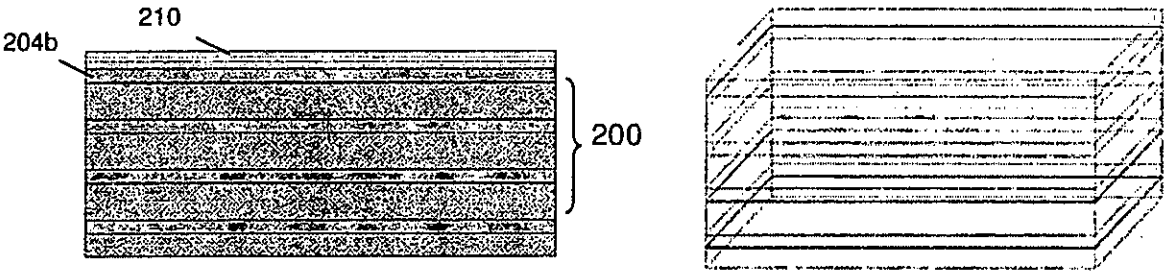


Figure 2B

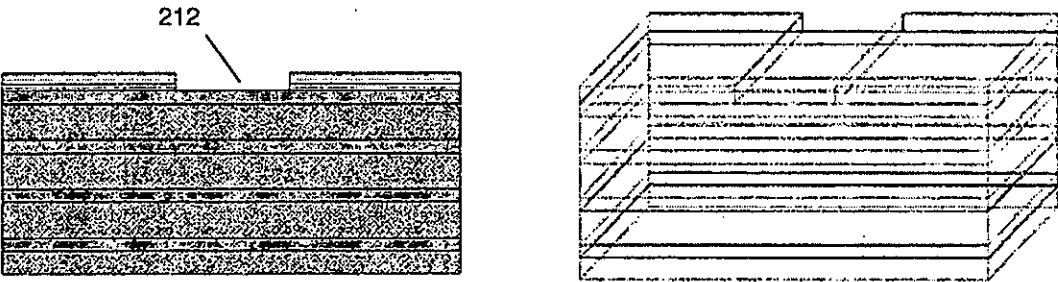


Figure 2C

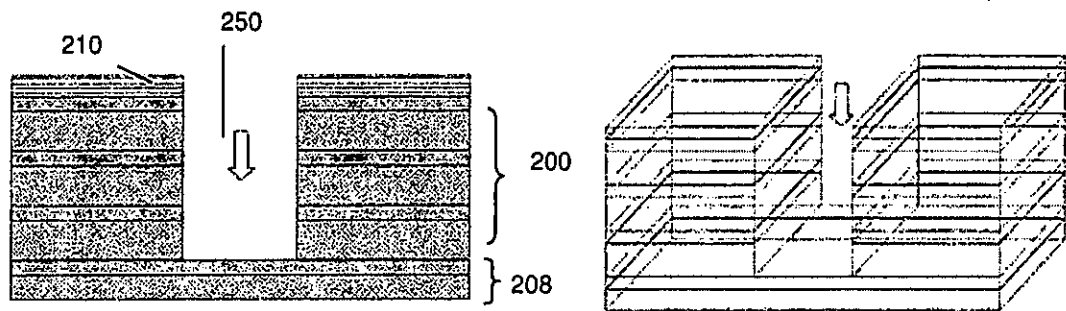


Figure 2D

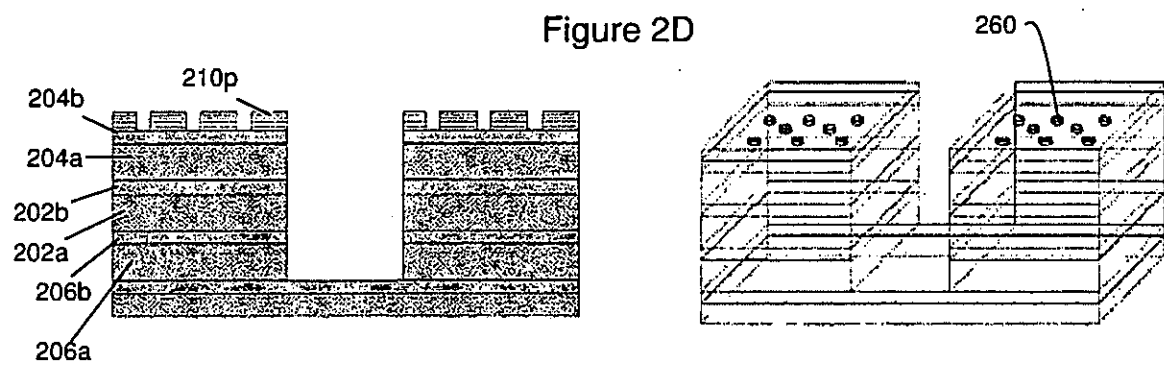


Figure 2E

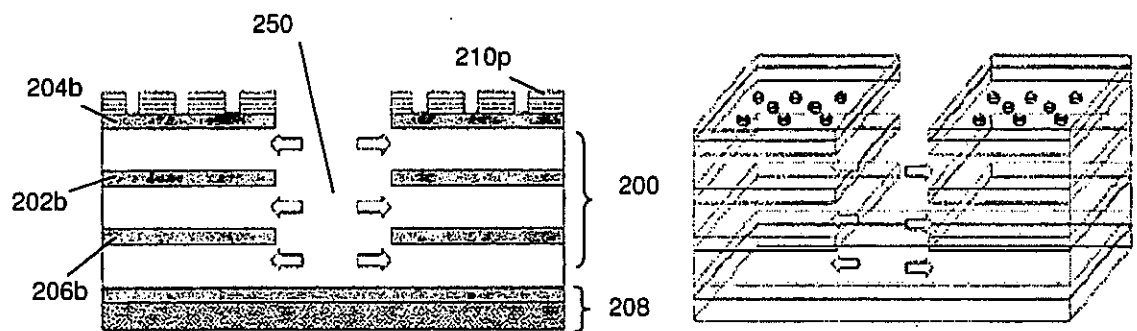


Figure 2F

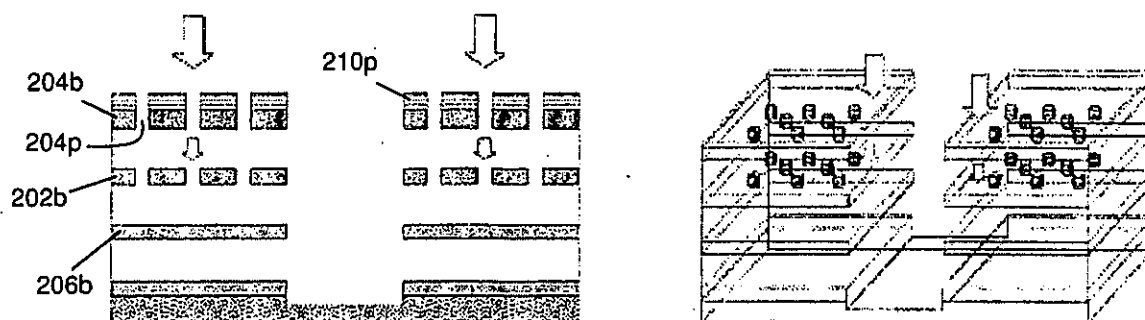


Figure 2G

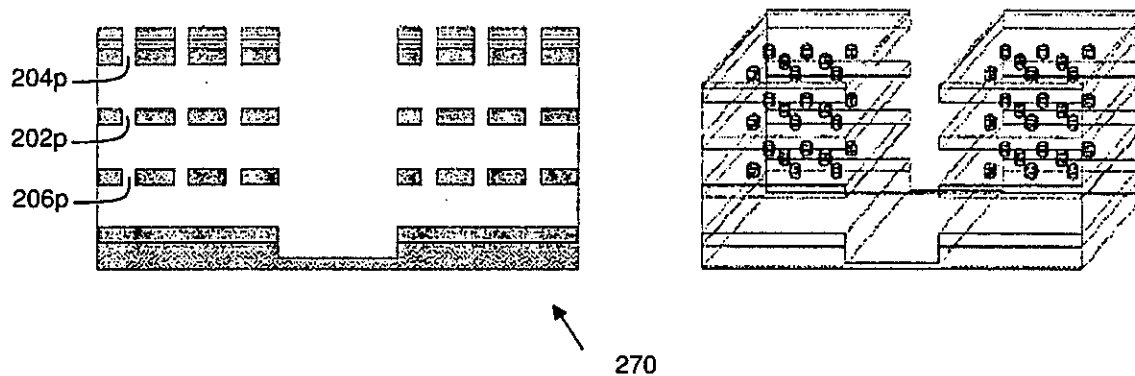


Figure 2H

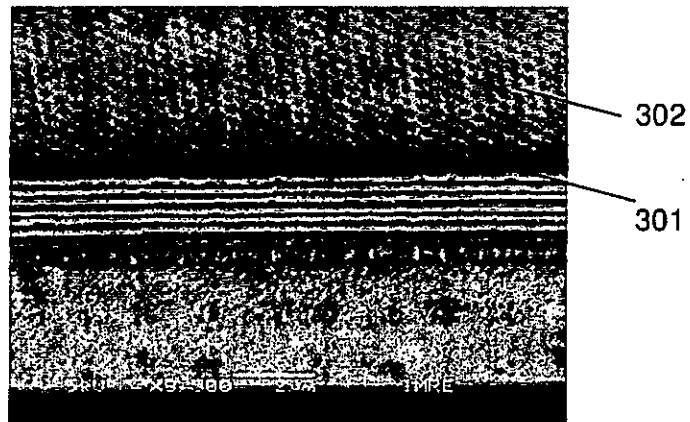


Figure 3A



Figure 3B

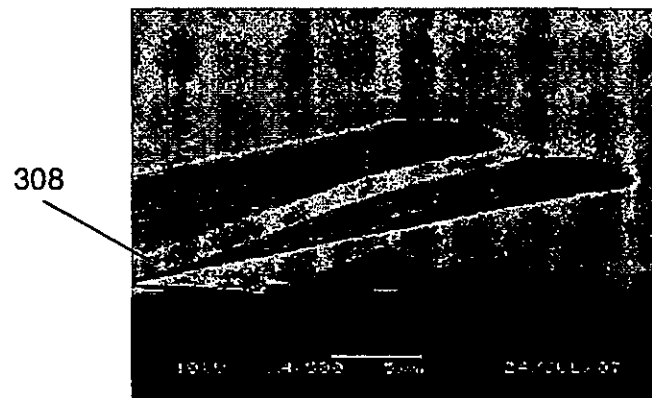


Figure 3C

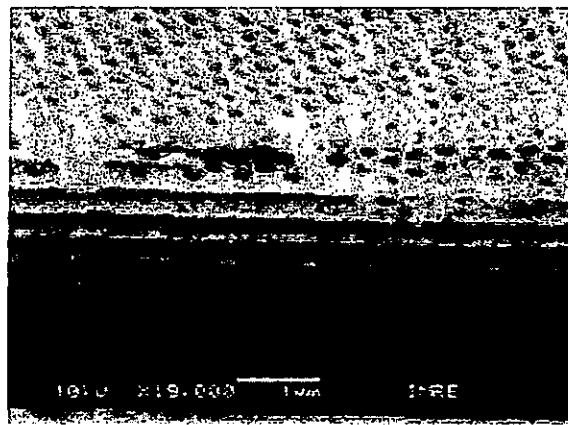


Figure 4A

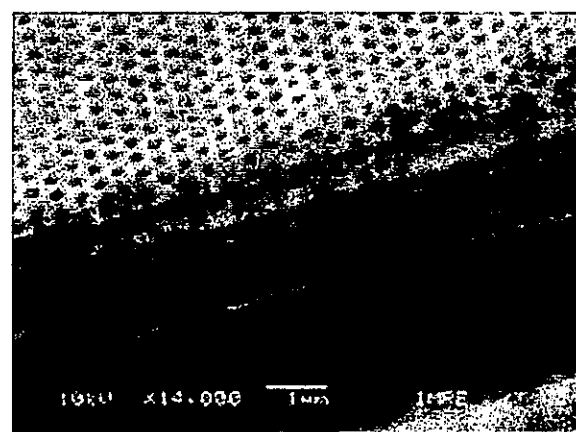


Figure 4B

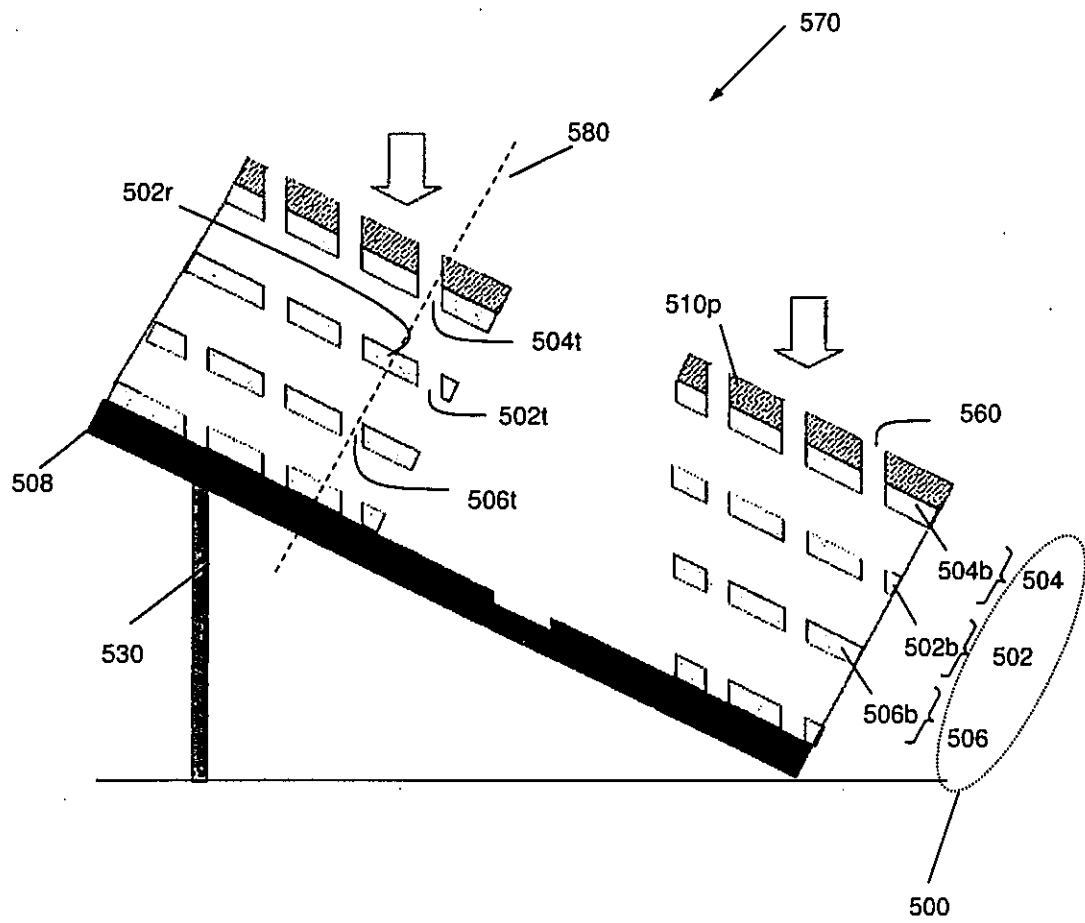


Figure 5

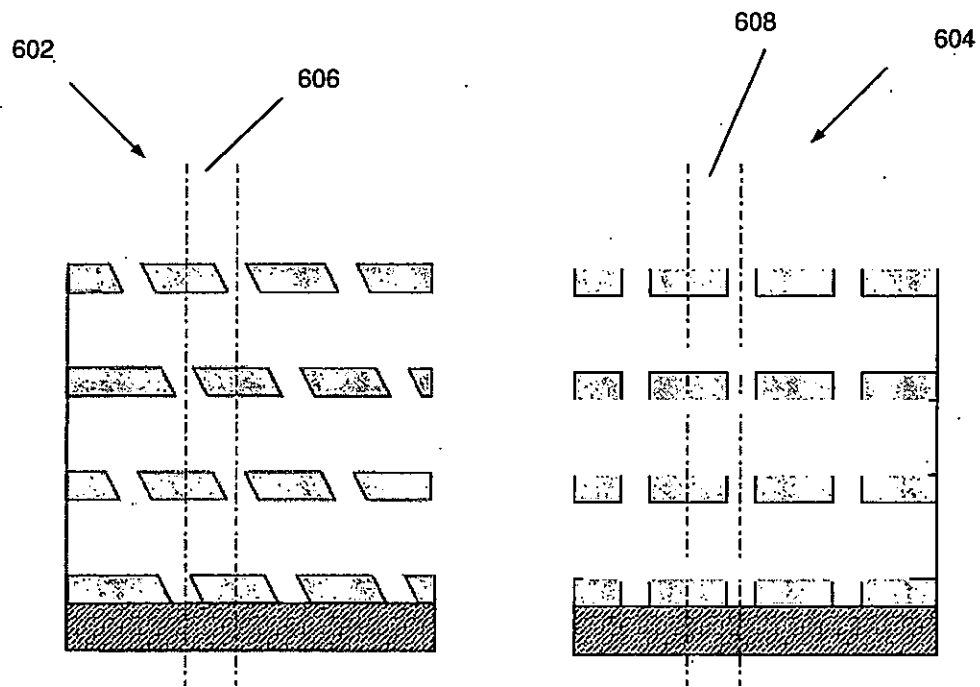


Figure 6

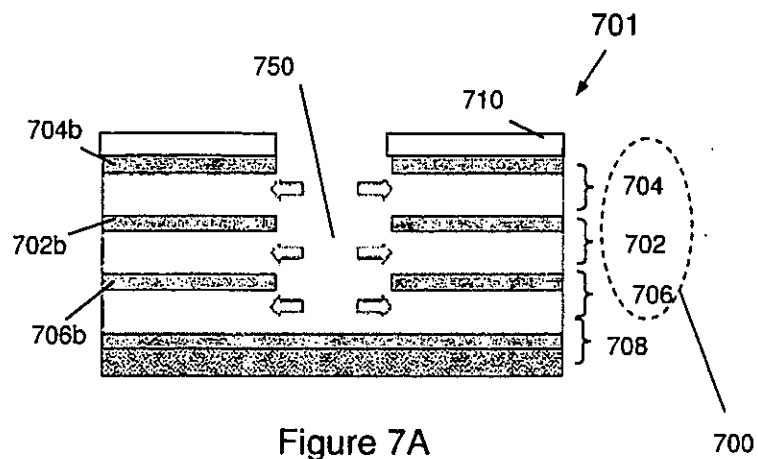


Figure 7A

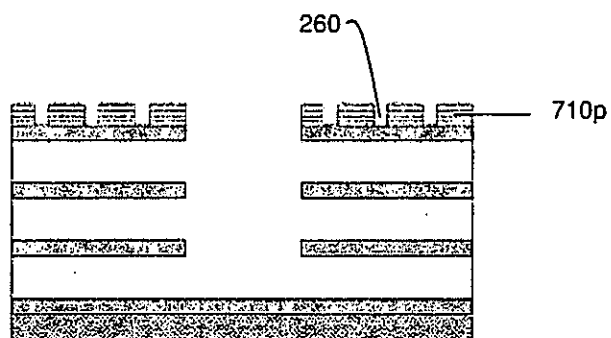


Figure 7B

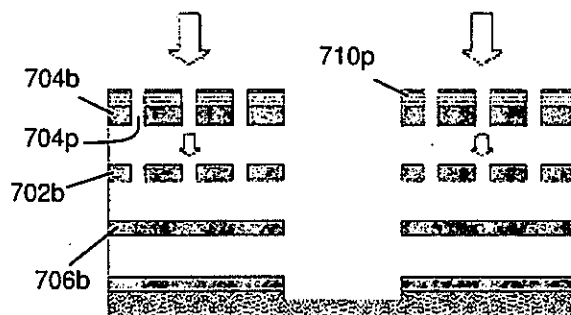


Figure 7C

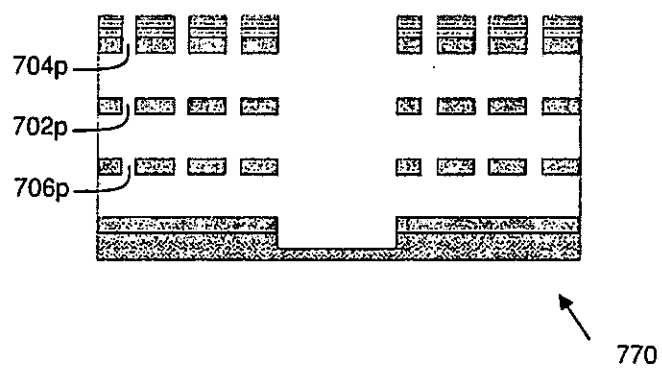


Figure 7D

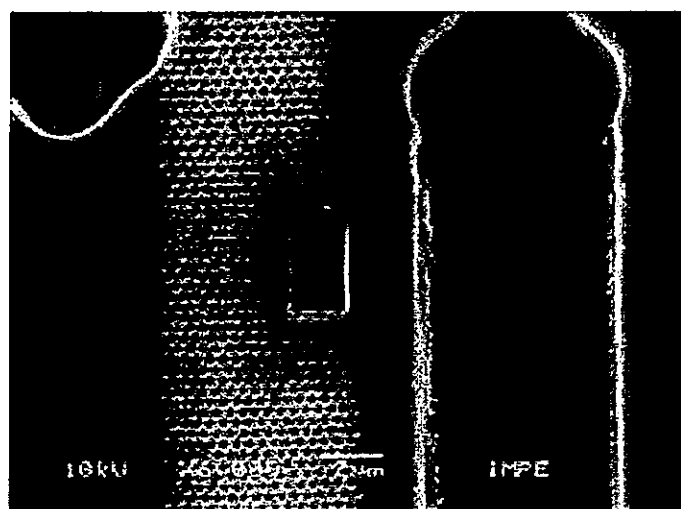


Figure 8

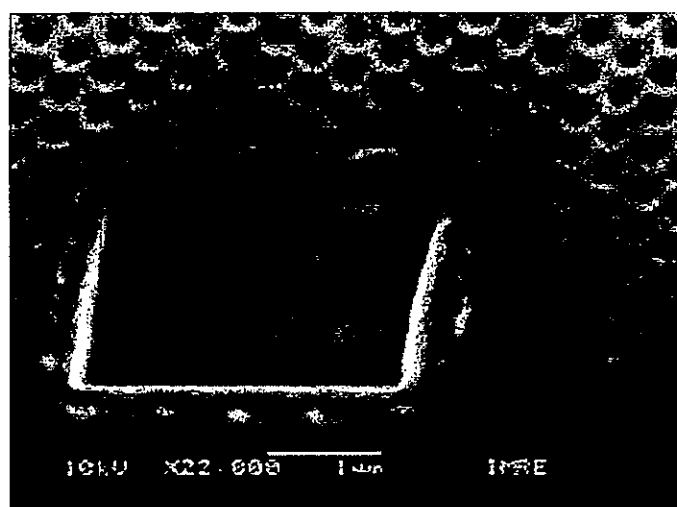


Figure 9

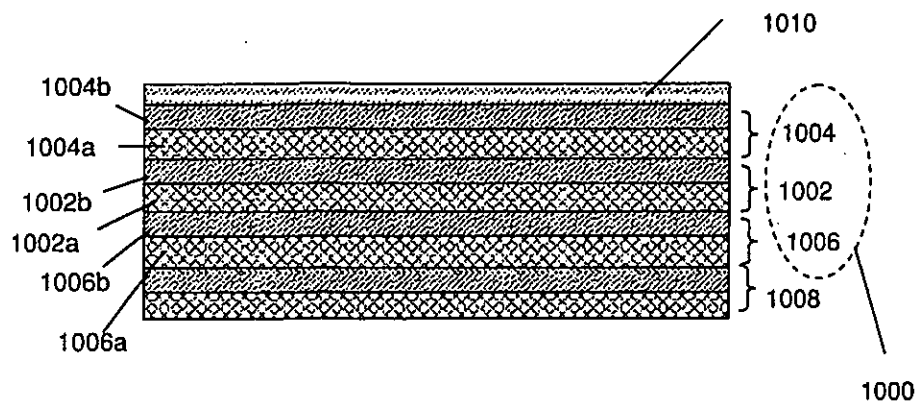


Figure 10A

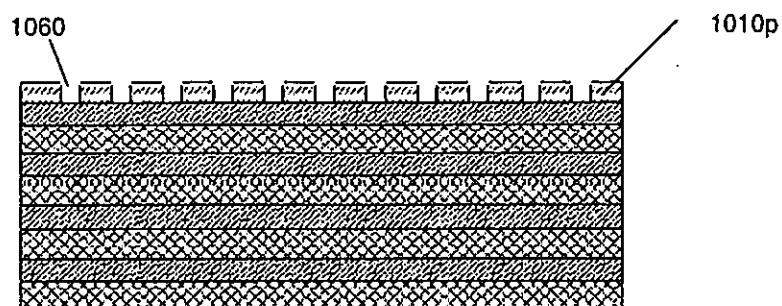


Figure 10B

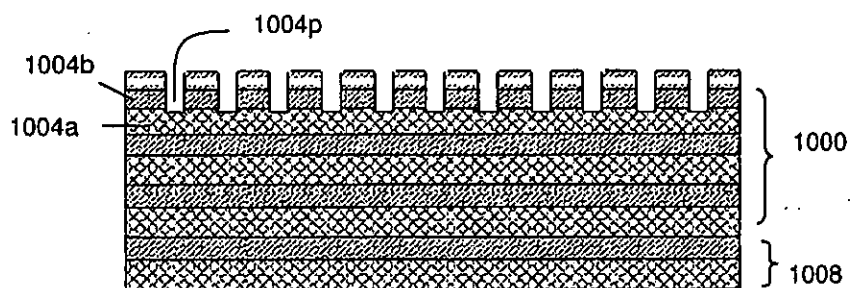


Figure 10C

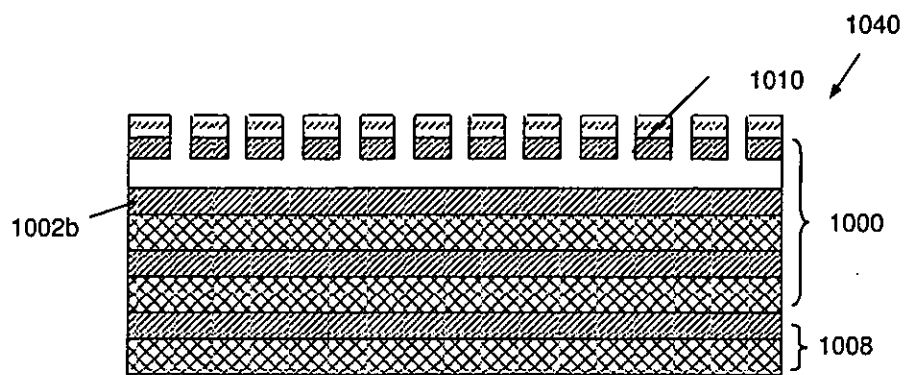


Figure 10D

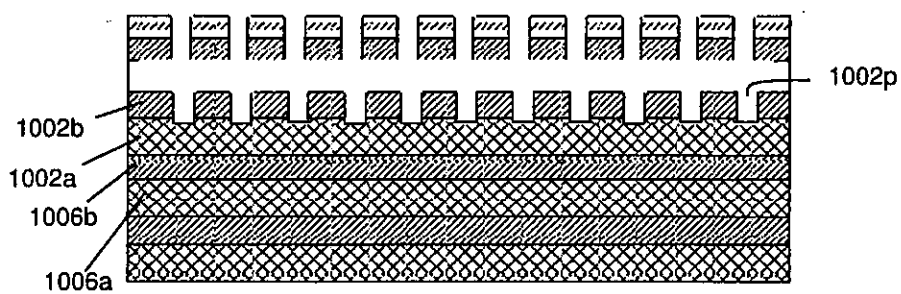


Figure 10E

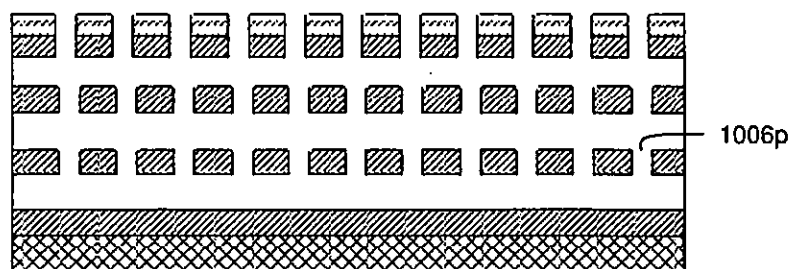


Figure 10F



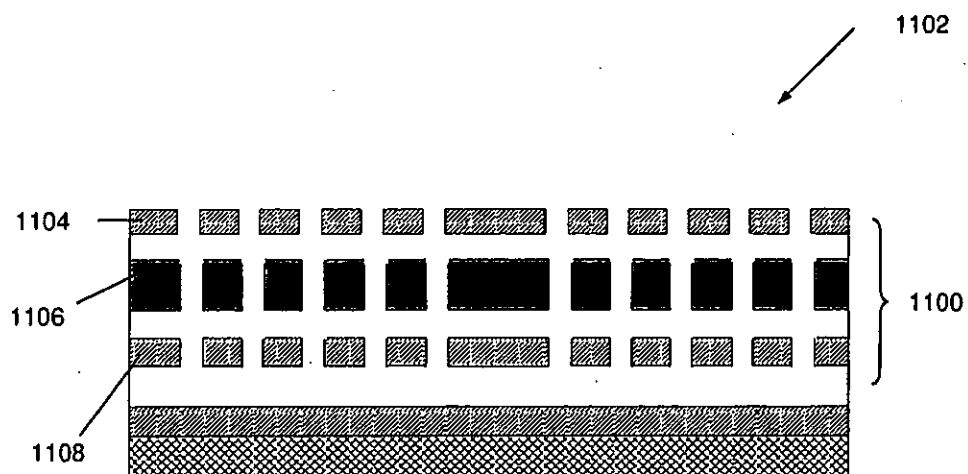


Figure 11

Layers	Thickness	Description
InGaAsP	160nm	7 pairs of InGaAsP/InP
InP	240 nm	
InGaAsP	100nm	
InP buffer	100 nm	
InP substrate		

Figure 12