System and Method for Protecting and Integrating Silicon Intellectual Property (IP) in an Integrated Circuit (IC)

ABSTRACT OF THE DISCLOSURE

System and method for integrated circuit (IC) design using silicon intellectual property (IP) libraries that permits the protecting of the designs of circuits in the silicon IP while allowing correctness verification of the IC design. A preferred embodiment comprises a phantom cell (for example, phantom cell 505) that contains circuit elements (for example, circuit element EL-A 510) connected to each input/output pin of the phantom cell. The inclusion of the circuit elements permits an engineering design tool to check for improperly connected wiring.

FIG. 8