signal vsync2 may be lower than a frequency of the synchronization signal vsync1. A time length of a porch interval pt1 of the synchronization signal vsync2 may be longer than a time length of a porch interval of the synchronization signal vsync1. That is, a time length of the porch interval pt1 of the synchronization signal vsync2 may be longer than a time length of the porch interval pt0 of the synchronization signal vsync2 in the period p0. A time length of a display interval dt1 of the synchronization signal vsync2 may be identical to a time length of a display interval of the synchronization signal vsync1. That is, a time length of the display interval dt1 of the synchronization signal vsync2 may be identical to a time length of the display interval dt0 of the synchronization signal vsync2 in the period p0.

[0089] In the period p1, a sum of the time length of the porch interval pt1 and the time length of the display interval dt1 may be longer than a sum of the time length of the porch interval pt0 and the time length of the display interval dt0. That is, a frame rate in the period p1 may be lower than the frame rate in the period p0. For example, in the period p1, the frame rate may be 48 Hz.

[0090] In the period p1, the power controller 180 may output the signals sc0 and sc1 depending on a logical value of the synchronization signal vsync2. The synchronization signal vsync2 may have a value of logic “1” in the display interval dt1. Accordingly, the power controller 180 may output the signals sc0 and sc1 having a value of logic “1” in the display interval dt1. The scan driver 141 and the source driver 150 may be turned on based on the signals sc0 and sc1 in the display interval dt1. The synchronization signal vsync2 may have a value of logic “0” in the porch interval pt1. Accordingly, the power controller 180 may output the signals sc0 and sc1 having a value of logic “0” in the porch interval pt1. The scan driver 141 and the source driver 150 may be turned off based on the signals sc0 and sc1 in the porch interval pt1.

What is Claimed is:

1. A display driver circuit comprising:

a source driver configured to output display data to data lines;

a controller configured to control the source driver, based on a synchronization signal; and

a frequency adjusting circuit configured to:

extend a first time interval of the synchronization signal from a first length to a second length, such that time interval in which the display data is not output to the data lines is extended, when second image data are not received from an external device during a reference time interval after first image data are received from the external device; and

shorten the first time interval, from the second length to a third length, when an instruction is received from the external device after the first time interval is extended to the second length,

wherein the frequency adjusting circuit is further configured to:

output the synchronization signal at a second time interval after the first time interval; and

maintain the second time interval such that time interval at which the display data is output to the data lines is maintained.

2. The display driver circuit of claim 1, wherein the frequency adjusting circuit is further configured to shorten the first time interval of the synchronization signal, from the second length to the third length, before the second image data are received based on the instruction.

3. The display driver circuit of claim 1 or claim 2, wherein the third length is identical to the first length.

4. The display driver circuit of any one of claims 1 to 3, wherein the frequency adjusting circuit is further configured to receive the instruction, and wherein the instruction is generated based on touch event of a touch panel.

5. The display driver circuit of any one of claims 1 to 4, wherein the frequency adjusting circuit is further configured to shorten the first time interval from the second length to the third length based on the instruction before the second image data are received from the external device.

6. The display driver circuit of any one of claims 1 to 5, wherein the frequency adjusting circuit is further configured to:

extend the first time interval from the first length to the second length by a first fixed length; and

shorten the first time interval from the second length to the third length by a second fixed length.

7. A display driver circuit comprising:

a source driver configured to output display data to data lines connected to pixels;

a controller configured to control the source driver, based on a synchronization signal;

a power controller configured to turn off the source driver during a first time interval, based on the synchronization signal; and

a frequency adjusting circuit configured to:

increase a period of the synchronization signal, from a first value to a second value, such that the first time interval is extended, when second image data are not received from an external device during a reference time interval after first image data are received from the external device; and

reduce the period of the synchronization signal, from the second value to a third value, when the second image data are received from the external device,

wherein the power controller is further configured to turn on the source driver during a second time interval, based on the synchronization signal, and

the frequency adjusting circuit is further configured to maintain the second time interval.

8. The display driver circuit of claim 7, wherein, when the source driver is turned off, a power that is supplied to the source driver is shut off.

9. The display driver circuit of claim 7 or claim 8, wherein the source driver is further configured to not output the display data in the first time interval and output the display data in the second time interval.

10. The display driver circuit of any one of claims 7 to 9, further comprising a scan driver configured to drive scan lines connected to the pixels,

wherein the power controller is further configured to turn off the scan driver during the first time interval, based on the synchronization signal.

11. The display driver circuit of any one of claims 7 to 10, wherein the frequency adjusting circuit is further configured to generate an emission signal such that a period of emission of a light from each of the pixels is maintained regardless of the period of the synchronization signal.

12. The display driver circuit of claim 11, wherein the period of the emission is associated with a quality of an image that is displayed in a display panel, based on the display data.

13. A display driver circuit comprising:

a source driver configured to output display data to data lines;

a controller configured to control the source driver, based on a synchronization signal; and

a frequency adjusting circuit configured to:

lower a frequency of the synchronization signal, from a first value to a second value, such that time interval in which the display data are not output is extended, when second image data are not received from an external device during a reference time interval after first image data are received from the external device;

increase the frequency of the synchronization signal, from the second value to a third value, when the second image data are received from the external device; and

adjust the frequency of the synchronization signal, such that time interval in which the display data are output is maintained.

14. The display driver circuit of claim 13, wherein the frequency adjusting circuit comprises:

a counter configured to count the time interval that the second image data are not received after the first image data are received from the external device;

a comparator configured to compare the time interval with the reference time interval; and

a frequency controller configured to adjust the frequency of the synchronization signal, based on a comparison result in the comparator.

15. The display driver circuit of claim 13 or claim 14, wherein the third value is identical to the first value.

16. The display driver circuit of any one of claims 13 to 15, wherein the frequency adjusting circuit is further configured to output a touch signal to a touch circuit at a frequency higher than the second value.

17. The display driver circuit of claim 16, wherein the frequency adjusting circuit is further configured to increase the frequency of the synchronization signal, from the second value to the third value, when an instruction received from the touch circuit, and

wherein the instruction is generated based on touch event of a touch panel.