What is claimed is:

1. A memory device comprising:

an address buffer configured to store a plurality of bits of a received address;

a first non-volatile memory configured to store a plurality of bits of a failed address;

a plurality of first logic circuits, which are each configured to compare one bit of the received address stored in the address buffer with a corresponding bit of the failed address stored in the first non-volatile memory;

a first selector configured to output a selected one of two output values from two of the first logic circuits, among the first logic circuits, in response to a selection signal;

a second logic circuit configured to output an address matching signal based on the selected output value, and output values of remaining first logic circuits, except for the two of the first logic circuits;

a second non-volatile memory configured to store an address bit value corresponding to the selection signal;

a second selector configured to output one bit of address bits, corresponding to the two of the first logic circuits, in response to a true or inverted version of the selection signal; and

a third logic circuit configured to perform an AND operation on the address matching signal and an output value of the second selector.

2. The memory device according to claim 1, wherein the received address is a row address or a column address.

3. The memory device according to claim 1 or claim 2, wherein each of the first logic circuits is configured to perform an XNOR operation; and wherein the second logic circuit performs an AND operation.

4. The memory device according to claim 1 or claim 2, wherein each of the first logic circuits is configured to perform an XOR operation; and wherein the

second logic circuit performs a NAND operation.

5. The memory device according to claim 1, wherein the received address is a 16-bit row address; and wherein each of the first selector and the second selector receives a first address bit and a sixteenth address bit, among the address bits of the row address.

6. The memory device according to claim 5, wherein the second non-volatile memory stores a bit value of the sixteenth address bit.

7. The memory device according to claim 5 or claim 6, wherein each of the first non-volatile memory and the second non-volatile memory comprises at least one fuse.

8. The memory device according to any one of claims 5 to 7, wherein the first non-volatile memory stores mapping information about a logical address and a physical address that corresponds to the logical address; and wherein a bit type of addresses and the number of addresses, corresponding to the mapping information, are variable.

9. A memory device, comprising:

a memory cell array having a redundancy area corresponding to redundancy word lines and/or redundancy bit lines, and a normal area corresponding to word lines and bit lines;

a row decoder configured to activate at least one of the word lines and/or activate at least one of the redundancy word lines, in response to a row address;

a column decoder configured to activate at least one of the bit lines and/or activate at least one of the redundancy bit lines, in response to a column address; and

a repair control circuit configured to compare the row address with a stored failed row address, to compare the column address with a stored failed column address, to control the row decoder to activate the at least one of the redundancy word lines when the row address corresponds to the failed row address, and to

control the column decoder to activate the at least one of the redundancy bit lines when the column address corresponds to the failed column address; and

wherein the repair control circuit is further configured to vary a repair unit according to an address input during a repair operation, and

wherein the repair control circuit comprises: an address comparator including a plurality of logic circuits configured to compare the row address with the failed row address, and/or compare the column address with the failed column address, and comprising a selector configured to select one output value of at least two logic circuits among the plurality of logic circuits in response to a selection signal.

10. The memory device according to claim 9, wherein the repair unit comprises a type of address bits or the number of address bits.

11. The memory device according to claim 9 or claim 10, wherein the repair control circuit further comprises:

a failed address reservoir configured to store the failed row address and/or the failed column address; and

a repair unit determiner configured to determine the repair unit corresponding to the address input.

12. The memory device according to claim 11, wherein the failed address reservoir comprises a first non-volatile memory storing a plurality of address bits corresponding to a failed address.

13. The memory device according to claim 12, wherein the repair unit determiner comprises:

a second non-volatile memory configured to store at least one address bit ignored in the repair operation, among the plurality of address bits, and output the selection signal; and

an inverter configured to invert the selection signal.

14. The memory device according to claim 13, wherein the address

comparator further comprises:

the plurality of logic circuits that are each configured to receive one address bit of the input address bits and an address bit stored in the first non-volatile memory corresponding to the one address bit, and to perform an XNOR operation on the one address bit and the stored address bit; and

a logic circuit configured to output an address matching signal by performing a logical AND operation on the output value of the selector and output values of remaining logic circuits except the at least two logic circuits of the plurality of logic circuits.

15. The memory device according to claim 13, wherein the address comparator further comprises:

the plurality of logic circuits that are each configured to receive one address bit of the input address bits and an address bit stored in the first non-volatile memory corresponding to the one address bit, and to perform an XOR operation on the one address bit and the stored address bit; and

a logic circuit configured to output an address matching signal by performing a logical NAND operation on the output value of the selector and output values of remaining logic circuits except the at least two logic circuits of the plurality of logic circuits.

16. The memory device according to claim 14 or claim 15, wherein the redundancy word lines and/or the redundancy bit lines are activated, in response to the address matching signal of the address comparator and the inverted selection signal of the repair unit determiner.

17. A repair method of a memory device, comprising:

receiving an address;

determining a repair unit using at least one address bit to be ignored in a repair operation, among address bits of the received address;

comparing the received address with a stored failed address using a plurality of logic circuits; and

when the received address corresponds to the stored failed address,

accessing a redundancy cell array with the repair unit in response to the address,

wherein the repair method further comprises: selecting one output value among output values of the plurality of logic circuits corresponding to the at least one address bit in response to a selection signal.

18. The repair method according to claim 17, further comprising storing mapping information about a logical address and a physical address, corresponding to the address in a test operation, in a non-volatile memory.

19. The repair method according to claim 17 or claim 18, wherein the determining the repair unit comprises determining a type of address bits and the number of address bits in the repair operation.

20. The repair method according to any one of claims 17 to 19, further comprising:

storing repair mapping information about redundancy cells; and

repairing normal cells with the redundancy cells using the repair mapping information; and

wherein a memory cell area corresponding to the repair mapping information is variable.