

Description

This invention relates to circuitry for reducing frequency instability in a digital phase locked loop that is controlled by a clock signal which may be unstable.

A digital phase locked loop (PLL) includes a variable digital oscillator which generates oscillatory signals that may be locked in frequency and phase to a reference signal. The frequency and phase of the signal produced by the digital PLL may depend on the frequency of the clock signal applied to the digital oscillator as well as on the frequency and phase of the reference signal.

For example, consider the digital phase locked loop used to regenerate the chrominance subcarrier signal in a line-locked digital television receiver. An exemplary system of this type is described in U.S. Patent No. 4,349,833 entitled "Apparatus For Digital Demodulation or Modulation of Television Chrominance Signals". Briefly, the system includes a discrete time oscillator (DTO) for regenerating a digital chrominance subcarrier signal locked in phase to the color reference burst component of the composite video signal. The oscillator has three components, an adder, an accumulator register and a read only memory (ROM). The value held by the accumulator register is incremented by an input signal (I_n) coincident with the leading edge of each pulse of the clock signal (CK). The output values of the accumulator register are applied as addresses to the ROM, which is programmed to provide a periodic output function, for example, a sine wave, as an output signal in response to the address values provided by the accumulator register. Assuming that $M-1$ is the largest value which may be held in the accumulator register, and that an increment signal (I_n) is applied to the DTO, the frequency of the signal produced by the DTO (f_{DTO}) may be expressed as:

$$f_{DTO} = (I_n/M)f_{CK} \quad (1)$$

When a DTO is used in a digital PLL, the range of values which may be held in the accumulator register (i.e. the modulus of the accumulator) and the frequency of a clock signal, f_{CK} , are assumed to be invariant so that the frequency of the signal provided by the DTO may be changed only by changing the increment value I_n applied to the input terminal of the DTO. In the U.S. Patent No. 4,349,833 referenced above, the input signal applied to the DTO is determined by the detected phase difference between the reconstructed color subcarrier signal produced by the DTO and the color reference burst signal component of the received video signals. This phase difference signal is applied to a low-pass filter, the output signals of

which are used to change the input value to the DTO so that the frequency and phase of the signal provided by the DTO remain locked to the burst signal.

As set forth above, a basic assumption for this type of digital PLL is that the clock frequency is invariant. This assumption may not be valid if the clock signal is generated by a PLL which locks to the horizontal line synchronizing signal components of the input video signals (a line locked PLL) and if the input video signals are derived from a nonstandard source such as a video tape recorder (VTR) or video disc player. The signal provided by a nonstandard source generally has relatively stable color or burst signal components but may have horizontal line synchronizing signal components which vary significantly in frequency from line to line. This variation may be caused by stretching of the tape, defects in the disc, or motor speed variations in either the VTR or disc player. The frequency of the clock signal generated by a line locked PLL will change to track the changes in the frequency of the horizontal line synchronizing signal. The time constant of the PLL which generates the line locked clock signal is generally relatively short, on the order of ten or fifteen horizontal line periods, for example. This relatively short time constant allows the system to track the changing line frequency rapidly, to keep the number of samples per line substantially constant throughout a field or frame. This feature is desirable in television signal processing systems which include field or frame store memories.

However, this tracking feature may cause sufficient variation in the frequency of the clock signal to cause color signal distortion in television systems which use a digital PLL to regenerate the color subcarrier signal.

The color subcarrier frequency for composite video signals is relatively stable since it is generated by a crystal controlled oscillator either at the transmitter or in the VTR or disc player. The color information in the video signal is quadrature amplitude modulated with respect to this color subcarrier frequency. To demodulate this signal, it is desirable for the regenerated subcarrier signal developed by the PLL to closely match the original subcarrier signal in frequency and phase. Since the color subcarrier signal is suppressed in a standard composite video signal, the PLL which regenerates the color subcarrier signal locks to the color reference burst components of the video signals. These components occur only during a small portion of each horizontal line. Consequently, it is desirable for the color subcarrier PLL to accumulate phase errors over a relatively large number of horizontal line periods to ensure that any measured phase error is accurate and uncontaminated by noise in

the video signal. Thus, the color subcarrier PLL preferably has a much longer time constant than the line locked PLL which generates the system clock signal. This time constant may be on the order of one frame period, for example.

Because of the difference in the loop time constants and because the frequency of the signal produced by the digital color subcarrier PLL depends on the frequency of the clock signal, the combination of the two PLL's may cause instabilities in the regenerated color subcarrier signal. This instability may even cause the color subcarrier PLL to lock at the wrong frequency.

In consideration of the above, the present invention provides phase locked loop stabilization circuitry for use with: a source of a sampling clock signal which exhibits frequency instabilities; and a first digital phase locked loop, clocked by said clock signal, for developing an output signal which has substantially the same frequency as a first reference signal, wherein the frequency instabilities of said clock signal tend to cause frequency instabilities in said output signal; characterized by a second digital phase locked loop, clocked by said clock signal, for developing an oscillatory signal which has substantially the same frequency as a second reference signal having a predetermined frequency, including circuitry for driving a control signal from the phase error signal developed in the second digital phase locked loop, said control signal substantially compensating said second digital phase locked loop for frequency instabilities in said clock signal and causing said oscillatory signal to be substantially independent of the frequency instabilities in said clock signal; and means, coupled to said second digital phase locked loop, with the phase error signal developed in the first digital phase locked loop to stabilize the frequency of said output signal.

In a further aspect, the invention provides a digital television signal processing system comprising an input terminal for applying composite video signal, including horizontal line synchronizing signal components and chrominance signal components including a color reference burst signal component; a horizontal line phase locked loop responsive to said composite video signals and having a predetermined loop time constant for generating a sampling clock signal that is locked in phase to said horizontal line synchronizing signal components, wherein said sampling clock signal may exhibit frequency instabilities; a first digital phase locked loop, clocked by said clock signal, responsive to said composite video signals and having a loop time constant that is substantially greater than that of the horizontal line phase locked loop for developing an output signal that has substantially the same frequency as the color reference burst

signal component of said composite video signals, wherein said output signal tends to exhibit frequency instabilities corresponding to frequency instabilities in said clock signal; characterized by phase locked loop stabilization circuitry comprising means for developing a reference signal having a predetermined frequency; a second digital phase locked loop, clocked by said clock signal, responsive to said reference signal and having a loop time constant that is not substantially greater than that of said horizontal line phase locked loop, for developing an oscillatory signal that is locked in frequency to said reference signal, wherein said second digital phase locked loop includes circuitry for driving a control signal from the phase error signal developed in the second digital phase locked loop; and means coupled to said second phase locked loop for combining the control signal developed by said second digital phase locked loop with the phase error signal developed in the first digital phase locked loop to substantially compensate said first digital phase locked loop for frequency instabilities in said output signal related to said clock signal.

The invention will now be described with reference to the accompanying drawings, in which:

FIGURE 1A is a block diagram of a discrete time oscillator and FIGURES 1B and 1C are waveform diagrams useful in explaining the operation of a discrete time oscillator.

FIGURE 2 is a block diagram of a portion of a digital television receiver.

FIGURE 3 is a block diagram of circuitry embodying the present invention which may be used with the portion of the television receiver shown in FIGURE 2.

FIGURE 4 is a block diagram showing the structure of exemplary low-pass filters for use in FIGURES 2 and 3.

In the drawings, broad arrows represent busses for multiple-bit parallel digital signals and line arrows represent connections carrying analog signals or single bit digital signals. Depending on the processing speed of the devices, compensating delays may be required in certain of the signal paths. One skilled in the art of digital circuit design would know where such delays would be needed in a particular system.

FIGURE 1A illustrates a discrete time oscillator (DTO) of the type described above, comprising an adder 10, an accumulator register 20, and a read only memory (ROM) 30. The adder 10 is responsive to an input signal (In) and to the output value (V) of the accumulator register 20, and supplies the sum thereof to the input of the accumulator register 20. The value held by the accumulator register 20 is incremented by the input signal coincident with the leading edge of each pulse of the clock signal

CJ. The output values of the accumulator register 20 are applied as addresses to ROM 30, which is programmed to provide a periodic output function (e.g., a sine wave) as an output signal (Out) in response to the address values provided by the accumulator register.

The frequency (f_{DTO}) of the signal produced by the DTO may be expressed, per previous explanation, as:

$$f_{\text{DTO}} = (I_n/M) f_{\text{CK}}$$

Examples of the signals "V" and "Out" developed by the DTO when $I_n/M = \frac{1}{2}$ are shown in FIGURES 1B and 1C, respectively. The points on the sinusoidal waveform shown in FIGURE 1C represent the output values provided by the ROM 30 in response to the addresses "V" (shown in FIGURE 1B) developed in the accumulator register 20.

FIGURE 2 is a block diagram of a portion of a television signal processing system which includes first and second PLL's 200 and 250 respectively. The PLL 200 develops a sampling clock signal, CK, which is phase locked to the horizontal line synchronizing signal components of the incoming video signal. The PLL 250 is a digital PLL, clocked by the sampling clock signal CK, which develops digital signals representing the color subcarrier signal at a predetermined phase and a signal that is quadrature phase related to this signal. These two signals are used to synchronously demodulate the chrominance signal components of the incoming video signals to develop two quadrature phase related color difference signals.

In FIGURE 2, a source of composite video signals 210, which may, for example, include the tuner, IF amplifier, video detector and analog to digital converter of a conventional digital television receiver, provides digitized composite video signals to sync separator circuitry 212. The circuitry 212, for example, develops a signal, HSYNC, representing the horizontal line synchronizing signal component of the composite video signals. The signal HSYNC is applied to one input terminal of a phase comparator 214. An internally generated horizontal line synchronizing signal, HS, is applied to a second input terminal of the phase comparator 214. The circuitry which develops the signal HS is described below. Phase comparator 214 may, for example, be similar to the circuitry described in U.S. Patent No. 4,506,175 entitled "Digital Phase Comparator Circuit Producing Sign and Magnitude Outputs". The signal provided by the phase comparator 214 may be, for example, the time delay between the leading edges of the respective pulse signals HSYNC and HS. This signal has positive values when the leading edges of the HSYNC pulses occur before the leading edges of the HS

pulses and negative values when the leading edges of the HSYNC pulses occur after the leading edges of the HS pulses.

The signal provided by the phase comparator circuitry 214 is applied to a low-pass filter 216. Filter 216 is the loop filter of the PLL 200. An exemplary structure for this filter is shown in FIGURE 4. In FIGURE 4, input signals are applied to a scaling circuit 410 which multiplies the input values by a scale factor K_p . The digital signals developed by the scaling circuit 410 are applied to one input port of an adder 450. The input signals to the filter are also applied to one input port of an adder 420 which, with the delay element 430, forms an integrator. The output port of the adder 420 is connected to the input port of the delay element 430, the output port of which is connected to the second input port of the adder 420. Delay element 430 may be, for example, a synchronous latch that is clocked by a signal CLK (e.g., the horizontal line synchronizing signal HS) to provide a sample delay interval of one period of the signal CLK. The signal provided by the delay element 430 is the integrated input signal (i.e. the integrated phase difference between HSYNC and HS). This signal is applied to a scaling circuit 440 which multiplies the integrated signal by a factor K_i . The output signal of the scaling circuit 440 is applied to the second input port of the adder 450. The signal developed by the adder 450 is the output signal of the low-pass filter. The low-pass filter shown in FIGURE 4 is a digital embodiment of a conventional proportional plus integral control network where the factors K_p and K_i correspond to the proportional gain and the integral gain of the network respectively. The values of the factors K_p and K_i depend on the desired time constant and damping factor of the PLL and upon the gains of the other elements in the loop. Filters of this type are commonly used as loop filters in PLL's.

Referring to FIGURE 2, the low-pass filtered phase difference signals provided by the filter 216 are applied to a digital to analog converter (DAC) 218. DAC 218 develops analog potential values representing the filtered phase difference signals and applies these values at a horizontal line rate to a voltage controlled oscillator (VCO) 220. The VCO 220, which may be of conventional design, produces sampling clock signal. VCO 220 is tuned to have a free running frequency of R times f_H . In the present embodiment, R is the ordinal number of a harmonic of the horizontal line frequency, f_H , which approximates a multiple of the color subcarrier frequency. For example, in the NTSC system, the frequency, f_{SC} , of the color subcarrier signal is the 455th harmonic of one-half of the horizontal line frequency, and the frequency, f_{CK} , of the sampling clock signal is four times the frequency of the color

subcarrier signal $4 f_{sc}$. So the VCO used in this embodiment has a free-running frequency of approximately 910 times the horizontal line frequency ($R = 910$).

The sinusoidal output signal of the VCO is applied to Schmitt trigger circuitry 221 which develops a square wave clock signal CK having a frequency, f_{CK} , equal to Rf_H . The signal CK is applied to frequency dividing circuitry 222. Circuitry 222 divides the frequency of the signal CK by R to develop a signal HS having a frequency substantially equal to f_H . As set forth above, the signal HS is applied to the second input terminal of the phase comparator 214.

The circuitry 222 may, for example, include a 10-bit counter (not shown) which is configured to be reset when a count value of 910 is achieved. The frequency dividing circuitry 222 may further include circuit elements (not shown) coupled to the counter to detect count values corresponding to the beginning and end of the burst interval and for generating a burst gate signal, BG, which spans the time interval defined by those count values in each horizontal line period.

The PLL 200 generates a clock signal, CK, which tracks the varying line frequency of a non-standard signal to provide a substantially uniform number of sampling clock pulses per line. In the present embodiment, the gain factors of the phase comparator 214, low-pass filter 216, DAC 218, VCO 220, Schmitt trigger 221 and frequency divider circuitry 222 are selected to achieve a filter time constant of approximately 15 horizontal line periods and a damping factor of 2. These gain values depend on the circuit elements to be used in the PLL and may be readily calculated by one skilled in the art of phase-locked loop design. An explanation of the relationship between the gain values, the damping factor and the PLL time constant may be found in Gruen, W.J. "Theory of AFC Synchronization" Proceedings of the IRE, August 1953, pp. 1043-1048.

Composite video signals from source 210 are also applied to Y/C separation filter circuitry 230. Circuitry 230 may include, for example, a low-pass filter and a band-pass filter for separating the respective luminance and chrominance signal components from the composite video signals. The luminance and chrominance signals are available at the output busses YB and CB of the circuitry 230 respectively.

The separated chrominance components are applied to multipliers 232 and 234 which, using signals provided by the PLL 250, demodulate the chrominance signals into two quadrature phase related baseband color difference signals, for example, I and Q.

The color difference signals are applied to a phase error detector 236. The phase error detector 236 develops an output signal representing the difference between the phase of the demodulated color reference burst signal and a reference phase value. The phase error detector 236 may include, for example, circuitry (not shown) to separately accumulate baseband I and Q sample values during the burst interval and to divide the accumulated I values by the accumulated Q values to develop values representing the phase of the burst signal relative to the sampling instants of the I and Q samples. These values may be subtracted from a reference value representing the desired burst phase to generate a phase error value to control the PLL 250. The phase error values developed by the detector 236 are applied to a low-pass filter 238. Filter 238 is clocked by the signal HS generated by the PLL 200 and may be similar to the filter 216 except for the values of the proportional and integral gain factors, K_p and K_i respectively. The filtered phase error signal, A, provided by the filter 238 is applied to one input port of an adder 240. A fixed increment value, K_1 , supplied by a source 242, is applied to the other input port of the adder 240. The signal, B, developed by the adder 240 is applied as the input increment value to a DTO 252 which includes an adder 244, an accumulator register 246 and a ROM 248 that is programmed to provide, at respective first and second output ports, the cosine and sine of the values applied to its address input port, normalized to 2π radians. These signals, which in the present embodiment are the cosine and sine of $2\pi f_{sc}t$ respectively, are applied to the respective multipliers 232 and 234, as set forth above, to synchronously demodulate the chrominance signal to recover the two quadrature phase related color difference signals.

In the steady state, when there is no difference between the phase value of the demodulated burst signal and the reference phase value, the frequency of the signal developed by the DTO is determined by the number of bits in the accumulator register 246, the increment value K_1 supplied by the source 242, and by the frequency of the clock signal CK. Assuming that the register 246 is an twenty-bit register and that the frequency of the clock signal CK is equal to $4f_{sc}$, a K_1 equal to 262,144 (i.e. 2^{18}) produces an output signal having a frequency of f_{sc} . In dynamic operation, when the burst phase does not match the reference phase, the phase error values provided by the detector 236 are accumulated by the low-pass filter 238 to develop a correction term which is added to the value K_1 by the adder 240 to change the frequency of the DTO in a sense that tends to reduce the phase error.

As set forth above, it is desirable for the time constant of the PLL 250 to be relatively long to reduce the effects of noise and to provide a high level of phase accuracy for the signals applied to the synchronous demodulating multipliers 232 and 234. In the present embodiment, for example, the gain factors of the various circuit elements in the PLL are set to values which produce a loop time constant of approximately one frame period (1/30th of a second for NTSC signals). Since the time constant of the PLL 250 is much longer than the time constant of the PLL 200, the PLL 250 may not be able to track frequency changes in the regenerated subcarrier signal that are induced by changes in the frequency of the clock signal, CK. This deficiency in the system shown in FIGURE 2 may cause random errors in the I and Q color difference signals or may cause the PLL 250 to generate a color subcarrier signal having the wrong frequency, locked to the wrong harmonic of the line frequency.

To understand this problem more completely, consider the PLL correction signals A and B. When the signals applied to the television receiver are from standard sources (e.g. broadcast signals) and the PLL 250 is locked to the color reference burst signal, the clock signal CK and regenerated subcarrier signal developed by the DTO are at their nominal frequencies, $f_{ck\ nom}$ and $f_{sc\ nom}$ respectively. Accordingly, the equation (1) may be restated as

$$In/M = f_{sc\ nom}/f_{ck\ nom} \quad (2)$$

In relation to FIGURE 2, the input increment signal, In, corresponds to the correction signal B. When the PLL 250 is locked to burst, the signal A is zero valued. In this instance, the input increment signal, B, applied to the DTO 252 is the value K_1 . Consequently,

$$B = K_1 = M f_{sc\ nom}/f_{ck\ nom} \quad (3)$$

In the non-locked condition, the frequency of the signal provided by the DTO 252 differs from $f_{sc\ nom}$ by some value Δf_{sc} and the signal A is non-zero. In this instance, the equation (3) becomes:

$$B = A + K_1 = M(f_{sc\ nom} + \Delta f_{sc})/f_{ck\ nom} \quad (4)$$

from which it may be deduced that:

$$A = M \Delta f_{sc}/f_{ck\ nom} \quad (5)$$

B is the input increment signal to the DTO. Substituting the equation (4) in the equation (1) yields:

$$f_{DTO\ 252} = (f_{sc\ nom} + \Delta f_{sc})f_{ck}/f_{ck\ nom} \quad (6)$$

Thus, even when the PLL 250 has locked to the

color burst signal and the term Δf_{sc} becomes zero, the frequency of the signal generated by the DTO 252 may change by the factor $f_{ck}/f_{ck\ nom}$, the actual clock frequency divided by the nominal clock frequency.

FIGURE 3 is a block diagram of circuitry which embodies the present invention. This circuitry modifies the signal B to develop a signal B' which is an input increment signal that allows the signal generated by the DTO to be substantially independent of changes in f_{ck} .

The circuitry includes an oscillator 310 which develops a sinusoidal output signal having a frequency f_{xtl} determined by the resonant crystal 312. The frequency of the signal generated by the oscillator may be fine tuned via the optional adjustment 330 (shown in phantom), the function of which is described below. The output signal of the oscillator is applied to an analog-to-digital converter (ADC) 314. ADC 314, which may, for example be a four-bit flash ADC, samples the sinusoidal signal at instants determined by the clock signal CK to develop digital signals for application to a phase detector 316. In addition to the phase detector 316, the PLL 300 also includes a low-pass filter 318, adder 320, digital value source 322, and a DTO 302 which includes an adder 324, an accumulator register 326 and a ROM 327. This PLL develops, for example, a four-bit digital signal at the output port of the ROM 327 that is locked in frequency and phase to the signal developed by the oscillator 310. The phase detector 316 compares the signal provided by the ROM 327 to the signal provided by the ADC 314. After the PLL 300 has initially locked to the reference signal, the phase difference signal developed by the phase detector 316 represents phase changes induced by the clock signal. This phase difference signal is applied to a low-pass filter 318. Filter 318 is the loop filter of the PLL 300 and may, for example, be of the same design as the filters 216 and 328 described above. The integral and proportional gain factors of the filter 318 are set, along with the gain constants of the other elements in the loop, to provide a loop time constant that is less than or approximately equal to the time constant of the PLL 200 (i.e. fifteen horizontal line periods). The filtered phase difference signal provided by the filter 318 is added to a fixed digital value, K_2 , from a source 322, by the adder 320. The signal provided by the adder 320 is applied as the input increment signal to the DTO 302 as set forth above. The output signal of the DTO 302 is applied to the phase detector 316 to complete the feedback loop.

The following is a more detailed analysis of the operation of the PLL 300. The frequency, f_{xtl} , of the reference signal is substantially constant since it is generated by a crystal controlled oscillator. Con-

sequently, the phase difference signals developed by the phase detector 316 and the phase correction signals developed by the low-pass filter 318 are proportional to the frequency and phase differences in the signal generated by the DTO 302 relative to the signal produced by the crystal oscillator. These frequency and phase differences are induced by the frequency instabilities in the clock signal CK. Thus, when the signals received via source 210 are from standard sources, the output signal C of the low-pass filter 318 is zero valued and the input increment signal to the DTO 302 is the digital value K_2 provided by the source 322. Using analysis similar to that set forth above in reference to the PLL 250, the value K_2 may be described by the equation (7).

$$K_2 = Nf_{xt1}/f_{ck\ nom} \quad (7)$$

where the number N is one greater than the largest number that can be stored in the accumulator register 326.

When the signals received via the source 210 are from non-standard sources, however, the frequency of the clock signal CK may vary from the nominal value $f_{ck\ nom}$ by an amount Δf_{ck} , so the signal C is non-zero. To ensure that the PLL 300 accurately tracks the changing clock frequency, it is desirable that the factor $f_{ck\ nom}$ in the equation (7) be replaced by the factor $(f_{ck\ nom} + \Delta f_{ck})$. This replacement produces the equation:

$$C' = C + K_2 = Nf_{xt1}/(f_{ck\ nom} + \Delta f_{ck}). \quad (8)$$

Multiplying the right-hand side of the equation (8) by $f_{ck\ nom}/f_{ck\ nom}$ yields:

$$C + K_2 = Nf_{xt1}f_{ck\ nom}/(f_{ck\ nom} + \Delta f_{ck})f_{ck\ nom}. \quad (9)$$

Replacing the numerator factor, $f_{ck\ nom}$, in the equation (9) by $f_{ck\ nom} + \Delta f_{ck} - \Delta f_{ck}$ yields:

$$C + K_2 = Nf_{xt1}/f_{ck\ nom} - Nf_{xt1}\Delta f_{ck}/(f_{ck\ nom} + \Delta f_{ck})f_{ck\ nom}. \quad (10)$$

From the equation (10), it can be deduced that

$$C = -Nf_{xt1}\Delta f_{ck}/(f_{ck\ nom} + \Delta f_{ck})f_{ck\ nom}. \quad (11)$$

The equation 11 describes the frequency difference signal provided by the low-pass filter 318 in response to the phase difference signals provided by the phase detector 316.

The signal C' , the sum of C and K_2 , when applied as the input increment signal to the DTO 302 causes the DTO 302 to accurately track the changes in f_{ck} and, maintain the frequency of the signal provided by the DTO 302 substantially equal

to f_{xt1} .

The signal C' is scaled by scaling circuitry 323 by a factor K_S which satisfies the equation (12).

$$K_S = f_{ck\ nom}/(N f_{xt1}) \quad (12)$$

to produce a signal C'' which is described by the equation (13).

$$C'' = f_{ck\ nom}/f_{ck}. \quad (13)$$

The signal B, provided by the adder 240 in FIGURE 2, is multiplied by the signal C'' in the multiplier 328 to develop a signal B' satisfying the equation (14).

$$B' = M(f_{sc\ nom} + \Delta f_{sc})/f_{ck}. \quad (14)$$

When B' is substituted for B as the input increment of the DTO 252, the equation (6) becomes

$$f_{DTO\ 252} = f_{sc\ nom} + \Delta f_{sc}. \quad (15)$$

So the frequency of the signal provided by the PLL 250 is substantially independent of the frequency of the clock signal CK.

In the present embodiment, the frequency f_{xt1} may have any predetermined value within the Nyquist limit of the sampling clock signal CK. It is preferable, however, that the system be designed to operate at a particular frequency since the digital constant factor K_S includes a factor of $1/f_{xt1}$. The frequency f_{xt1} may be set to the predetermined value either by using a very accurate resonant crystal 312 or by using the optional frequency adjustment circuitry 330 in the oscillator 310 and using a less accurate crystal.

Claims

1. Phase locked loop stabilization circuitry for use with:

a source (200) of a sampling clock signal (CK) which exhibits frequency instabilities; and

a first digital phase locked loop (250), clocked by said clock signal, for developing an output signal (from 248) which has substantially the same frequency as a first reference signal, wherein the frequency instabilities of said clock signal tend to cause frequency instabilities in said output signal; characterized by:

a second digital phase locked loop (300), clocked by said clock signal, for developing an oscillatory signal which has substantially the same frequency as a second reference signal having a predetermined frequency, including circuitry (318-322) for deriving a control signal

sequently, the phase difference signals developed by the phase detector 316 and the phase correction signals developed by the low-pass filter 318 are proportional to the frequency and phase differences in the signal generated by the DTO 302 relative to the signal produced by the crystal oscillator. These frequency and phase differences are induced by the frequency instabilities in the clock signal CK. Thus, when the signals received via source 210 are from standard sources, the output signal C of the low-pass filter 318 is zero valued and the input increment signal to the DTO 302 is the digital value K_2 provided by the source 322. Using analysis similar to that set forth above in reference to the PLL 250, the value K_2 may be described by the equation (7).

$$K_2 = Nf_{xt1}/f_{ck\ nom} \quad (7)$$

where the number N is one greater than the largest number that can be stored in the accumulator register 326.

When the signals received via the source 210 are from non-standard sources, however, the frequency of the clock signal CK may vary from the nominal value $f_{ck\ nom}$ by an amount Δf_{ck} , so the signal C is non-zero. To ensure that the PLL 300 accurately tracks the changing clock frequency, it is desirable that the factor $f_{ck\ nom}$ in the equation (7) be replaced by the factor $(f_{ck\ nom} + \Delta f_{ck})$. This replacement produces the equation:

$$C' = C + K_2 = Nf_{xt1}/(f_{ck\ nom} + \Delta f_{ck}). \quad (8)$$

Multiplying the right-hand side of the equation (8) by $f_{ck\ nom}/f_{ck\ nom}$ yields:

$$C + K_2 = Nf_{xt1}f_{ck\ nom}/(f_{ck\ nom} + \Delta f_{ck})f_{ck\ nom}. \quad (9)$$

Replacing the numerator factor, $f_{ck\ nom}$, in the equation (9) by $f_{ck\ nom} + \Delta f_{ck} - \Delta f_{ck}$ yields:

$$C + K_2 = Nf_{xt1}/f_{ck\ nom} - Nf_{xt1}\Delta f_{ck}/(f_{ck\ nom} + \Delta f_{ck})f_{ck\ nom}. \quad (10)$$

From the equation (10), it can be deduced that

$$C = -Nf_{xt1}\Delta f_{ck}/(f_{ck\ nom} + \Delta f_{ck})f_{ck\ nom}. \quad (11)$$

The equation 11 describes the frequency difference signal provided by the low-pass filter 318 in response to the phase difference signals provided by the phase detector 316.

The signal C' , the sum of C and K_2 , when applied as the input increment signal to the DTO 302 causes the DTO 302 to accurately track the changes in f_{ck} and, maintain the frequency of the signal provided by the DTO 302 substantially equal

to f_{xt1} .

The signal C' is scaled by scaling circuitry 323 by a factor K_S which satisfies the equation (12).

$$K_S = f_{ck\ nom}/(N f_{xt1}) \quad (12)$$

to produce a signal C'' which is described by the equation (13).

$$C'' = f_{ck\ nom}/f_{ck}. \quad (13)$$

The signal B, provided by the adder 240 in FIGURE 2, is multiplied by the signal C'' in the multiplier 328 to develop a signal B' satisfying the equation (14).

$$B' = M(f_{sc\ nom} + \Delta f_{sc})/f_{ck}. \quad (14)$$

When B' is substituted for B as the input increment of the DTO 252, the equation (6) becomes

$$f_{DTO\ 252} = f_{sc\ nom} + \Delta f_{sc}. \quad (15)$$

So the frequency of the signal provided by the PLL 250 is substantially independent of the frequency of the clock signal CK.

In the present embodiment, the frequency f_{xt1} may have any predetermined value within the Nyquist limit of the sampling clock signal CK. It is preferable, however, that the system be designed to operate at a particular frequency since the digital constant factor K_S includes a factor of $1/f_{xt1}$. The frequency f_{xt1} may be set to the predetermined value either by using a very accurate resonant crystal 312 or by using the optional frequency adjustment circuitry 330 in the oscillator 310 and using a less accurate crystal.

Claims

1. Phase locked loop stabilization circuitry for use with:

a source (200) of a sampling clock signal (CK) which exhibits frequency instabilities; and

a first digital phase locked loop (250), clocked by said clock signal, for developing an output signal (from 248) which has substantially the same frequency as a first reference signal, wherein the frequency instabilities of said clock signal tend to cause frequency instabilities in said output signal; characterized by:

a second digital phase locked loop (300), clocked by said clock signal, for developing an oscillatory signal which has substantially the same frequency as a second reference signal having a predetermined frequency, including circuitry (318-322) for deriving a control signal



(C') from the phase error signal developed in the second digital phase locked loop, said control signal substantially compensating said second digital phase locked loop for frequency instabilities in said clock signal and causing said oscillatory signal to be substantially independent of the frequency instabilities in said clock signal; and

means (323, 328), coupled to said second digital phase locked loop (300), for combining the control signal (C') developed by said second phase locked loop with the phase error signal developed in the first digital phase locked loop to stabilize the frequency of said output signal.

2. The stabilization circuitry of claim 1 for use with a first digital phase locked loop (250) which includes:

an input terminal for applying said first reference signal;

a first discrete time oscillator (252) responsive to said clock signal (CK) and to a first input increment signal (B) for developing said output signal having substantially the same frequency as said first reference signal;

means, including first phase comparison means (236) for developing a signal representing the difference in phase between said first reference signal and said output signal; and

first summing means (240) coupled to said first phase comparison means for combining the signal developed thereby with a signal (K1) having a predetermined value to develop said input increment signal for application to said discrete time oscillator (252);

further characterized in that:

said means for combining said control signal includes signal modifying means (328) having a first input port coupled to receive the output signal of said first summing means (240), a second input port coupled to receive a second signal (C'') derived from said control signal (C'), and an output port coupled to apply the signal provided by said first summing means as modified by said control signal to said discrete time oscillator (252) as a modified first input increment signal (B').

3. The stabilization circuitry of claim 2 characterized by:

means for developing said second reference signal including:

a crystal oscillator (310) for developing an output signal having a frequency substantially equal to said predetermined frequency; and

an analog to digital converter (314) coupled to said crystal oscillator and to said source

of clock signal (CK) for developing digital samples representing said second reference signal, said samples having values representing the values of the signal provided by said crystal oscillator at instants in time determined by said clock signal; and further characterized in that:

said second digital phase locked loop (300) includes:

a second discrete time oscillator (302) responsive to said clock signal and to a second input increment signal (C') for developing said oscillatory signal having substantially the same frequency as said second reference signal;

means including second phase comparison means (316) coupled to said analog to digital converter (314) and to said second discrete time oscillator (302) for developing a signal representing the difference in phase between said second reference signal and said oscillatory signal; and

second summing means (320) coupled to said second phase comparison means (316) for combining the signal provided thereby with a signal (K2) having a predetermined value to develop a signal (C') for application to said second discrete time oscillator as said second input increment signal and to said signal modifying means as said control signal.

4. The stabilization circuitry as in claim 3 further characterized in that said signal modifying means includes a multiplier (328) responsive to first and second input signals provided by the first and second summing means (240, 320) of said first and second phase locked loops (250, 300) respectively for developing a signal which is proportional to the product of the first and second input signals for application to said first discrete time oscillator as said modified first input increment signal.

5. A digital television signal processing system comprising:

an input terminal for applying (from 210) composite video signal, including horizontal line synchronizing signal components and chrominance signal components including a color reference burst signal component;

a horizontal line phase locked loop (200) responsive to said composite video signals and having a Predetermined loop time constant for generating a sampling clock signal (CK) that is locked in phase to said horizontal line synchronizing signal components, wherein said sampling clock signal may exhibit frequency instabilities;

a first digital phase locked loop (250), clocked by said clock signal, responsive to said



composite video signals and having a loop time constant that is substantially greater than that of the horizontal line phase locked loop for developing an output signal that has substantially the same frequency as the color reference burst signal component of said composite video signals, wherein said output signal tends to exhibit frequency instabilities corresponding to frequency instabilities in said clock signal; characterized by phase locked loop stabilization circuitry comprising:

means (310) for developing a reference signal having a predetermined frequency;

a second digital phase locked loop (300), clocked by said clock signal, responsive to said reference signal and having a loop time constant that is not substantially greater than that of said horizontal line phase locked loop, for developing an oscillatory signal that is locked in frequency to said reference signal, wherein said second digital phase locked loop includes circuitry (318-322) for deriving a control signal (C') from the phase error signal developed in the second digital phase locked loop; and

means (323, 328) coupled to said second phase locked loop for combining the control signal (C') developed by said second digital phase locked loop (300) with the phase error signal developed in the first digital phase locked loop to substantially compensate said first digital phase locked loop for frequency instabilities in said output signal related to said clock signal.

6. The system of claim 5 wherein:

said first digital phase locked loop (250) includes:

a first discrete time oscillator (252) responsive to said clock signal (CK) and to a first input increment signal (B) for developing said output signal having substantially the same frequency as said color reference burst signal;

means including first phase comparison means (236) for developing a signal representing the difference in phase between said color reference burst signal and said output signal; and

first summing means (240) coupled to said phase comparison means for combining the signal provided thereby with a signal having a predetermined value to develop said input increment signal for application to said discrete time oscillator; and characterized in that:

said means (323, 328) for combining said control signal includes signal modifying means (328) for modifying the signal provided by said first summing means in accordance with a

signal (C'') derived from control signal (C') to produce a modified first input increment signal (B').

7. The circuitry set forth in claim 6 wherein:

said means for developing said reference signal includes:

a crystal oscillator (310) for developing an output signal having a frequency substantially equal to said predetermined frequency; and

an analog to digital converter (314) coupled to said crystal oscillator and to said source of clock signals (CK) for developing digital samples representing said reference signal, said samples representing the values of the signal provided by said crystal oscillator at instants in time determined by said clock signal; and wherein

said second digital phase locked loop (300) includes:

a second discrete time oscillator (302) responsive to said clock signal and to a second input increment signal (C') for developing said oscillatory signal having substantially the same frequency as said reference signal;

means including second phase comparison means (316) coupled to said analog to digital converter (314) and to said second discrete time oscillator (302) for developing a signal representing the difference in phase between said second reference signal and said oscillatory signal; and

second summing means (320) coupled to said second phase comparison means (316) for combining the signal provided thereby with a signal (K2) having a predetermined value to develop a signal for application to said second discrete time oscillator as said second input increment signal (C') and to said signal modifying means (328) as said control signal.

8. The apparatus set forth in claim 7 wherein said signal modifying means (328) includes a multiplier responsive to first and second input signals provided by the respective first and second summing means for developing a signal which is proportional to the product of the first and second input signals for application to said first discrete time oscillator as said modified first input increment signal.

Patentansprüche

1. PLL-Stabilisierungsschaltung zur Verwendung mit

- einer Quelle (200) eines Abtast-Taktsignales (CK), welches Frequenz-Instabilitäten aufweist;



- einer ersten Digital-PLL (250), die von dem Taktsignal getaktet wird, zum Bilden eines Ausgangssignales (von 248), welches im wesentlichen dieselbe Frequenz aufweist, wie ein erstes Referenzsignal, wobei die Frequenz-Instabilitäten des Taktsignales dazu neigen, Frequenz-Instabilitäten in dem Ausgangssignal zu bewirken;

gekennzeichnet durch

- eine - von dem Taktsignal getaktete - zweite Digital-PLL (300), zum Bilden eines Schwingungssignales, welches im wesentlichen dieselbe Frequenz wie ein zweites Referenzsignal mit vorbestimmter Frequenz aufweist, welche eine Schaltungsanordnung (318 bis 322) beinhaltet zum Ableiten eines Steuersignales (C') aus dem Phasen-Fehlersignal, welches in der zweiten Digital-PLL gebildet wird, wobei das Steuersignal die zweite Digital-PLL hinsichtlich der Frequenz-Instabilitäten in dem Taktsignal im wesentlichen kompensiert und bewirkt, daß das Schwingungssignal im wesentlichen unabhängig von den Frequenz-Instabilitäten in dem Taktsignal ist;
- Mittel (323, 328), die mit der zweiten Digital-PLL (300) gekoppelt sind, zum Kombinieren des Steuersignales (C'), welches von der zweiten PLL gebildet wird, mit dem Phasen-Fehlersignal, welches in der ersten Digital-PLL gebildet wird, um die Frequenz des Ausgangssignales zu stabilisieren.

2. Stabilisierungsschaltung nach Anspruch 1 zur Verwendung mit einer ersten Digital-PLL (250), welche beinhaltet:

- einen Eingangsanschluß zum Anlegen des ersten Referenzsignales;
- einen ersten zeitdiskreten Oszillator (252), der abhängig von dem Taktsignal (CK) und einem ersten Eingangs-Inkrementalsignal (B) ist, zum Bilden des Ausgangssignales, mit im wesentlichen derselben Frequenz, wie das erste Referenzsignal;
- Mittel, die erste Phasen-Vergleichermittel (236) beinhalten, zum Bilden eines Signals, das repräsentativ für die Differenzphase zwischen dem ersten Referenzsignal und dem Ausgangssignal ist;
- erste Summiermittel (240), die mit den ersten Phasen-Vergleichermitteln gekoppelt sind, zum Kombinieren des Signales, das davon gebildet wird, mit einem Signal (K1), welches einen vorbestimmten

Wert aufweist, um das Eingangs-Inkrementalsignal - zum Anlegen an den zeitdiskreten Oszillator (252) - zu bilden;

dadurch gekennzeichnet,

- daß die Mittel zum Kombinieren des Steuersignales beinhalten: Signal-Modifiziermittel (328), die einen ersten Eingangsport haben, der gekoppelt ist zum Erhalt des Ausgangssignales der ersten Summiermittel (240), einen zweiten Eingangsport, der gekoppelt ist zum Erhalt eines zweiten Signales (C'), welches von dem Steuersignal (C') abgeleitet ist, und einen Ausgangsport, der gekoppelt ist zum Anlegen des Signales
- welches von den ersten Summiermitteln bereitgestellt wird - in der Modifizierung durch das Steuersignal an den zeitdiskreten Oszillator (252), und zwar als modifiziertes erstes Eingangs-Inkrementalsignal (B').

3. Stabilisierungsschaltung nach Anspruch 2, gekennzeichnet durch:

- Mittel zum Bilden des zweiten Referenzsignales, welche beinhalten:
- einen Quarzoszillator (310) zum Bilden eines Ausgangssignales mit einer Frequenz, die im wesentlichen gleich der vorbestimmten Frequenz ist;
- einen Analog/Digital-Umsetzer (314), der mit dem Quarzoszillator und der Quelle des Taktsignales (CK) gekoppelt ist, zum Bilden von Digital-Abtastwerten, welche das zweite Referenzsignal repräsentieren, wobei die Abtastwerte solche Werte haben, welche die Werte des Signales repräsentieren, das von dem Quarzoszillator zu Zeitpunkten zur Verfügung gestellt wird, welche von dem Taktsignal bestimmt werden;
- weiter dadurch gekennzeichnet, daß die zweite Digital-PLL (300) beinhaltet:
- einen zweiten zeitdiskreten Oszillator (302), welcher abhängig von dem Taktsignal und einem zweiten Eingangs-Inkrementalsignal (C') ist, zum Bilden des Schwingungssignales mit im wesentlichen derselben Frequenz, wie das zweite Referenzsignal;
- Mittel, welche zweite Phasen-Vergleichermittel (316) aufweisen, die mit dem Analog/Digital-Umsetzer (314) und dem zweiten zeitdiskreten Oszillator (302) gekoppelt sind, zum Bilden eines Signales, das die Phasendifferenz zwischen dem zweiten Referenzsignal und dem Schwingungssignal repräsentiert;



- zweite Summiermittel (320), welche mit den zweiten Phasen-Vergleichermitteln (316) gekoppelt sind, zum Kombinieren des Signales, das davon erzeugt wird, mit einem Signal (K2), welches einen vorgegebenen Wert hat, um ein Signal (C') zu bilden zum Anlegen an den zweiten zeitdiskreten Oszillator als zweites Eingangs-Inkrementalsignal und an die Signal-Modifiziermittel als Steuersignal. 10
4. Stabilisierungsschaltung nach Anspruch 3, dadurch gekennzeichnet,
- daß die Signal-Modifiziermittel einen Multiplizierer (328) beinhalten, der abhängig von ersten und zweiten Eingangssignalen ist, die von den ersten und zweiten Summiermitteln (240, 320) der ersten bzw. zweiten PLL (250, 300) erzeugt werden, zum Bilden eines Signales, welches proportional zu dem Produkt der ersten und zweiten Eingangssignale ist, zum Anlegen an den ersten zeitdiskreten Oszillator als modifiziertes erstes Eingangs-Inkrementalsignal. 25
5. Digital-Fernsehsignal-Verarbeitungssystem
- mit einem Eingangsanschluß zum Anlegen (von 210) eines Video-Signalgemisches, welches Horizontal-Zeilensynchron-Signalkomponenten aufweist und Chrominanz-Signalkomponenten, welche ein Farb-Referenzburst-Signalkomponente beinhalten; 30
 - mit einer Horizontal-Zeilen-PLL (200), die abhängig von dem Video-Signalgemisch ist und eine vorbestimmte Schleifen-Zeitkonstante hat, zum Erzeugen eines Abtast-Taktsignales (CK), welches phasenstarr mit den Horizontal-Zeilensynchron-Signalkomponenten verriegelt ist (locked), wobei das Abtast-Taktsignal Frequenz-Instabilitäten aufweisen kann; 40
 - mit einer - von dem ersten Taktsignal getakteten - Digital-PLL (250), die abhängig von dem Video-Signalgemisch ist und eine Schleifen-Zeitkonstante aufweist, die wesentlich größer ist als diejenige der Horizontal-Zeilen-PLL, zum Bilden eines Ausgangssignales, welches im wesentlichen dieselbe Frequenz aufweist, wie die Farb-Referenzburst-Signalkomponente des Video-Signalgemisches, wobei das Ausgangssignal dazu neigt, Frequenz-Instabilitäten entsprechend den Frequenz-Instabilitäten des Taktsignales aufzuweisen; 55
- gekennzeichnet durch eine PLL-Stabilisierungsschaltung
- mit Mitteln (310) zum Bilden eines Referenzsignales, welches eine vorbestimmte Frequenz aufweist;
 - mit einer zweiten Digital-PLL (300), welche von dem Taktsignal getaktet wird, abhängig von dem Referenzsignal, und welche eine Schleifen-Zeitkonstante hat, die nicht wesentlich größer ist, als diejenige der Horizontal-Zeilen-PLL, zum Bilden eines Schwingungssignales, das mit dem Referenzsignal frequenzverriegelt ist, wobei die zweite Digital-PLL eine Schaltungsanordnung (318 bis 322) aufweist zum Ableiten eines Steuersignales (C') aus dem Phasen-Fehlersignal, welches von/in der zweiten Digital-PLL gebildet wird;
 - mit Mitteln (323, 328), welche mit der zweiten PLL gekoppelt sind zum Kombinieren des Steuersignales (C'), welches von der zweiten Digital-PLL (300) gebildet wird, mit dem Phasen-Fehlersignal, welches in der ersten Digital-PLL erzeugt wird, zum im wesentlichen Kompensieren der ersten Digital-PLL hinsichtlich Frequenz-Instabilitäten in dem Ausgangssignal, bezüglich des Taktsignales.
6. System nach Anspruch 5, wobei die erste Digital-PLL (250) aufweist:
- einen ersten zeitdiskreten Oszillator (252), der abhängig von dem Taktsignal (CK) und einem ersten Eingangs-Inkrementalsignal (B) ist, zum Bilden des Ausgangssignales mit im wesentlichen derselben Frequenz, wie das Farb-Referenzburst-Signal;
 - Mittel, welche erste Phasen-Vergleichermittel (236) beinhalten, zum Bilden eines Signales, das die Phasendifferenz zwischen dem Farb-Referenzburst-Signal und dem Ausgangssignal repräsentiert;
 - erste Summiermittel (240), die mit den Phasen-Vergleichermitteln gekoppelt sind, zum Kombinieren des davon erzeugten Signales mit einem Signal, welches einen vorbestimmten Wert hat, zum Bilden des Eingangs-Inkrementalsignales zum Anlegen an den zeitdiskreten Oszillator;
- dadurch gekennzeichnet,
- daß die Mittel (323,328) zum Kombinieren des Steuersignales Signal-Modifiziermittel (328) beinhalten zum Modifizieren des Signales, das von den ersten Summiermitteln in Übereinstimmung mit ei-



nem Signal (C'') erzeugt wird, welches aus dem Steuersignal (C') abgeleitet wird, zum Erzeugen eines modifizierten ersten Eingangs-Inkrement-signal (B').

7. Schaltungsanordnung nach Anspruch 6, bei der die Mittel zum Bilden des Referenzsignales beinhalten:

- einen Quarzoszillator (310) zum Bilden eines Ausgangssignales mit einer Frequenz, die im wesentlichen gleich der vorbestimmten Frequenz ist; 10
- einen Analog/Digital-Umsetzer (314), der mit dem Quarzoszillator und der Quelle von Taktsignalen (CK) gekoppelt ist, zum Bilden von Digital-Abtastwerten, welche das Referenzsignal repräsentieren, wobei die Abtastwerte (samples) die Werte des Signales repräsentieren, das von dem Quarzoszillator zu Zeitpunkten abgegeben wird, die von dem Taktsignal bestimmt werden; 15
- wobei die zweite Digital-PLL (300) beinhaltet; 20
- einen zweiten zeitdiskreten Oszillator (302), der abhängig von dem Taktsignal und einem zweiten Eingangs-Inkrement-signal (C') ist, zum Bilden des Schwingungssignales mit im wesentlichen derselben Frequenz wie das Referenzsignal; 25
- Mitteln, welche zweite Phasen-Vergleichermittel (316) beinhalten, die mit des Analog/Digital-Umsetzer (314) und dem zweiten zeitdiskreten Oszillator (302) gekoppelt sind, zum Bilden eines Signales, das die Phasendifferenz zwischen dem zweiten Referenz-Signal und dem Schwingungssignal repräsentiert; 30
- zweite Summierungsmittel (320), die mit den zweiten Phasen-Vergleichermitteln (316) gekoppelt sind, zum Kombinieren des davon abgegebenen Signales mit einem Signal (K2), welches einen vorbestimmten Wert aufweist, zum Bilden eines Signales zum Anlegen an den zweiten zeitdiskreten Oszillator als zweites Eingangs-Inkrement-signal (C') und an die Signal-Modifizierungsmittel (328) als das Steuersignal. 35

8. Anordnung nach Anspruch 7, bei der die Signal-Modifizierungsmittel (328) einen Multiplizierer beinhalten, der abhängig von ersten und zweiten Eingangssignalen ist, die von den jeweiligen ersten und zweiten Summierungsmitteln abgegeben werden, zum Bilden eines Signales, welches proportional zu dem Produkt der ersten und zweiten Eingangssignale ist, zum

Anlegen an den ersten zeitdiskreten Oszillator als das modifizierte erste Eingangs-Inkrement-signal.

5 Revendications

1. Circuit de stabilisation de boucle à verrouillage de phase pour utilisation avec :
 une source (200) de signal d'horloge d'échantillonnage (CK) qui présente des instabilités de fréquence ; et
 une première boucle à verrouillage de phase numérique (250), rythmée par ledit signal d'horloge, pour développer un signal de sortie (à partir de 248) qui possède sensiblement la même fréquence qu'un premier signal de référence, dans lequel les instabilités de fréquence dudit signal d'horloge tendent à provoquer des instabilités de fréquences dans ledit signal de sortie ; caractérisé par :
 une seconde boucle à verrouillage de phase numérique (300), rythmée par ledit signal d'horloge, pour développer un signal oscillatoire qui possède sensiblement la même fréquence qu'un second signal de référence ayant une fréquence prédéterminée, comportant le circuit (318-322) pour délivrer un signal de commande (C') à partir du signal d'erreur de phase développé dans la seconde boucle à verrouillage de phase numérique, ledit signal de commande compensant fortement dans ladite seconde boucle à verrouillage de phase numérique les instabilités de fréquence dudit signal d'horloge et entraînant ledit signal oscillatoire à être indépendant des instabilités de fréquence dudit signal d'horloge ; et
 un moyen (323, 328) couplé à ladite seconde boucle à verrouillage de phase numérique (300), pour combiner le signal de commande (C') développé par ladite seconde boucle à verrouillage de phase avec le signal d'erreur de phase développé dans la première boucle à verrouillage de phase numérique pour stabiliser la fréquence dudit signal de sortie. 10
2. Circuit de stabilisation selon la revendication 1 pour utilisation avec une première boucle à verrouillage de phase numérique (250) qui comprend :
 une borne d'entrée pour appliquer ledit premier signal de référence
 un premier oscillateur temporel numérique (252) sensible audit signal d'horloge (CK) et à un premier signal incrémental d'entrée (B) pour développer ledit signal de sortie possédant sensiblement la même fréquence que ledit premier signal de référence ; 15



un moyen, incluant un premier moyen de comparaison de phase (236) pour développer un signal représentant la différence de phase entre ledit premier signal de référence et ledit signal de sortie; et

un premier moyen additionneur (240) couplé audit premier moyen de comparaison de phase afin de combiner le signal développé ainsi avec un signal (K1) ayant une valeur prédéterminée pour développer ledit signal incrémental d'entrée pour application audit oscillateur temporel numérique (252);

caractérisé de plus en ce que:

ledit moyen pour combiner ledit signal de commande inclut un moyen de modification de signal (328) ayant un premier accès d'entrée couplé pour recevoir le signal de sortie dudit premier moyen additionneur (240), un second accès d'entrée couplé pour recevoir un second signal (C'') dérivé dudit signal de commande (C') et un accès de sortie couplé pour appliquer le signal fourni par ledit premier moyen additionneur tel que modifié par ledit signal de commande audit oscillateur temporel numérique (252) comme un premier signal incrémental d'entrée modifié (B').

3. Circuit de stabilisation selon la revendication 2 caractérisé par:

un moyen pour développer ledit second signal de référence incluant:

un oscillateur à quartz (310) pour développer un signal de sortie ayant une fréquence sensiblement égale à ladite fréquence prédéterminée; et

un convertisseur analogique-numérique (314) couplé audit oscillateur à quartz et à ladite source du signal d'horloge (CK) pour développer des échantillons numériques représentant ledit second signal de référence, lesdits échantillons possédant des valeurs représentant les valeurs du signal fourni par ledit oscillateur à quartz à des instants dans le temps déterminés par ledit signal d'horloge; et caractérisé, en outre, en ce que:

ladite seconde boucle à verrouillage de phase numérique (300) inclut:

un second oscillateur temporel numérique (302) sensible audit signal d'horloge et à un second signal incrémental d'entrée (C') pour développer ledit signal oscillatoire ayant sensiblement la même fréquence que ledit second signal de référence;

un moyen comportant un second moyen de comparaison de phase (316) couplé audit convertisseur analogique-numérique (314) et audit oscillateur temporel numérique (302) pour développer un signal représentant la dif-

férence de phase entre ledit second signal de référence et ledit signal oscillatoire; et

un second moyen additionneur (320) couplé audit second moyen de comparaison de phase (316) afin de combiner le signal fourni ainsi avec un signal (K2) ayant une valeur prédéterminée pour développer un signal (C') pour application audit oscillateur temporel numérique comme ledit second signal incrémental d'entrée et audit moyen de modification de signal comme ledit signal de commande.

4. Circuit de stabilisation selon la revendication 3, caractérisé, de plus, en ce que ledit moyen de modification de signal inclut un multiplicateur (328) sensible auxdits premier et second signaux d'entrée fournis respectivement par les premier et second moyens additionneurs (240, 320) desdites première et seconde boucles à verrouillage de phase (252, 300) pour développer un signal qui est proportionnel au produit des premier et second signaux d'entrée pour application audit premier oscillateur temporel numérique comme ledit premier signal incrémental d'entrée.

5. Système de traitement de signaux de télévision numériques comprenant:

une borne d'entrée pour appliquer (à partir de 210) un signal vidéo composite comportant des composantes de signaux de synchronisation du balayage horizontal et des composantes des signaux de chrominance incluant une composante de signaux à impulsions de référence de couleurs

une boucle à verrouillage de phase de lignes horizontales (200) sensible auxdits signaux vidéo composites et ayant une constante de temps de boucle prédéterminée pour produire un signal d'horloge d'échantillonnage (CK) qui est verrouillé en phase auxdites composantes de signaux de synchronisation de balayage horizontal, dans laquelle ledit signal d'horloge d'échantillonnage peut présenter des instabilités en fréquence;

une première boucle à verrouillage de phase numérique (250) rythmée par ledit signal d'horloge, sensible auxdits signaux vidéo composites et possédant une constante de temps de boucle qui est sensiblement plus élevée que celle de la boucle à verrouillage de phase de lignes horizontales pour développer un signal de sortie qui possède sensiblement la même fréquence que la composante de signaux à impulsions de référence de couleurs desdits signaux vidéo composites, dans laquelle ledit signal de sortie tend à présenter des instabilités en fréquence correspondant aux



instabilités en fréquence dudit signal d'horloge ; caractérisé par un circuit de stabilisation d'une boucle à verrouillage de phase comprenant :

un moyen (310) pour développer un signal de référence ayant une fréquence prédéterminée ;

une seconde boucle à verrouillage de phase numérique (300) rythmée par ledit signal d'horloge, sensible audit signal de référence et possédant une constante de temps de boucle qui n'est pas sensiblement plus élevée que celle de ladite boucle à verrouillage de phase des lignes horizontales, pour développer un signal oscillatoire qui est verrouillé en fréquence audit signal de référence, dans laquelle ladite seconde boucle à verrouillage de phase numérique inclut un circuit (318-322) pour dériver un signal de commande (C') à partir du signal d'erreur de phase développé dans la seconde boucle à verrouillage de phase numérique ; et

un moyen (323-328) couplé à ladite seconde boucle à verrouillage de phase afin de combiner le signal de commande (C') développé par ladite seconde boucle à verrouillage de phase numérique (300) avec le signal d'erreur de phase développé dans la première boucle à verrouillage de phase numérique pour compenser de façon notable dans ladite première boucle à verrouillage de phase numérique les instabilités en fréquence dudit signal de sortie associé audit signal d'horloge.

6. Système selon la revendication 5 dans lequel : ladite première boucle à verrouillage de phase numérique (250) comprend :

un premier oscillateur temporel numérique (252) sensible audit signal d'horloge (CK) et à un premier signal incrémental d'entrée (B) pour développer ledit signal de sortie ayant sensiblement la même fréquence que ledit signal à impulsions de référence de couleurs ;

un moyen incluant le premier moyen de comparaison de phase (236) pour développer un signal représentant la différence de phase entre ledit signal à impulsions de référence de couleurs et ledit signal de sortie ; et

un premier moyen additionneur (240) couplé audit moyen de comparaison de phase afin de combiner le signal produit ainsi avec un signal ayant une valeur prédéterminée pour développer ledit signal incrémental d'entrée pour application audit oscillateur temporel numérique ; et caractérisé en ce que :

ledit moyen (323, 328) pour combiner ledit signal de commande comporte un moyen de modification de signal (328) destiné à modifier

le signal fourni par ledit premier moyen additionneur en conformité avec le signal (C'') dérivé du signal de commande (C') pour produire le premier signal incrémental d'entrée modifié (B').

7. Circuit selon la revendication 6 dans lequel :

ledit moyen pour développer ledit signal de référence inclut :

un oscillateur à quartz (310) pour développer un signal de sortie ayant une fréquence sensiblement égale à ladite fréquence prédéterminée ;

un convertisseur analogique - numérique (314) couplé audit oscillateur à quartz et à ladite source de signaux d'horloge (CK) afin de développer les échantillons numériques représentant ledit signal de référence, lesdits échantillons représentant les valeurs du signal fourni par ledit oscillateur à quartz à des instants dans le temps déterminés par ledit signal d'horloge ; et dans lequel

ladite seconde boucle à verrouillage de phase numérique (300) inclut

un second oscillateur temporel numérique (302) sensible audit signal d'horloge et au second signal incrémental d'entrée (C') pour développer ledit signal oscillatoire ayant sensiblement la même fréquence que ledit signal de référence ;

un moyen incluant le second moyen de comparaison de phase (316) couplé audit convertisseur analogique-numérique (314) et audit second oscillateur temporel numérique (302) pour développer un signal représentant la différence de phase entre ledit second signal de référence et ledit signal oscillatoire ; et

un moyen additionneur (320) couplé audit second moyen de comparaison de phase (316) afin de combiner le signal fourni ainsi avec le signal (K2) ayant une valeur prédéterminée pour développer un signal pour application audit second oscillateur temporel numérique comme ledit second signal incrémental d'entrée (C') et audit moyen de modification de signal (328) comme ledit signal de commande

8. Dispositif selon la revendication 7 dans lequel ledit moyen de modification de signal (328) inclut un multiplicateur sensible aux premier et second signaux d'entrée fournis par les premier et second moyens additionneurs respectifs afin de développer un signal qui est proportionnel au produit des premier et second signaux d'entrée pour application audit premier oscillateur temporel numérique comme ledit premier signal incrémental d'entrée modifié.

