Description

The present invention relates to a waveform shaping apparatus for waveform-shaping a digital signal in the form of a base-band.

It is known in data transmission that, in order to minimize code errors due to intersymbol interference, the waveform has to be equalized, i. e., the waveform of a base-band signal has to be shaped such that on a first reference of Nyquist, or on a time axis of an impulse response signal, the signal will cross at zero points at equal intervals. A waveform shaping apparatus for performing the just mentioned purpose is described in US-A-4,374,426. It comprises:

- a shift register having a clock input terminal, a data input terminal and a plurality of data output terminals;
- a plurality of coefficient multipliers having respective input and output terminals, said input terminals of said coefficient multipliers being connected to respective data output terminals of said shift register; and
- adder means supplied with output signals from said output terminals of said coefficient multipliers to produce a summing output signal.

US-A-4,374,426 does not describe the value of the coefficients as used by said coefficient multipliers.

It is known that prior art waveform shaping apparatuses do not effectively use their entire dynamic range by shaping given data. It is therefore an object of the present invention to provide a waveform shaping apparatus utilizing its entire dynamic range for shaping a waveform with improved precision.

The waveform shaping apparatus of the present invention comprises the features of the prior art apparatus, as listed above, and it is characterized in that

- each of said coefficient multipliers uses a 2's-complement binary code being offset from the normal 2's-complement binary code by a predetermined amount; and
- a code converter means is provided for receiving said summing output signal and for converting the same to the normal binary code or the 2's-complement binary code without offset.

The above and other objects, features and advantages of the present invention will be come apparent from the following detailed description taken in conjunction with the accompanying drawings. In the drawings:

Fig. 1 is a circuit block diagram showing the fundamental construction of a waveform shaping apparatus according to an embodiment of the present invention;

Fig. 2 is a circuit block diagram showing a data transmitting-receiving system in which the waveform shaping apparatus of Fig. 1 may be advantageously employed;

Figs. 3A to -3F are respectively diagrams used to explain the operation of the present invention;

Fig. 4 is a circuit connection diagram showing an example of a coefficient multiplier included in the waveform shaping apparatus according to the present invention;

Fig. 5 is a code table to which reference will be made in explaining the present invention;

Fig. 6 is a waveform diagram showing an output waveform of a D/A (digital-to-analog) converter included in the system of Fig. 2;

Figs. 7,8 and 9 show respective code tables to which reference will be made in explaining the present invention; and

Fig. 10 is a circuit connection diagram showing an example of a code converter included in the waveform shaping apparatus according to the present invention.

A waveform shaping apparatus according to an embodiment of the present invention is shown on Fig. 1 to generally comprise a shift register 1 and a coefficient multiplier 2 consisting of elements 2_1 to 2_4 which are each formed of a coefficient generator and a multiplier and correspond in number to the respective bits of shift register 1. Coefficient multiplier 2 carries out either positive or negative weighting on an input data "1" supplied thereto from the shift register 1. The waveform shaping apparatus of Fig. 1 is further shown to comprise an adder 3 which carries out 2's-complement binary code addition with the binary code offset and then defined for the purpose of utilizing the given word length as effectively as possible, as will be described later. A binary code converter 4 is provided to convert the content or data from adder 3 to, for example, a natural binary code or 2's-complement binary code. Finally, in Fig. 1, there is shown a data input terminal 5 through which input data is supplied to shift register 1, a clock input terminal 6 through which a clock is supplied to shift register 1, and an output terminal 7 led out from binary code converter 4. In the embodiment being described, the clock applied to clock input terminal 6 has a data rate or frequency twice that at which the input data is applied to input terminal 5.

The waveform shaping apparatus of Fig. 1 is desirably used in, for example, a data transmitting-receiving system as shown in Fig. 2. Such data transmitting-receiving system is shown to have an input terminal 10 to which data from an information source is supplied, a waveform shaping apparatus 11, as shown in Fig. 1, connected between terminal 10 and a D/A converter 12 which supplies its

output through a low-pass filter 13 to a modulator 14 (for example, an amplitude modulator), and a band-pass filter 15 through which the output of modulator 14, is applied to a transmission line TL. A band-pass filter 16 receives the transmitted signal from line TL, and a detector 17 (AM detector) is connected between band-pass filter 16 and a low-pass filter 18. A slicer 19 is connected to filter 18 for detecting or demodulating the digital signal, and an output terminal 20 is led out therefrom. In this case, the transmitting side of the system is formed of the circuit elements from the input terminal 10 to the band-pass filter 15, while the receiving side is formed of the circuit elements from the band-pass filter 16 to the output terminal 20. The transmitting side and the receiving side are connected to each other by way of the transmission line TL.

The waveform shaping apparatus 11 is operated to correct the distortion of each section of the base-band signal which is demodulated in the receiving side and developed at the output of low-pass filter 18, so that such base-band signal may satisfy the first reference of Nyquist and thereby minimize the code error produced by the inter-symbol interference.

Next, the way to carry out the coefficient weighting and addition of the coefficients in the circuit of Fig. 1 will be described with reference to Figs. 3A to 3F.

If, now, the data "1" from input terminal 5 is latched in the first bit of shift register 1, as shown in Fig. 3A, this data "1" is weighted by the coefficient multiplier 2. In elements 2_1 to 2_4 of coefficient multiplier 2, the weighting coefficients of, for example, 1,2,-1 and 0, are respectively set, as in the expression of the natural number, and each of these weighting coefficients is multiplied with the respective bit of the shift register. Since the multiplied results are 1,0,0 and 0 considered from the left-hand side, if these multiplied results are added to one another in adder 3 (using the 2's-complement binary code), the added result becomes 1. By the next (second) shift clock, the content of shift register 1 is changed to 1,1,0 and 0 as shown in Fig. 3B. If this data is weighted similarly as described above, the multiplied results become 1,2,0 and 0 considered from the left-hand side. If these multiplied results are added together by adder 3, the added results become 3. If the weighting and the addition are carried out similarly thereafter, the added result becomes 1 in Fig. 3C, -1 in Fig. 3D and 0 in Fig. 3E, respectively. As a result, at the output side of adder 3, there is obtained the output signal shown in Fig. 3F and which corresponds to the input data "1".

For each of the elements 2_1 to 2_4 of coefficient multiplier 2, there may be used, for example, the circuit arrangement shown in Fig. 4. In Fig. 4, if the bit number of the weighting coefficients is, for example, 3 bits, in correspondence with such bit number of the weighting coefficients there are provided three switches 21a,21b and 21c. These switches 21a to 21c are connected in common at one side to a predetermined potential, such as, ground, while the other sides thereof are respectively connected to first input terminals of AND gate circuits 22a,22b and 22c and, through resistors 23a,23b and 23c, respectively, to a positive voltage source terminal +Vcc. The other or second input terminals of AND gate circuits 22a to 22c are connected in common to the respective bit of shift register 1 (not shown in Fig. 4). The outputs of AND gate circuits 22a,22b and 22c are led out to output terminals 24a,24b and 24c, respectively. The output terminals 24a to 24c are connected to the input side of adder 3 (not shown in Fig. 4).

Considering the case of weighting element 2_2, and assuming that the weighting coefficient thereof is 2 (Figs. 3A-3E), or "010" in 2's-complement binary code, it will be seen that such coefficient is achieved when switches 21a and 21c are turned on, while switch 21b is turned off. Accordingly, the levels at the first input terminals of AND gate circuits 22a,22b and 22c become "0","1" and "0", respectively. Under these circumstances, when the data of level "1" is supplied from the respective bit of shift register 1 to the other or second input terminals of AND gate circuits 22a,22b and 22c, only AND gate circuit 22b opens its gate, while AND gate circuits 22a and 22c remain closed. As a result, at output terminals 24a,24b and 24c, there are produced data of levels, "0","1" and "0", or data added with the weighting coefficient "2".

Considering now weighting element 2_3 which has a weighting coefficient of -1 presented as "111" by the 2's-complement binary code expression, it will be seen that, for this coefficient, switches 21a to 21c are all turned off so that, in accordance therewith, the levels at the first input terminals of AND gate circuits 22a,22b and 22c become "1","1" and "1", respectively. Under these circumstances, when the data of level "1" is supplied to the second input terminals of AND gate circuits 22a,22b and 22c from shift register 1, AND gate circuits 22a to 22c are all opened. As a result, at the output terminals 24a,24b and 24c, there are produced the data having the levels of "1","1" and "1", or the data added with the weighting coefficient "-1".

In other words, coefficient multiplier 2 supplies to adder 3 the data added with the positive or negative weighting coefficient with respect to the input data "1". The adder 3 carries out the 2's-complement binary code addition and supplies the added result to binary code converter 4. In such

circuit arrangement, problems may arise as to the effective availability of the dynamic range in adder 3, and as to whether or not the given word length is utilized as effectively as possible.

The 2's-complement binary code is defined as shown in the table of Fig. 5 in the case of 3 bits. In such case, in respect to the 0 level, three levels are expressed at the positive side and four levels are expressed at the negative side.

However, if waveform shaping is carried out by the waveform shaping circuit of Fig. 1, the added result is largely displaced to the positive side, while the large level at the negative side does not appear so that the available word length is not utilized effectively. In other words, if the word length is not limited, the added result is largely displaced to the positive side, for example, as shown on Fig. 6.

Accordingly, in order to carry out such addition precisely within the limitations of the limited word length, the waveform shaping apparatus must be arranged so that the addition can be carried out by a normal adder similarly to the 2's-complement binary code and a binary code whose dynamic range is wide at the positive side must be defined. To this end, it is sufficient that the normal 2's-complement binary code be offset and defined.

For example, as shown in Fig. 7, if the least significant two levels "101" (-3) and "100" (-4) at the negative side of the normal 2's-complement binary code shown in column (A) are shifted to the most significant positive side and defined as "101" (5) and "100" (4), as shown in column (B), the resulting binary code defined between the positive maximum value and the negative minimum value, has a fine quantization step and the accuracy can be improved. Further, addition can be carried out in the form of the normal 2's-complement binary code.

The positive and negative displacements of the added results become different dependent on the roll-off rate, the characteristic of distortion to be equalized and so on. Accordingly, when the binary code is defined, the weighting coefficient, which is calculated with the assumption that there is no word length limitation, is set first. The amount of the displacement is checked by carrying out the adding simulation by using a calculator and then the offset level is determined such that the ability of the given word length can be demonstrated as much as possible. Then, the weighting coefficient expressed by the defined binary code is determined. The offset binary code defined here is effective only for this particular waveform shaping circuit so that, when the latter is connected to, for example, the D/A converter 12, such offset binary code must be first converted to the binary code which is defined by the D/A converter 12. This conversion is carried out by the binary code converter 4.

For example, if as shown in Fig. 8, "010" (2) is added to the offset binary code for addition (corresponding to column (B) of Fig. 7), such offset binary code is converted to the natural binary code. On the other hand, when "110" (-2) is added to the offset binary code of column (B) in Fig. 7, such binary code is converted to the 2's-complement binary code. More specifically, comparing the offset binary code shown in the left-hand table of Fig. 8 with the natural binary code shown in the right-hand table in Fig. 8, it will be seen that the defined or offset binary code is equal to the binary code which is offset by -2 from the natural binary code. Therefore, when such defined or offset binary code is converted to the natural binary code, +2 is added thereto so as to restore it to the original binary code as mentioned above. Further, when the ordinary 2's-complement binary code in column (A) of Fig. 7 is defined as the 2's-complement binary code in column (B) of Fig. 7, such ordinary or normal binary code is offset by +2. Accordingly, when such offset 2's-complement binary code is to be converted to the normal 2's-complement binary code, such offset binary code is returned to the original binary code by adding -2 thereto.

A numerical value other than 2 can be used for offsetting the binary code. For example, when the 2's-complement binary code in column (B) of Fig. 7 is defined from the normal 2's-complement binary code in column (A), if "110" (-2) in column (B) is shifted to "110" (6), to thereby make "110" (6) the maximum value at the positive side and to make "111" (-1) the minimum value at the negative side, as shown in the table at the left-hand side of Fig. 9. Such further offset binary code is converted to the natural binary code or the 2's-complement binary code as follows: In the case of conversion to the natural binary code, since that offset or adding binary code is offset by -1 in respect to the natural binary code, it is returned to the natural or normal binary code by offsetting it by +1 ("001"). In the case of returning to the 2's-complement binary code, it is offset by +3 so that it is returned to the normal 2's-complement binary code by offsetting it -3 ("101"), as shown in Fig. 9.

Referring now to Fig. 10, it will be seen that the binary code converter 4 of Fig. 1 may have input terminals 4a,4b and 4c through which the outputs (three bits) from adder 3 are supplied to an adder 4d having output terminals 4e, 4f and 4g at which the converted binary codes are developed. In accordance with the number of bits to be added in the conversion, switches of a predetermined number, for example, three switches 4h,4i and 4j are provided. These switches 4h to 4j are connected in common at one side to the ground, while the other sides thereof are connected to respective inputs of

adder 4d and, through resistors 4k, 4ℓ, and 4m, respectively, to a positive power source terminal +Vcc.

When a conversion, for example, as shown in Fig. 8, is carried cut, in order to reconvert the offset binary code for addition to the natural binary code, the switches 4h and 4j are turned on but the switch 4i is turned off so that the data of level "010" is supplied to adder 4d in which it is added to the 3 bits from input terminals 4a to 4c in the binary code manner. Similarly, in order to reconvert the offset binary code for addition to the normal 2's-complement binary code, the switches 4h and 4i are turned off but the switch 4j is turned on so that the data of level "110" is supplied to adder 4d in which it is added to the 3 bits from input terminals 4a to 4c.

When the conversion shown in Fig. 9 is carried out, in order to reconvert the offset binary code for addition to the natural binary code, switches 4h and 4i are turned on but switch 4j is turned off so that the data of level "001" is supplied to adder 4d in which it is added with the 3 bits from input terminals 4a to 4c in the binary code manner. Similarly, in order to reconvert the offset binary code for addition, as shown on the left side of Fig. 9, to the normal 2's-complement binary code switches 4h and 4j are turned off but switch 4i is turned on so that the data of level "101" is supplied to the adder 4d in which it is added with the 3 bits from input terminals 4a to 4c.

As set forth above, in accordance with the present invention, the weighted coefficients are selected so that the offset binary code is defined and calculated for utilizing the given word length as much as possible and the added result is converted to the natural binary code or the 2's-complement binary code, so that the addition can be carried out by utilizing the given word length as effectively as possible. Accordingly, the full dynamic range can be used as effectively as possible. Thus, the precision in waveform shaping can be improved considerably. Moreover, the desired highest precision can be realized by hardware of simple circuit construction.

Furthermore, since the optimum binary code for the waveform shaping can be defined and the weighting coefficients can be easily set by such definition of the optimum binary code, the optimum waveform shaping operation for various kinds of systems can be carried out easily by the same hardware.

Claims

1. A waveform shaping apparatus (11) comprising:
   - a shift register (1) having a clock input terminal (6), a data input terminal (5) and a plurality of data output terminals;
   - a plurality of coefficient multipliers (2_1, 2_2, 2_3, 2_4) having respective input and output terminals, said input terminals of said coefficient multipliers being connected to respective data output terminals of said shift register; and
   - adder means (3) supplied with output signals from said output terminals of said coefficient multipliers to produce a summing output signal;

   characterized in that
   - each of said coefficient multipliers uses a 2's-complement binary code being offset from the normal 2's-complement binary code by a predetermined amount; and
   - a code converter means (4) is provided for receiving said summing output signal and for converting the same to the normal binary code or the 2's-complement binary code without offset.

2. A waveform shaping apparatus according to claim 1, **characterized in that** each of said coefficient multipliers (2_1, 2_2, 2_3, 2_4) is presettable manually to a predetermined coeffient.

3. A waveform shaping apparatus according to claim 2, **characterized in that** each of said coefficient multipliers (2_1, 2_2, 2_3, 2_4) comprises
   - a plurality of AND gate circuits (22a, 22b, 22c) each having first and second input terminals and an output terminal (24a, 24b, 24c), each of said first input terminals being connected to a respective one of said data output terminals of said shift register (1) and each of said output terminals (24a, 24b, 24c) being connected to the input terminal of said adder means (3);
   - a plurality of ON/OFF switches (21a, 21b, 21c) connected between a reference point and a respective one of said second input terminals of said AND gate circuits; and
   - a biasing voltage source (Vcc) connected to said second input terminals.

4. A waveform shaping apparatus according to one of the preceding claims, **characterized by** a D/A-converter (12) connected to said code converter means (4) to produce an analog signal in response to the digital signal as output by said code converter means.

Revendications

adder 4d and, through resistors 4k, 4ℓ, and 4m, respectively, to a positive power source terminal +Vcc.

When a conversion, for example, as shown in Fig. 8, is carried cut, in order to reconvert the offset binary code for addition to the natural binary code, the switches 4h and 4j are turned on but the switch 4i is turned off so that the data of level "010" is supplied to adder 4d in which it is added to the 3 bits from input terminals 4a to 4c in the binary code manner. Similarly, in order to reconvert the offset binary code for addition to the normal 2's-complement binary code, the switches 4h and 4i are turned off but the switch 4j is turned on so that the data of level "110" is supplied to adder 4d in which it is added to the 3 bits from input terminals 4a to 4c.

When the conversion shown in Fig. 9 is carried out, in order to reconvert the offset binary code for addition to the natural binary code, switches 4h and 4i are turned on but switch 4j is turned off so that the data of level "001" is supplied to adder 4d in which it is added with the 3 bits from input terminals 4a to 4c in the binary code manner. Similarly, in order to reconvert the offset binary code for addition, as shown on the left side of Fig. 9, to the normal 2's-complement binary code switches 4h and 4j are turned off but switch 4i is turned on so that the data of level "101" is supplied to the adder 4d in which it is added with the 3 bits from input terminals 4a to 4c.

As set forth above, in accordance with the present invention, the weighted coefficients are selected so that the offset binary code is defined and calculated for utilizing the given word length as much as possible and the added result is converted to the natural binary code or the 2's-complement binary code, so that the addition can be carried out by utilizing the given word length as effectively as possible. Accordingly, the full dynamic range can be used as effectively as possible. Thus, the precision in waveform shaping can be improved considerably. Moreover, the desired highest precision can be realized by hardware of simple circuit construction.

Furthermore, since the optimum binary code for the waveform shaping can be defined and the weighting coefficients can be easily set by such definition of the optimum binary code, the optimum waveform shaping operation for various kinds of systems can be carried out easily by the same hardware.

Claims

1. A waveform shaping apparatus (11) comprising:
   - a shift register (1) having a clock input terminal (6), a data input terminal (5) and a plurality of data output terminals;
   - a plurality of coefficient multipliers (2_1, 2_2, 2_3, 2_4) having respective input and output terminals, said input terminals of said coefficient multipliers being connected to respective data output terminals of said shift register; and
   - adder means (3) supplied with output signals from said output terminals of said coefficient multipliers to produce a summing output signal;

   characterized in that
   - each of said coefficient multipliers uses a 2's-complement binary code being offset from the normal 2's-complement binary code by a predetermined amount; and
   - a code converter means (4) is provided for receiving said summing output signal and for converting the same to the normal binary code or the 2's-complement binary code without offset.

2. A waveform shaping apparatus according to claim 1, **characterized in that** each of said coefficient multipliers (2_1, 2_2, 2_3, 2_4) is presettable manually to a predetermined coeffient.

3. A waveform shaping apparatus according to claim 2, **characterized in that** each of said coefficient multipliers (2_1, 2_2, 2_3, 2_4) comprises
   - a plurality of AND gate circuits (22a, 22b, 22c) each having first and second input terminals and an output terminal (24a, 24b, 24c), each of said first input terminals being connected to a respective one of said data output terminals of said shift register (1) and each of said output terminals (24a, 24b, 24c) being connected to the input terminal of said adder means (3);
   - a plurality of ON/OFF switches (21a, 21b, 21c) connected between a reference point and a respective one of said second input terminals of said AND gate circuits; and
   - a biasing voltage source (Vcc) connected to said second input terminals.

4. A waveform shaping apparatus according to one of the preceding claims, **characterized by** a D/A-converter (12) connected to said code converter means (4) to produce an analog signal in response to the digital signal as output by said code converter means.

Revendications

* C L M S *

1. Appareil de formage de formes d'onde (11) comprenant :
   - un registre (1) à décalage comportant une borne d'entrée d'horloge (6), une borne d'entrée de données et une pluralité de bornes de sortie de données ;
   - une pluralité de multiplieurs à coefficient (2_1, 2_2, 2_3, 2_4) comportant des entrées et des sorties respectives, lesdites bornes d'entrée desdits multiplieurs à coefficient étant connectées à des bornes de sortie de données respectives dudit registre à décalage ; et,
   - des moyens additionneurs (3) alimentés par les signaux de sortie desdites bornes de sortie desdits multiplieurs à coefficient pour produire un signal de sortie de sommation ;

     caractérisé en ce que :
   - chacun des multiplieurs à coefficient utilise un code binaire complémenté à deux, qui est décalé du code binaire normal complémenté à deux d'une quantité prédéterminée ; et
   - un moyen de conversion de code (4) est prévu pour recevoir ledit signal de sortie de sommation et pour convertir celui-ci en un code binaire normal ou en un code binaire à complément à deux sans décalage.

2. Appareil de formage de formes d'onde selon la revendication 1, caractérisé en ce que chacun desdits multiplieurs à coefficient (2_1, 2_2, 2_3, 2_4) est manuellement préréglable à un coefficient prédéterminé.

3. Appareil de formage de formes d'onde selon la revendication 2, caractérisé en ce que chacun des multiplieurs à coefficient comporte :

   une pluralité de portes ET (22a, 22b, 22c) chacune ayant des premières et secondes bornes d'entrée et une borne de sortie (24a, 24b, 24c), chacune desdites premières bornes d'entrée étant connectée à l'une respective desdites bornes de sortie de données dudit registre à décalage (1), et chacune desdites bornes de sortie (24a, 24b, 24c) étant connectée à la borne d'entrée desdits moyens additionneurs (3) ;
   - une pluralité d'interrupteurs (21a, 21a, 21c) connectés entre un point de référence et l'une quelconque desdites secondes bornes d'entrée desdites portes ET ; et,
   - une source de tension de polarisation (Vcc) connectée aux dites secondes bornes d'entrée.

4. Appareil de formage de formes d'onde selon l'une quelconque des revendications précédentes, caractérisé en ce que on connecte un convertisseur numérique analogique (12) aux dits moyens de conversion de code (4) pour produire un signal analogique en réponse au signal numérique comme sortie desdits moyens de conversion de code.

Patentansprüche

1. Vorrichtung (11) zur Wellenformung mit:
   - einem Schieberegister (1) mit einem Takteingang (6), einem Dateneingang (5) und einer Mehrzahl von Datenausgängen;
   - einer Mehrzahl mit entsprechenden Ein- und Ausgängen versehenen Koeffizienten-Multiplizierern (2_1, 2_2, 2_3, 2_4), deren Eingänge mit den entsprechend zugeordneten Datenausgängen der Schieberegister verbunden sind; und
   - Addierern (3), die mit den Ausgangssignalen der Ausgänge der Koeffizienten-Multiplizierer beaufschlagt sind und ein Summenausgangssignal liefern, **dadurch gekennzeichnet,** daß
   - jeder der Koeffizienten-Multiplizierer einen 2 er-Komplement-Binärcode verwendet, der gegenüber dem normalen 2 er-Komplement-Binärcode um einen bestimmten Betrag versetzt ist; und
   - ein Codeumsetzer (4) vorhanden ist, der durch das Summenausgangssignal beaufschlagt ist und dieses in den normalen Binärcode oder den 2-er Komplement-Binärcode ohne Versatz umsetzt.

2. Vorrichtung zur Wellenformung nach Anspruch 1, **dadurch gekennzeichnet,** daß jeder der Koeffizienten-Multiplizierer (2_1, 2_2, 2_3, 2_4) manuell auf einen vorgebbaren Koeffizienten voreinstellbar ist.

3. Vorrichtung zur Wellenformung nach Anspruch 2, **dadurch gekennzeichnet,** daß jeder der Koeffizienten-Multiplizierer (21, 22, 23, 24) folgende Baugruppen umfaßt:
   - eine Mehrzahl von UND-Gliedern (22a, 22b, 22c), die jeweils erste und zweite Eingänge und einen Ausgang (24a, 24b, 24c) aufweisen, wobei jeder der ersten Eingänge mit einem entsprechend zugeordneten der Datenausgänge des Schieberegisters (1) und jeder der Ausgänge (24a, 24b, 24c) an den Eingang des Addierers (3) angeschlossen ist;

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- eine Mehrzahl von EIN/AUS-Schaltern (21, 21b, 21c), die zwischen einem Referenzpunkt und einem jeweils zugeordneten der zweiten Eingänge der UND-Glieder angeschlossen sind; sowie
- eine an die zweiten Eingänge angeschlossene Vorspannungsquelle (Vcc).

4. Vorrichtung zur Wellenformung nach einem der vorstehenden Ansprüche, **gekennzeichnet durch** einen mit dem Codeumsetzer (4) verbundenen D/A-Wandler (12), der einen dem Digitalsignal am Ausgang des Codeumsetzers entsprechendes Analogsignal erzeugt.