

Description

The present invention relates to a method of, and a circuit for, estimating true data from distorted digital data signals which may have become distorted during transmission.

In systems involving the transmission of data, it is important to try and avoid the effects of data becoming sufficiently distorted that falsing of the data occurs. For example, in a paging system if address data becomes distorted in transmission then it is possible that the true addressee of the paging call is not alerted because the address information has become corrupted.

US Patent Specification 3479457 discloses an apparatus for demodulating phase - or frequency - modulated signals by high speed coded signals. Faults, for example, degradations in the signal to be demodulated, are corrected by clocking the signal into a shift register at a higher frequency than the frequency of the signal to be demodulated. Then pairs of signals from the shift register are compared in an Exclusive-OR circuit and the result is fed to a second shift register having three stages. Different pairs of outputs of the second shift register are taken and supplied to a majority logic circuit comprising three AND gates and three input OR gates connected to the output of each of the AND gates. If necessary this circuitry is duplicated to rectify further faults. A drawback to this known circuit is the amount of hardware involved in the majority logic stage if the number of samples is increased. For example, this cited specification states that if one stores five samples in the second shift register which now has five stages then to obtain a majority logic decision by considering different combinations of three samples, ten AND gates are required.

US Patent Specification 3859655 also discloses reforming a signal using a shift register and majority logic.

US Patent Specification 4241311 discloses a method of filtering high frequency noise from an alternating analog data signal of a selected frequency F. In the known method a bi-level or square wave signal is formed from the analog data. The bi-level data signal is sampled at a sample rate of at least 8 times the frequency F of the alternating analog data signal and the samples are fed successively to a shift register having at least three stages. A selected number of samples are read-out in parallel from the shift register into a majority gate. The majority decision from the majority gate is applied to a latch in synchronism with the clock signal. The output of the latch is a digital majority noise filtered version of the input analogue signal.

A drawback to these known systems is that to improve performance more and more circuit ele-

ments are required to increase the number of samples used in making the majority logic decision. Accordingly, in situations where space and power consumption are of importance, such as in paging receivers, then it is desirable to be able to make a confident decision based on a smaller number of samples when estimating true data from distorted digital data signals.

According to one aspect of the present invention there is provided a method of estimating true data from distorted digital data signals, comprising successively sampling the digital signal at a clock frequency greater than that of the data rate, applying a plurality of n successive samples to a majority logic circuit having $(n + 1)$ inputs, feeding back to the $(n + 1)$ th input a preceding majority logic circuit decision and repeating the operation by adding at least one new sample to, and discarding at least the longest held sample from, said plurality of successive samples, the output of the majority logic circuit being used to determine the true value of the digital data signal.

According to another aspect of the present invention there is provided a circuit for estimating true data from distorted digital data signals, comprising a shift register having a plurality of n stages, each stage having an output, an input terminal connected to the shift register for applying digital data signals thereto, means for clocking the shift register at a frequency greater than the data rate, and a majority logic circuit having $(n + 1)$ inputs, n inputs of which are coupled to respective outputs of the shift register stages, the $(n + 1)$ th input being coupled to a feedback connection which in use applies a preceding majority logic circuit decision thereto.

The method and circuit in accordance with the present invention not only enables an estimation of the true signal from a noisy or distorted digital signal but also enables the effective signal-to-noise ratio of the input signal to be improved.

By having feedback to the $(n + 1)$ th input of the majority logic circuit, fewer true samples have to be taken in order to correct a false one. If the number of samples taken is $(n + 1)$, then the number of samples which can be corrected is $(n/2)$.

The circuit is independent of technology and the rate of sampling or clocking is optional although it is preferred that it should be of the order of eight times the data rate.

The present invention will now be described, by way of example, with reference to the accompanying drawings, wherein:

Figure 1 is a block schematic circuit diagram of an embodiment of the present invention in which feedback is provided between the data output and an input to the majority logic circuit.

Figure 2 shows four waveform diagrams referen-

ced (a), (b), (c) and (d).

Figure 3 shows different data signals, signals (a) and (b) are for use with a circuit with feedback, signals (c) and (d) are for use with a circuit without feedback, signal (e) is a distorted input signal and signal (f) is an output estimation of the true version of the distorted signal (e), and Figure 4 is a schematic circuit diagram of an embodiment of the present invention.

Referring to Figure 1 of the drawings, a data input signal is applied via an input terminal 10 to a six stage shift register 12 which is clocked at say eight times the data rate by a clock signal generator 14. The outputs Q_0 to Q_5 of the shift register 12 are applied to respective inputs of a seven input majority logic circuit 16. An output of the circuit 16 is connected to a latching circuit 18 which is clocked in antiphase relative to the clocking of the shift register 12. An output of the latching circuit 18 is applied to an output terminal 20 and is also fed back to the seventh input of the circuit 16.

In operation the clock waveforms (a) and (d) of Figure 2 are applied to the clock inputs of the shift register 12 and the latching circuit 18, respectively, both of which are clocked on a low to high transition as indicated by the arrows applied to these transitions. The data signal, waveform (b) of Figure 2, is applied to the input terminal 10. The value of the input signal when sampled is stored serially in the shift register 12. The outputs Q_0 to Q_5 of the respective stages of the shift register 12 are applied to the majority logic circuit 16 together with the output the latch circuit 18. As the circuit 16 has an odd number of inputs there will always be a majority decision output. Thus if three inputs are "1"s and the three others are "0"s then the output will be dependant on the output of the latch 18. If this output is a "1" then the majority output will be a "1" and conversely if it a "0" then the majority output will be a "0". In effect the output produced by the latch 18 in one clock cycle influences the majority decision in the next following clock cycle. When the clock input to the latch 18 next goes high the majority decision of the circuit 16, waveform (c) in Figure 2, is stored. There is a majority logic circuit propagation delay τ between the transitions in the data and the majority logic decision.

The number of input signal errors which can be corrected is related to the number $(n + 1)$ of the inputs to the majority logic circuit 16 and is defined generally as $\lfloor (n/2) \rfloor$. In the case of $n = 6$ then three error bits can be corrected, for example in Figure 3(a) the three "0"s will be corrected to all "1"s and conversely in Figure 3(b) the three "1"s will be corrected to all "0"s.

If feedback from the output of the latching circuit 18 to the seventh input of the majority logic

circuit is not provided then in order to be able to correct three errors, a seven stage shift register would be required. Thus the number of shift register stages and the number of majority logic circuit inputs equals an odd number $(n + 1)$. Figures 3(c) and 3(d) illustrate that in order to correct three successive errors, that is the "0"s in Figure 3(c) and the "1"s in Figure 3(d), it is necessary to have four correct digits before and after the erroneous ones as opposed to three correct digits before and after the erroneous ones as shown in Figures 3(a) and 3(b).

Figure 3(e) illustrates a signal having a distorted transition from 1 to 0 and Figure 3(f) illustrates how this signal can be estimated by the circuit in accordance with the present invention so that there is a single transition from "1" to "0".

Figure 4 is a schematic circuit diagram of an embodiment of the present invention having a feedback connection between the output of the latching circuit 18 and the majority logic circuit 16. In this embodiment the latching circuit 18 comprises part of an integrated circuit type CD 4013 and the shift register 12 comprises two six stage shift register integrated circuits 12A, 12B of type CD 4015, both of these integrated circuit types being manufactured by the Radio Corporation of America. The majority logic circuit 16 is constituted by a plurality of NAND-gates, EX-OR gates and inverters.

For convenience of description the circuit 16 may be regarded as comprising four identical modules 30, 40, 50 and 60 and several other components. Only one of the modules, the module 30, will be described in detail.

Outputs Q_0 and Q_1 of the shift register circuit 12A are connected to the inputs of a NAND gate 22 and of an EX-OR gate 24. The output of the NAND gate 22 is inverted by an inverter 26 and is applied as one (31) of two inputs to the module 30, the other (32) of the two inputs being the output of the EX-OR gate 24.

The input 31 is applied to an EX-OR gate 33 and to a NAND gate 34 and the other input 32 is applied to the EX-OR gate 33 and to an EX-OR gate 35. The output of the EX-OR gate 33 is applied as an input to a NAND gate 36. An output Q_2 of the shift register circuit 12A is connected as an input to the EX-OR gate 35 and the NAND gate 36, and, via an inverter 37, to the NAND gate 38. An output of the NAND gate 38 and an input of the EX-OR gate 35 comprise, respectively, inputs 41 and 42 of the module 40. A third input to the module 40 comprises the output Q_3 of the shift register circuit 12A. These three inputs are applied as respective inputs to a NAND gate 70 whose output comprises one input of a four input NAND gate 78.

The outputs of the module 40 are applied as

inputs 51 and 52 of the module 50. Additionally an output Q_0' of the shift register circuit 12B is applied as a third input to the module 50. These three inputs are also applied to a NAND gate 72 whose output is connected to a second input of the NAND gate 78.

In a similar manner the outputs of the module 50 comprise inputs 61 and 62 of the module 60 whose third input is the output Q_1' of the shift register circuit 12B. These three inputs are connected to a NAND gate 74 whose output comprises a third input of the NAND gate 78.

The two outputs of the module 60 together with the feedback connection from the output of the latch 18 are applied to a NAND gate 76 whose output comprises a fourth input of the NAND gate 78. The output of the NAND gate 78 is connected to the data input D of the latch 18.

As an example of the operation of the majority logic circuit 16, it can be shown that in the event of shift register outputs Q_0 , Q_1 and Q_2 being "1" and the outputs Q_3 , Q_0' , and Q_1' being "0" then the binary value of the feedback signal determines whether the output or the latch, when clocked, will be a "1" or a "0".

In the event of not having a feedback input, then it will be necessary to have an extra module in the circuit 16 together with a further output from the shift register 12.

Claims

1. A method of estimating true data from distorted digital data signals, including successively sampling the digital signal at a clock frequency (14) greater than that of the data rate and applying a plurality of the successive samples to n inputs of a majority logic circuit (16), characterised in that the majority logic circuit (16) has $(n + 1)$ inputs, in that a preceding majority logic circuit decision is fed back to the $(n + 1)$ th input of the majority logic circuit (16), in that the operation is repeated by adding at least one new sample (Q_0) to, and discarding at least the longest held sample (Q_5) from, said plurality of successive samples, and in that the output (20) of the majority logic circuit (16) is used to determine the true value of the digital data signal.
2. A method as claimed in Claim 1, characterised in that the sampling is carried out at least eight times the data rate.
3. A method as claimed in Claim 1 or 2, characterised in that the preceding logic circuit decision is stored by a latching circuit (18), the output (20) of the latching circuit being applied

to the $(n + 1)$ th input of the majority logic (16).

4. A circuit for estimating true data from distorted digital data signals, comprising a shift register (12) having a plurality of n stages, each stage having an output, an input terminal (10) connected to the shift register (12) for applying digital data signals thereto, means (14) for clocking the shift register at a frequency greater than the data rate, and a majority logic circuit (16) having inputs connected respectively to the outputs of the n shift register stages, characterised in that the majority logic circuit (16) has $(n + 1)$ inputs, and in that the $(n + 1)$ th input is coupled to a feedback connection which in use applies a preceding majority logic circuit decision thereto.
5. A circuit as claimed in Claim 4, characterised in that a latching circuit (18) is connected to an output of the majority logic circuit (16), and in that the latching circuit is clocked by the clocking means (14).
6. A circuit as claimed in Claim 5, characterised in that the feedback connection is connected to an output of the latching circuit (18).

Revendications

1. Procédé pour l'estimation de données vraies dans des signaux de données numériques déformés, comprenant l'échantillonnage successif du signal numérique à une fréquence d'horloge (14) supérieure à la fréquence de données et l'application d'une pluralité d'échantillons successifs à n entrées d'un circuit logique majoritaire (16), caractérisé en ce que le circuit logique majoritaire (16) présente $(n + 1)$ entrées, en ce qu'une décision précédente du circuit logique majoritaire est rétrocouplée à la $(n + 1)^{\text{ème}}$ entrée du circuit logique majoritaire (16), en ce que l'opération est répétée par addition d'au moins un nouvel échantillon (Q_0) à ladite pluralité d'échantillons successifs et par suppression d'au moins l'échantillon le plus longtemps maintenu (Q_5) de celle-ci et en ce que la sortie (20) du circuit logique majoritaire (16) est utilisée pour déterminer la valeur vraie du signal de données numériques.
2. Procédé selon la revendication 1, caractérisé en ce que l'échantillonnage est effectué à au moins huit fois la fréquence de données.
3. Procédé selon la revendication 1 ou 2, caractérisé en ce que la décision précédente du circuit logique est emmagasinée par un circuit de



inputs 51 and 52 of the module 50. Additionally an output Q_0' of the shift register circuit 12B is applied as a third input to the module 50. These three inputs are also applied to a NAND gate 72 whose output is connected to a second input of the NAND gate 78.

In a similar manner the outputs of the module 50 comprise inputs 61 and 62 of the module 60 whose third input is the output Q_1' of the shift register circuit 12B. These three inputs are connected to a NAND gate 74 whose output comprises a third input of the NAND gate 78.

The two outputs of the module 60 together with the feedback connection from the output of the latch 18 are applied to a NAND gate 76 whose output comprises a fourth input of the NAND gate 78. The output of the NAND gate 78 is connected to the data input D of the latch 18.

As an example of the operation of the majority logic circuit 16, it can be shown that in the event of shift register outputs Q_0 , Q_1 and Q_2 being "1" and the outputs Q_3 , Q_0' , and Q_1' being "0" then the binary value of the feedback signal determines whether the output or the latch, when clocked, will be a "1" or a "0".

In the event of not having a feedback input, then it will be necessary to have an extra module in the circuit 16 together with a further output from the shift register 12.

Claims

1. A method of estimating true data from distorted digital data signals, including successively sampling the digital signal at a clock frequency (14) greater than that of the data rate and applying a plurality of the successive samples to n inputs of a majority logic circuit (16), characterised in that the majority logic circuit (16) has $(n + 1)$ inputs, in that a preceding majority logic circuit decision is fed back to the $(n + 1)$ th input of the majority logic circuit (16), in that the operation is repeated by adding at least one new sample (Q_0) to, and discarding at least the longest held sample (Q_5) from, said plurality of successive samples, and in that the output (20) of the majority logic circuit (16) is used to determine the true value of the digital data signal.
2. A method as claimed in Claim 1, characterised in that the sampling is carried out at least eight times the data rate.
3. A method as claimed in Claim 1 or 2, characterised in that the preceding logic circuit decision is stored by a latching circuit (18), the output (20) of the latching circuit being applied

to the $(n + 1)$ th input of the majority logic (16).

4. A circuit for estimating true data from distorted digital data signals, comprising a shift register (12) having a plurality of n stages, each stage having an output, an input terminal (10) connected to the shift register (12) for applying digital data signals thereto, means (14) for clocking the shift register at a frequency greater than the data rate, and a majority logic circuit (16) having inputs connected respectively to the outputs of the n shift register stages, characterised in that the majority logic circuit (16) has $(n + 1)$ inputs, and in that the $(n + 1)$ th input is coupled to a feedback connection which in use applies a preceding majority logic circuit decision thereto.
5. A circuit as claimed in Claim 4, characterised in that a latching circuit (18) is connected to an output of the majority logic circuit (16), and in that the latching circuit is clocked by the clocking means (14).
6. A circuit as claimed in Claim 5, characterised in that the feedback connection is connected to an output of the latching circuit (18).

Revendications

1. Procédé pour l'estimation de données vraies dans des signaux de données numériques déformés, comprenant l'échantillonnage successif du signal numérique à une fréquence d'horloge (14) supérieure à la fréquence de données et l'application d'une pluralité d'échantillons successifs à n entrées d'un circuit logique majoritaire (16), caractérisé en ce que le circuit logique majoritaire (16) présente $(n + 1)$ entrées, en ce qu'une décision précédente du circuit logique majoritaire est rétrocouplée à la $(n + 1)^{\text{ème}}$ entrée du circuit logique majoritaire (16), en ce que l'opération est répétée par addition d'au moins un nouvel échantillon (Q_0) à ladite pluralité d'échantillons successifs et par suppression d'au moins l'échantillon le plus longtemps maintenu (Q_5) de celle-ci et en ce que la sortie (20) du circuit logique majoritaire (16) est utilisée pour déterminer la valeur vraie du signal de données numériques.
2. Procédé selon la revendication 1, caractérisé en ce que l'échantillonnage est effectué à au moins huit fois la fréquence de données.
3. Procédé selon la revendication 1 ou 2, caractérisé en ce que la décision précédente du circuit logique est emmagasinée par un circuit de

- verrouillage (18), le signal de sortie (20) du circuit de verrouillage étant appliqué à la (n + 1)^{ème} entrée du circuit logique majoritaire (16).
4. Circuit pour l'estimation de données vraies dans des signaux de données numériques déformés, comportant un registre de décalage (12) ayant une pluralité de n étages, chaque étage ayant une sortie, une borne d'entrée (10) reliée au registre de décalage (12) pour appliquer des signaux de données numériques à celui-ci, des moyens d'horloge (14) pour rythmer le registre de décalage à une fréquence supérieure à la fréquence de données, et un circuit logique majoritaire (16) ayant des entrées reliées respectivement aux sorties des n étages de registre de décalage, caractérisé en ce que le circuit logique majoritaire (16) présente (n + 1) entrées et en ce que la (n + 1)^{ème} entrée est couplée à une liaison de rétrocouplage qui, lors du fonctionnement, applique une décision précédente du circuit logique majoritaire à celle-ci.
 5. Circuit logique selon la revendication 4, caractérisé en ce qu'un circuit de verrouillage (18) est relié à une sortie du circuit logique majoritaire, et en ce que le circuit de verrouillage est rythmé sous la commande d'une horloge (14).
 6. Circuit selon la revendication 5, caractérisé en ce que la liaison de rétrocouplage est reliée à une sortie du circuit de verrouillage (18).

Patentansprüche

1. Verfahren zum Abschätzen wahrer Daten aus verzerrten digitalen Datensignalen, wobei nacheinander die folgenden Verfahrensschritte durchgeführt werden: das Abtasten des digitalen Signals mit einer Taktimpulsfrequenz (14), die höher ist als die Datengeschwindigkeit und das Zuführen einer Anzahl aufeinanderfolgender Abtastwerte zu n Eingängen einer Mehrheitslogik (16), dadurch gekennzeichnet, daß die Mehrheitslogik (16) (n+1)-Eingänge hat, daß eine vorhergehende Mehrheitslogikentscheidung zu dem (n+1). Eingang der Mehrheitslogik (16) zurückgeführt wird, daß der Vorgang dadurch wiederholt wird, daß wenigstens ein neuer Abtastwert (Q_0) hinzuaddiert wird und daß wenigstens der am längsten festgehaltene Abtastwert (Q_5) aus der genannten Anzahl aufeinanderfolgender Abtastwerte gelöscht wird, und daß der Ausgang (20) der Mehrheitslogik (16) dazu benutzt wird, den wahren Wert des digitalen Datensignals zu ermitteln.
2. Verfahren nach Anspruch 1, dadurch gekennzeichnet, daß das Abtasten mit mindestens der achtfachen Datengeschwindigkeit erfolgt.
3. Verfahren nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die vorhergehende Mehrheitslogikentscheidung von einer Verriegelungsschaltung (18) gespeichert wird, wobei der Ausgang (20) derselben mit dem (n+1). Eingang der Mehrheitslogik (16) verbunden ist.
4. Schaltungsanordnung zum Abschätzen wahrer Daten aus verzerrten digitalen Datensignalen mit einem Schieberegister (12) mit einer Anzahl von n Stufen mit je einem Ausgang, wobei eine Eingangsklemme (10) mit dem Schieberegister (12) verbunden ist, und zwar zum Zuführen digitaler Datensignale zu derselben, mit Mitteln (14) zum Takten des Schieberegisters mit einer Frequenz, die höher ist als die Datengeschwindigkeit, und mit einer Mehrheitslogik (16), deren Eingänge (16) mit jeweiligen Ausgängen der n Schieberegisterstufen verbunden sind, dadurch gekennzeichnet, daß die Mehrheitslogik (16) (n+1) Eingänge hat, und daß der (n+1). Eingang mit einer Rückkopplungsverbindung gekoppelt ist, die im Betrieb eine vorhergehende Mehrheitslogikentscheidung demselben zuführt.
5. Schaltungsanordnung nach Anspruch 4, dadurch gekennzeichnet, daß eine Verriegelungsschaltung (18) mit dem Ausgang der Mehrheitslogik (16) verbunden ist und durch die Taktmittel (14) getaktet wird.
6. Schaltungsanordnung nach Anspruch 5 dadurch gekennzeichnet, daß die Rückkopplungsverbindung mit einem Ausgang der Verriegelungsschaltung (18) verbunden ist.

