

CHANNEL BOUNDARY LOCATING METHOD, BASE STATION, AND USER EQUIPMENT

TECHNICAL FIELD

Embodiments of the present invention relate to the field of communications technologies, and
5 in particular, to a channel boundary locating method, a base station, and a user equipment.

BACKGROUND

When a universal mobile telecommunications system (Universal Mobile Telecommunications
System, UMTS for short) technology evolves to Release Rel-11, a multiflow transmission
(Multiflow) feature is introduced. This feature allows a plurality of intra-frequency or
10 inter-frequency cells to be configured as high-speed downlink shared channel (High-Speed
Downlink Shared Channel, HS-DSCH for short) serving cells of a user equipment (User Equipment,
UE for short), which obviously improves user experience. In UMTS Rel-7, a downlink
discontinuous reception (Discontinuous Reception, DRX for short) feature is introduced, which can
allow a UE to receive downlink data in a discontinuous manner, thereby reducing power
15 consumption of the UE. In a case of the Multiflow, there may be certain timing differences between
downlink common channels of a plurality of intra-frequency HS-DSCH serving cells, which are
mainly caused by base station clock timing corresponding to the cells, timing offsets (T_{cell}) of the
cells, and timing differences (T_p) introduced by air interface transmission.

A timing relationship between HS-DSCH serving cells may specifically include a high speed
20 shared control channel (High Speed-Shared Control Channel, HS-SCCH for short), a high speed
physical downlink shared channel (High Speed-Physical Downlink Shared Channel, HS-PDSCH
for short), a high speed dedicated physical control channel (High Speed-Dedicated Physical Control
Channel, HS-DPCCH for short), and a fractional dedicated physical channel (Fractional Dedicated
Physical Channel, F-DPCH for short), where the HS-PDSCH is a channel for indicating HSDPA
25 data transmission; the HS-SCCH carries data indication information, for example, an identifier for
scheduling a UE; the HS-PDSCH carries specific data information; the HS-DPCCH carries
feedback indication information for downlink data, for example, a channel condition indication and
data reception feedback indication information; and the F-DPCH channel is a dedicated channel,
and is used for performing power control on a dedicated channel and performing control on data

transmit power of an uplink channel of a UE. These channels have fixed timing relationships. Seen from the perspective of a cell side, it is necessary to find a start point of the HS-DPCCH to receive uplink data; according to protocol specifications, a cell needs to find backwards, according to an HS-SCCH start point, an HS-DPCCH boundary that is closest to 1280 chips as a boundary.

5 Using a single frequency dual cell (Single Frequency Dual Cell, SF-DC for short) feature as an example, in a case of the SF-DC feature, there are two serving cells. There is a certain timing difference of cells between downlink common channels within the cells, and the two cells may belong to a same base station or different base stations. In the case of the SF-DC, a UE needs to receive data in two cells in the downlink direction, but only needs to perform sending in one cell, 10 and the other cell also needs to demodulate data (in an inter-base station SF-DC scenario). This requires a UE side to specify a matching relationship between subframes for receiving downlink data. The two cells of the UE may be separately defined as a time reference cell and a non-time reference cell, where timing of channels between the time reference cell and the UE is same as channel timing specified in Rel-5 HSDPA, and the other cell is the non-time reference cell. For 15 example, HS-SCCH S_DRX=0 in the time reference cell of the UE is matched with HS-SCCH S_DRX=0 in the non-time reference cell; then, after the UE receives data of the two subframes, the UE performs, in the time reference cell, feedback on the HS-DPCCH according to an existing timing rule, where there is a fixed timing relationship between the HS-DPCCH and the HS-SCCH. For the non-time reference cell, a boundary of the HS-DPCCH is also searched for according to a 20 protocol. However, because of the timing difference between the downlink common channels of the cells, an error may occur when the UE or the non-time reference cell searches for the boundary of the HS-DPCCH. Because the UE side receives HS-SCCH S_DRX=0 of the two cells at the same time and performs feedback through one HS-DPCCH, the UE or the non-time reference cell may incorrectly locate an HS-DPCCH boundary, which eventually affects downlink data transmission 25 performance.

SUMMARY

Embodiments of the present invention provide a channel boundary locating method, a base station, and a user equipment, so as to address a problem in the prior art that a non-time reference cell incorrectly locates an HS-DPCCH boundary, which eventually affects performance of downlink 30 data transmission.

According to a first aspect, an embodiment of the present invention provides a channel boundary locating method, including:

receiving, by a base station of non-time reference cell, cell timing information delivered

by a network side, where the cell timing information includes a non-time reference parameter, and the non-time reference parameter Non-time Reference corresponds to a smallest timing difference between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell;

calculating, by the base station of non-time reference cell, boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to the non-time reference parameter; and

acquiring, by the base station of non-time reference cell, boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

With reference to the first aspect, in a first implementation manner of the first aspect, the calculating boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to the non-time reference parameter includes:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor;$$

T_{TX_diff2} is equal to a smallest timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell; and

T_{TX_diff1} is equal to the Non-time Reference.

With reference to the first aspect, in a second implementation manner of the first aspect, the calculating boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to the non-time reference parameter includes:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH

subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840\text{chips} \leq \tau_{\text{DRX}} - T_0 - 7680 * \text{DRX_OFFSET} < 3840\text{chips}$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$\text{DRX_OFFSET is } \left\lfloor \frac{\frac{T_{\text{TX_diff2}}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{\text{TX_diff1}}}{2560} - 0.9}{3} \right\rfloor;$$

$T_{\text{TX_diff1}}$ is equal to the Non-time Reference; and

if $T_{\text{TX_diff3}}$ is less than or equal to 7680×1.5 , less than or equal to 7680×2 , or less than or equal to 7680×2.5 , $T_{\text{TX_diff2}}$ is equal to $T_{\text{TX_diff3}}$; and if $T_{\text{TX_diff3}}$ is greater than or equal to 7680×1.5 , greater than or equal to 7680×2 , or greater than or equal to 7680×2.5 , $T_{\text{TX_diff2}}$ is equal to $T_{\text{TX_diff3}} - 38400$, where

$T_{\text{TX_diff3}}$ is equal to a timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell, and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to $T_{\text{TX_diff3}}$ and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to the Non-time Reference are in a same HS-DPCCH subframe.

With reference to the first aspect, in a third implementation manner of the first aspect, the calculating boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to the non-time reference parameter includes:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840\text{chips} \leq \tau_{\text{DRX}} - T_0 - 7680 * \text{DRX_OFFSET} < 3840\text{chips}$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor; \text{ and}$$

if T_{TX_diff3} is less than or equal to 7680×1.5 , less than or equal to 7680×2 , or less than or equal to 7680×2.5 , T_{TX_diff2} is equal to T_{TX_diff3} , and T_{TX_diff1} is equal to the Non-time Reference; and if T_{TX_diff3} is greater than or equal to 7680×1.5 , greater than or equal to 7680×2 , or greater than or equal to 7680×2.5 , T_{TX_diff2} is equal to a smallest timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell, and T_{TX_diff1} is equal to the Non-time Reference plus 7680, where

T_{TX_diff3} is a timing difference between the downlink F-DPCH frame of non-time reference cell and the HS-PDSCH subframe of non-time reference cell, and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff3} and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to the Non-time Reference are in a same HS-DPCCH subframe.

With reference to any one of the first to third implementation manners of the first aspect, in a fourth implementation manner of the first aspect, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

when a UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is

closest in time to $1280 - |T_{TX_diff2} - T_{TX_diff1}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

With reference to any one of the first to third implementation manners of the first aspect, in a fifth implementation manner of the first aspect, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

5 when a UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 + |T_{TX_diff2} - T_{TX_diff1}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a
10 serial number of HS-DPCCH CFN_DRX.

With reference to any one of the first to third implementation manners of the first aspect, in a sixth implementation manner of the first aspect, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

determining boundary information of an HS-DPCCH subframe that is closest in time to
15 $1280 + T_{TX_diff1} - T_{TX_diff2}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

According to a second aspect, an embodiment of the present invention provides a channel
20 boundary locating method, including:

calculating, by a base station of non-time reference cell, boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference T_{TX_diff} between a downlink F-DPCH frame of non-time reference cell and an
25 HS-PDSCH subframe of non-time reference cell and a timing difference τ_{DIFF} between an HS-PDSCH subframe of time reference cell and the HS-PDSCH subframe of non-time reference cell; and

acquiring, by the base station of non-time reference cell, boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

30 With reference to the second aspect, in a first implementation manner of the second aspect, the calculating boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference T_{TX_diff} between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing

difference τ_{DIFF} between an HS-PDSCH subframe of time reference cell and the HS-PDSCH subframe of non-time reference cell includes:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

when a user equipment (UE) is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, DRX_OFFSET is

$$\begin{aligned}
 & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} - \tau_{DIFF}}{2560} - 0.9}{3} \right\rfloor, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} - \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9}{3} \right\rfloor, \\
 & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} - \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9}{3} \right\rfloor, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} - \text{round}\left(\frac{\tau_{DIFF}}{256}\right) \times 256}{2560} - 0.9}{3} \right\rfloor, \\
 & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} - \frac{\tau_{DIFF}}{256} \times 256}{2560} - 0.9}{3} \right\rfloor, \quad \text{or}
 \end{aligned}$$

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\left\lfloor \frac{T_{TX_diff} - \frac{\tau_{DIFF}}{256}}{2560} \right\rfloor \times 256 - 0.9}{3} \right\rfloor ; \text{ or}$$

when a user equipment (UE) is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, DRX_OFFSET is

$$\begin{aligned} & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} + \tau_{DIFF}}{2560} - 0.9}{3} \right\rfloor , \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256 - 0.9}{2560} - 0.9 \right\rfloor , \\ 5 \quad & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256 - 0.9}{2560} - 0.9 \right\rfloor , \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \text{round}\left(\frac{\tau_{DIFF}}{256}\right) \times 256 - 0.9}{2560} - 0.9 \right\rfloor , \\ & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\left\lfloor \frac{T_{TX_diff} + \frac{\tau_{DIFF}}{256}}{2560} \right\rfloor \times 256 - 0.9}{2560} - 0.9 \right\rfloor , \quad \text{or} \\ & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\left\lfloor \frac{T_{TX_diff} + \frac{\tau_{DIFF}}{256}}{2560} \right\rfloor \times 256 - 0.9}{2560} - 0.9 \right\rfloor . \end{aligned}$$

With reference to the second aspect or the first implementation manner of the second aspect, in a second implementation manner of the second aspect, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

when the UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 - \tau_{DIFF}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is,

HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

With reference to the second aspect or the first implementation manner of the second aspect, in a third implementation manner of the second aspect, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 + \tau_{DIFF}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

According to a third aspect, an embodiment of the present invention provides a channel boundary locating method, including:

calculating, by a base station of non-time reference cell, boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference $T_{TX_diff,B}$ between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference $T_{TX_diff,A}$ between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell; and

acquiring, by the base station of non-time reference cell, boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

With reference to the third aspect, in a first implementation manner of the third aspect, the calculating boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference $T_{TX_diff,B}$ between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference $T_{TX_diff,A}$ between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell includes:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and

T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$\text{DRX_OFFSET is } \left\lfloor \frac{\frac{T_{TX_diff,B}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff,A}}{2560} - 0.9}{3} \right\rfloor; \text{ a hybrid automatic retransmission}$$

request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to $T_{TX_diff,B}$ and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to $T_{TX_diff,A}$ are in a same HS-DPCCH subframe; and $|T_{TX_diff,B} - T_{TX_diff,A}| < 7680$ or $|T_{TX_diff,B} - T_{TX_diff,A}| \leq 3840$.

With reference to the third aspect or the first implementation manner of the third aspect, in a second implementation manner of the third aspect, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

when a user equipment (UE) is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 - |T_{TX_diff,B} - T_{TX_diff,A}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

With reference to the third aspect or the first implementation manner of the third aspect, in a third implementation manner of the third aspect, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

when a user equipment (UE) is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 + |T_{TX_diff,B} - T_{TX_diff,A}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH

CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

With reference to the third aspect or the first implementation manner of the third aspect, in a third implementation manner of the third aspect, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 + T_{TX_diff,A} - T_{TX_diff,B}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

According to a fourth aspect, an embodiment of the present invention provides a channel boundary locating method, including:

calculating, by a user equipment (UE), boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a smallest timing difference between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell; and

acquiring, by the UE, boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

With reference to the fourth aspect, in a first implementation manner of the fourth aspect, the calculating boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a smallest timing difference between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell includes:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor;$$

T_{TX_diff2} is equal to a smallest timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell; and

T_{TX_diff1} is equal to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell.

With reference to the fourth aspect, in a second implementation manner of the fourth aspect, the calculating boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a smallest timing difference between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell includes:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor;$$

T_{TX_diff1} is equal to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell; and

if T_{TX_diff3} is less than or equal to 7680×1.5 , less than or equal to 7680×2 , or less than or equal to 7680×2.5 , T_{TX_diff2} is equal to T_{TX_diff3} ; and if T_{TX_diff3} is greater than or equal to 7680×1.5 , greater than or equal to 7680×2 , or greater than or equal to 7680×2.5 , T_{TX_diff2} is equal to $T_{TX_diff3} - 38400$, where

T_{TX_diff3} is a timing difference between a downlink F-DPCH frame of non-time

reference cell and an HS-PDSCH subframe of non-time reference cell, and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff3} and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff1} are in a same HS-DPCCH subframe.

With reference to the fourth aspect, in a third implementation manner of the fourth aspect, the calculating boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a smallest timing difference between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell includes:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor; \text{ and}$$

if T_{TX_diff3} is less than or equal to 7680×1.5 , less than or equal to 7680×2 , or less than or equal to 7680×2.5 , T_{TX_diff2} is equal to T_{TX_diff3} , and T_{TX_diff1} is equal to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell; and if T_{TX_diff3} is greater than or equal to 7680×1.5 , greater than or equal to 7680×2 , or greater than or equal to 7680×2.5 , T_{TX_diff2} is equal to a smallest timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell, and T_{TX_diff1} is equal to 7680 plus the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell, where

T_{TX_diff3} is a timing difference between the downlink F-DPCH frame of non-time reference cell and the HS-PDSCH subframe of non-time reference cell, and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff3} and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell are in a same HS-DPCCH subframe.

With reference to any one of the first to third implementation manners of the fourth aspect, in a fourth implementation manner of the fourth aspect, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

when the UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 - |T_{TX_diff2} - T_{TX_diff1}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

With reference to any one of the first to third implementation manners of the third aspect, in a fifth implementation manner of the third aspect, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 + |T_{TX_diff2} - T_{TX_diff1}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

With reference to any implementation manner of the first to third implementation manners of the third aspect, in a sixth implementation manner of the third aspect, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

determining boundary information of an HS-DPCCH subframe that is closest in time to

1280+ $T_{TX_diff1}-T_{TX_diff2}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

5 According to a fifth aspect, an embodiment of the present invention provides a channel boundary locating method, including:

calculating, by a user equipment (UE), boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference T_{TX_diff} between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference τ_{DIFF} between an HS-PDSCH subframe of time reference cell and the HS-PDSCH subframe of non-time reference cell; and

acquiring, by the UE, boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

With reference to the fifth aspect, in a first implementation manner of the fifth aspect, the calculating boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference T_{TX_diff} between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference τ_{DIFF} between an HS-PDSCH subframe of time reference cell and the HS-PDSCH subframe of non-time reference cell includes:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

when the UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer

HARQ processing time, DRX_OFFSET is $\left\lfloor \frac{T_{TX_diff} - 0.9}{2560} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \tau_{DIFF} - 0.9}{2560} \right\rfloor$,

$$\left\lfloor \frac{T_{TX_diff} - 0.9}{2560} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256 - 0.9}{2560} \right\rfloor, \quad \left\lfloor \frac{T_{TX_diff} - 0.9}{2560} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \left\lceil \frac{\tau_{DIFF}}{256} \right\rceil \times 256 - 0.9}{2560} \right\rfloor,$$

$$\left\lfloor \frac{T_{TX_diff} - 0.9}{2560} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \text{round}\left(\frac{\tau_{DIFF}}{256}\right) \times 256 - 0.9}{2560} \right\rfloor, \quad \left\lfloor \frac{T_{TX_diff} - 0.9}{2560} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256 - 0.9}{2560} \right\rfloor, \text{ or}$$

$$\left\lfloor \frac{T_{TX_diff} - 0.9}{2560} \right\rfloor - \left\lfloor \frac{\left\lceil \frac{T_{TX_diff} - \tau_{DIFF}}{256} \right\rceil \times 256 - 0.9}{2560} \right\rfloor; \text{ or}$$

5 when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, DRX_OFFSET is

$$\left\lfloor \frac{T_{TX_diff} - 0.9}{2560} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \tau_{DIFF} - 0.9}{2560} \right\rfloor, \quad \left\lfloor \frac{T_{TX_diff} - 0.9}{2560} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256 - 0.9}{2560} \right\rfloor,$$

$$\left\lfloor \frac{T_{TX_diff} - 0.9}{2560} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \left\lceil \frac{\tau_{DIFF}}{256} \right\rceil \times 256 - 0.9}{2560} \right\rfloor, \quad \left\lfloor \frac{T_{TX_diff} - 0.9}{2560} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \text{round}\left(\frac{\tau_{DIFF}}{256}\right) \times 256 - 0.9}{2560} \right\rfloor,$$

$$\left\lfloor \frac{T_{TX_diff} - 0.9}{2560} \right\rfloor - \left\lfloor \frac{\left\lceil \frac{T_{TX_diff} + \tau_{DIFF}}{256} \right\rceil \times 256 - 0.9}{2560} \right\rfloor, \quad \text{or}$$

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\left\lceil \frac{T_{TX_diff} + \frac{\tau_{DIFF}}{256}}{1} \right\rceil \times 256}{2560} - 0.9 \right\rfloor.$$

With reference to the fifth aspect or the first implementation manner of the fifth aspect, in a second implementation manner of the fifth aspect, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

- 5 when the UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 - \tau_{DIFF}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is,
10 HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

With reference to the fifth aspect or the first implementation manner of the fifth aspect, in a third implementation manner of the fifth aspect, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

- 15 when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 + \tau_{DIFF}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of
20 HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

According to a sixth aspect, an embodiment of the present invention provides a channel boundary locating method, including:

- calculating, by a user equipment (UE), boundary information HS-SCCH CFN_DRX n of
25 a high speed shared control channel (HS-SCCH) according to a timing difference $T_{TX_diff,B}$ between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference $T_{TX_diff,A}$ between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell; and

acquiring, by the UE, boundary information of a high speed dedicated physical control

channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

With reference to the sixth aspect, in a first possible implementation manner of the sixth aspect, the calculating boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference $T_{TX_diff,B}$ between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference $T_{TX_diff,A}$ between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell includes:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and T_0 is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff,B}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff,A}}{2560} - 0.9}{3} \right\rfloor; \text{ a hybrid automatic retransmission}$$

request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to $T_{TX_diff,B}$ and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to $T_{TX_diff,A}$ are in a same HS-DPCCH subframe; and $|T_{TX_diff,B} - T_{TX_diff,A}| < 7680$ or $|T_{TX_diff,B} - T_{TX_diff,A}| \leq 3840$.

With reference to the sixth aspect or the first possible implementation manner of the sixth aspect, in a second possible implementation manner of the sixth aspect, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

when the UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 - |T_{TX_diff,B} - T_{TX_diff,A}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the

HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

With reference to the sixth aspect or the first possible implementation manner of the sixth aspect, in a third possible implementation manner of the sixth aspect, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH

subframe that is closest in time to $1280 + |T_{TX_diff,B} - T_{TX_diff,A}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

With reference to the sixth aspect or the first possible implementation manner of the sixth aspect, in a fourth possible implementation manner of the sixth aspect, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 + T_{TX_diff,A} - T_{TX_diff,B}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

According to a seventh aspect, an embodiment of the present invention provides a base station, including:

a receiving module, configured to receive cell timing information delivered by a network side, where the cell timing information includes a non-time reference parameter, and the non-time reference parameter Non-time Reference corresponds to a smallest timing difference between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell; and

a processing module, configured to calculate boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to the non-time reference parameter, where:

the processing module is further configured to acquire boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

With reference to the seventh aspect, in a first implementation manner of the seventh aspect, the processing module is further configured to:

- align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840\text{chips} \leq \tau_{\text{DRX}} - T_0 - 7680 * \text{DRX_OFFSET} < 3840\text{chips}$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$\text{DRX_OFFSET is } \left\lfloor \frac{\frac{T_{\text{TX_diff2}}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{\text{TX_diff1}}}{2560} - 0.9}{3} \right\rfloor;$$

$T_{\text{TX_diff2}}$ is equal to a smallest timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell; and

- $T_{\text{TX_diff1}}$ is equal to the Non-time Reference.

With reference to the seventh aspect, in a second implementation manner of the seventh aspect, the processing module is further configured to:

- align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840\text{chips} \leq \tau_{\text{DRX}} - T_0 - 7680 * \text{DRX_OFFSET} < 3840\text{chips}$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$\text{DRX_OFFSET is } \left\lfloor \frac{\frac{T_{\text{TX_diff2}}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{\text{TX_diff1}}}{2560} - 0.9}{3} \right\rfloor;$$

T_{TX_diff1} is equal to the Non-time Reference; and

if T_{TX_diff3} is less than or equal to 7680×1.5 , less than or equal to 7680×2 , or less than or equal to 7680×2.5 , T_{TX_diff2} is equal to T_{TX_diff3} ; and if T_{TX_diff3} is greater than or equal to 7680×1.5 , greater than or equal to 7680×2 , or greater than or equal to 7680×2.5 , T_{TX_diff2} is equal to $T_{TX_diff3} - 38400$, where

T_{TX_diff3} is equal to a timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell, and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff3} and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to the Non-time Reference are in a same HS-DPCCH subframe.

With reference to the seventh aspect, in a third implementation manner of the seventh aspect, the processing module is further configured to:

align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor; \text{ and}$$

if T_{TX_diff3} is less than or equal to 7680×1.5 , less than or equal to 7680×2 , or less than or equal to 7680×2.5 , T_{TX_diff2} is equal to T_{TX_diff3} , and T_{TX_diff1} is equal to the Non-time Reference; and if T_{TX_diff3} is greater than or equal to 7680×1.5 , greater than or equal to 7680×2 , or greater than or equal to 7680×2.5 , T_{TX_diff2} is equal to a smallest timing difference between a

downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell, and T_{TX_diff1} is equal to the Non-time Reference plus 7680, where

T_{TX_diff3} is a timing difference between the downlink F-DPCH frame of non-time reference cell and the HS-PDSCH subframe of non-time reference cell, and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff3} and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to the Non-time Reference are in a same HS-DPCCH subframe.

With reference to any one of the first to third implementation manners of the seventh aspect, in a fourth implementation manner of the seventh aspect, the processing module is further configured to:

when a UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 - |T_{TX_diff2} - T_{TX_diff1}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

With reference to any one of the first to third implementation manners of the seventh aspect, in a fifth implementation manner of the seventh aspect, the processing module is further configured to:

when a UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 + |T_{TX_diff2} - T_{TX_diff1}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

With reference to any one of the first to third implementation manners of the seventh aspect, in a sixth implementation manner of the seventh aspect, the processing module is further configured to:

determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 + T_{TX_diff1} - T_{TX_diff2}$ chips after the start time of the boundary information of the HS-SCCH,

that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

According to an eighth aspect, an embodiment of the present invention provides a base station,
5 including:

a preprocessing module, configured to calculate boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference T_{TX_diff} between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference τ_{DIFF} between an HS-PDSCH subframe of time reference cell and the HS-PDSCH subframe of non-time reference cell; and
10

a processing module, configured to acquire boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

With reference to the eighth aspect, in a first implementation manner of the eighth aspect, the
15 preprocessing module is further configured to:

align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, where

20 CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

25 when a user equipment (UE) is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, DRX_OFFSET is

$$\left\lfloor \frac{T_{TX_diff}}{2560} - 0.9 \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \tau_{DIFF}}{2560} - 0.9 \right\rfloor, \quad \left\lfloor \frac{T_{TX_diff}}{2560} - 0.9 \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor,$$

$$\begin{aligned}
& \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} - \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560}}{3} - 0.9 \right\rfloor, & \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} - \text{round}\left(\frac{\tau_{DIFF}}{256}\right) \times 256}{2560}}{3} - 0.9 \right\rfloor, \\
& \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{\left\lfloor \frac{T_{TX_diff} - \frac{\tau_{DIFF}}{256}}{256} \right\rfloor \times 256}{2560}}{3} - 0.9 \right\rfloor, & \text{or} \\
& \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{\left\lceil \frac{T_{TX_diff} - \frac{\tau_{DIFF}}{256}}{256} \right\rceil \times 256}{2560}}{3} - 0.9 \right\rfloor; \text{ or}
\end{aligned}$$

when a user equipment (UE) is configured in multiple-input multiple-output mode and
5 the UE indicates requiring a longer HARQ processing time, DRX_OFFSET is

$$\begin{aligned}
& \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} + \tau_{DIFF} - 0.9}{2560}}{3} \right\rfloor, & \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} + \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560}}{3} - 0.9 \right\rfloor, \\
& \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} + \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560}}{3} - 0.9 \right\rfloor, & \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} + \text{round}\left(\frac{\tau_{DIFF}}{256}\right) \times 256}{2560}}{3} - 0.9 \right\rfloor, \\
& \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{\left\lceil \frac{T_{TX_diff} + \frac{\tau_{DIFF}}{256}}{256} \right\rceil \times 256}{2560}}{3} - 0.9 \right\rfloor, & \text{or}
\end{aligned}$$

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\left\lceil \frac{T_{TX_diff} + \frac{\tau_{DIFF}}{256}}{2560} \right\rceil \times 256 - 0.9}{3} \right\rfloor$$

With reference to the eighth aspect or the first implementation manner of the eighth aspect, in a second implementation manner of the eighth aspect, the processing module is further configured to:

- when the UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 - \tau_{DIFF}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

With reference to the eighth aspect or the first implementation manner of the eighth aspect, in a third implementation manner of the eighth aspect, the processing module is further configured to:

- when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 + \tau_{DIFF}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

- According to a ninth aspect, an embodiment of the present invention provides a base station, including:

- a preprocessing module, configured to calculate boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference $T_{TX_diff,B}$ between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference $T_{TX_diff,A}$ between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell; and

a processing module, configured to acquire boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

With reference to the ninth aspect, in a first implementation manner of the ninth aspect, the preprocessing module is further configured to:

- align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840\text{chips} \leq \tau_{\text{DRX}} - T_0 - 7680 * \text{DRX_OFFSET} < 3840\text{chips}$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

DRX_OFFSET is $\left\lfloor \frac{\frac{T_{\text{TX_diff},B}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{\text{TX_diff},A}}{2560} - 0.9}{3} \right\rfloor$; a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to $T_{\text{TX_diff},B}$ and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to $T_{\text{TX_diff},A}$ are in a same HS-DPCCH subframe; and $|T_{\text{TX_diff},B} - T_{\text{TX_diff},A}| < 7680$ or $|T_{\text{TX_diff},B} - T_{\text{TX_diff},A}| \leq 3840$.

With reference to the ninth aspect or the first implementation manner of the ninth aspect, in a second implementation manner of the ninth aspect, the processing module is further configured to:

- when a user equipment (UE) is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 - |T_{\text{TX_diff},B} - T_{\text{TX_diff},A}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

With reference to the ninth aspect or the first implementation manner of the ninth aspect, in a third implementation manner of the ninth aspect, the processing module is further configured to:

when a user equipment (UE) is configured in multiple-input multiple-output mode and

the UE indicates requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 + \left| T_{TX_diff,B} - T_{TX_diff,A} \right|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

With reference to the ninth aspect or the first implementation manner of the ninth aspect, in a fourth implementation manner of the ninth aspect, the processing module is further configured to:

determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 + T_{TX_diff,A} - T_{TX_diff,B}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

According to a tenth aspect, an embodiment of the present invention provides a user equipment (UE), including:

a preprocessing module, configured to calculate boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a smallest timing difference between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell; and

a processing module, configured to acquire boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

With reference to the tenth aspect, in a first implementation manner of the tenth aspect, the preprocessing module is further configured to:

align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n

and F-DPCH CFN n, where

$$\text{DRX_OFFSET is } \left\lfloor \frac{\frac{T_{TX_diff2} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1} - 0.9}{2560}}{3} \right\rfloor;$$

T_{TX_diff2} is equal to a smallest timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell; and

- 5 T_{TX_diff1} is equal to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell.

With reference to the tenth aspect, in a second implementation manner of the tenth aspect, the preprocessing module is further configured to:

- align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe,
10 where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840\text{chips} \leq \tau_{\text{DRX}} - T_0 - 7680 * \text{DRX_OFFSET} < 3840\text{chips}$, and T_0 is 1024 chips, where

- CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of
15 an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$\text{DRX_OFFSET is } \left\lfloor \frac{\frac{T_{TX_diff2} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1} - 0.9}{2560}}{3} \right\rfloor;$$

- T_{TX_diff1} is equal to the smallest timing difference between the downlink F-DPCH frame
20 of time reference cell and the HS-PDSCH subframe of time reference cell; and

if T_{TX_diff3} is less than or equal to 7680×1.5 , less than or equal to 7680×2 , or less than or equal to 7680×2.5 , T_{TX_diff2} is equal to T_{TX_diff3} ; and if T_{TX_diff3} is greater than or equal to 7680×1.5 , greater than or equal to 7680×2 , or greater than or equal to 7680×2.5 , T_{TX_diff2} is equal to $T_{TX_diff3} - 38400$, where

- 25 T_{TX_diff3} is a timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell, and a hybrid automatic

retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff3} and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff1} are in a same HS-DPCCH subframe.

5 With reference to the tenth aspect, in a third implementation manner of the tenth aspect, the preprocessing module is further configured to:

align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe,

where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is

10 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor; \text{ and}$$

if T_{TX_diff3} is less than or equal to 7680×1.5 , less than or equal to 7680×2 , or less than or equal to 7680×2.5 , T_{TX_diff2} is equal to T_{TX_diff3} , and T_{TX_diff1} is equal to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell; and if T_{TX_diff3} is greater than or equal to 7680×1.5 , greater than or equal to 7680×2 , or greater than or equal to 7680×2.5 , T_{TX_diff2} is equal to a smallest timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell, and T_{TX_diff1} is equal to 7680 plus the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell, where

T_{TX_diff3} is a timing difference between the downlink F-DPCH frame of non-time reference cell and the HS-PDSCH subframe of non-time reference cell, and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH

subframe corresponding to T_{TX_diff3} and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell are in a same HS-DPCCH subframe.

5 With reference to any one of the first to third implementation manners of the tenth aspect, in a fourth implementation manner of the seventh aspect, the processing module is further configured to:

when the UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest

10 in time to $1280 - |T_{TX_diff2} - T_{TX_diff1}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

15 With reference to any one of the first to third implementation manners of the tenth aspect, in a fifth implementation manner of the seventh aspect, the processing module is further configured to:

when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH

subframe that is closest in time to $1280 + |T_{TX_diff2} - T_{TX_diff1}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

25 With reference to any one of the first to third implementation manners of the tenth aspect, in a sixth implementation manner of the seventh aspect, the processing module is further configured to:

determine boundary information of an HS-DPCCH subframe that is closest in time to

$1280 + T_{TX_diff1} - T_{TX_diff2}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

30 According to an eleventh aspect, an embodiment of the present invention provides a user equipment (UE), including:

a preprocessing module, configured to calculate boundary information HS-SCCH

CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference T_{TX_diff} between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference τ_{DIFF} between an HS-PDSCH subframe of time reference cell and the HS-PDSCH subframe of non-time reference cell; and

5 a processing module, configured to acquire boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

With reference to the eleventh aspect, in a first implementation manner of the eleventh aspect, the preprocessing module is further configured to:

10 align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and
15 n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

when the UE is not configured in multiple-input multiple-output mode, or when the UE
20 is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer

$$\text{HARQ processing time, DRX_OFFSET is } \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} - \tau_{DIFF}}{2560} - 0.9}{3} \right\rfloor,$$

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} - \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9}{3} \right\rfloor, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} - \left\lceil \frac{\tau_{DIFF}}{256} \right\rceil \times 256}{2560} - 0.9}{3} \right\rfloor,$$

$$\left\lfloor \frac{T_{TX_diff} - 0.9}{2560} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \text{round}\left(\frac{\tau_{DIFF}}{256}\right) \times 256}{2560} - 0.9 \right\rfloor, \left\lfloor \frac{T_{TX_diff} - 0.9}{2560} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \frac{\tau_{DIFF}}{256} \times 256}{2560} - 0.9 \right\rfloor, \text{ or}$$

$$\left\lfloor \frac{T_{TX_diff} - 0.9}{2560} \right\rfloor - \left\lfloor \frac{\left\lfloor \frac{T_{TX_diff} - \tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor; \text{ or}$$

when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, DRX_OFFSET is

$$5 \left\lfloor \frac{T_{TX_diff} - 0.9}{2560} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \tau_{DIFF} - 0.9}{2560} \right\rfloor, \left\lfloor \frac{T_{TX_diff} - 0.9}{2560} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor,$$

$$\left\lfloor \frac{T_{TX_diff} - 0.9}{2560} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \left\lceil \frac{\tau_{DIFF}}{256} \right\rceil \times 256}{2560} - 0.9 \right\rfloor, \left\lfloor \frac{T_{TX_diff} - 0.9}{2560} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \text{round}\left(\frac{\tau_{DIFF}}{256}\right) \times 256}{2560} - 0.9 \right\rfloor,$$

$$\left\lfloor \frac{T_{TX_diff} - 0.9}{2560} \right\rfloor - \left\lfloor \frac{\left\lceil \frac{T_{TX_diff} + \tau_{DIFF}}{256} \right\rceil \times 256}{2560} - 0.9 \right\rfloor, \text{ or}$$

$$\left\lfloor \frac{T_{TX_diff} - 0.9}{2560} \right\rfloor - \left\lfloor \frac{\left\lceil \frac{T_{TX_diff} + \tau_{DIFF}}{256} \right\rceil \times 256}{2560} - 0.9 \right\rfloor.$$

With reference to the eleventh aspect or the first implementation manner of the eleventh aspect, in a second implementation manner of the eleventh aspect, the processing module is further configured to:

when the UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 - \tau_{DIFF}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

With reference to the eleventh aspect or the first implementation manner of the eleventh aspect, in a third implementation manner of the eleventh aspect, the processing module is further configured to:

when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 + \tau_{DIFF}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

According to a twelfth aspect, an embodiment of the present invention provides a user equipment (UE), including:

a preprocessing module, configured to calculate boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference $T_{TX_diff,B}$ between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference $T_{TX_diff,A}$ between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell; and

a processing module, configured to acquire boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

With reference to the twelfth aspect, in a first possible implementation manner of the twelfth aspect, the preprocessing module is further configured to:

align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is

1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$\text{DRX_OFFSET is } \left\lfloor \frac{\frac{T_{\text{TX_diff},B} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{\text{TX_diff},A} - 0.9}{2560}}{3} \right\rfloor; \text{ a hybrid automatic retransmission}$$

request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to $T_{\text{TX_diff},B}$ and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to $T_{\text{TX_diff},A}$ are in a same HS-DPCCH subframe, and $|T_{\text{TX_diff},B} - T_{\text{TX_diff},A}| < 7680$ or $|T_{\text{TX_diff},B} - T_{\text{TX_diff},A}| \leq 3840$.

With reference to the twelfth aspect or the first possible implementation manner of the twelfth aspect, in a second possible implementation manner of the twelfth aspect, the processing module is further configured to:

when the UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 - |T_{\text{TX_diff},B} - T_{\text{TX_diff},A}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

With reference to the twelfth aspect or the first possible implementation manner of the twelfth aspect, in a third possible implementation manner of the twelfth aspect, the processing module is further configured to:

when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 + |T_{\text{TX_diff},B} - T_{\text{TX_diff},A}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH

CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

With reference to the twelfth aspect or the first possible implementation manner of the twelfth aspect, in a fourth possible implementation manner of the twelfth aspect, the processing module is further configured to:

determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 + T_{TX_diff,A} - T_{TX_diff,B}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

According to a thirteenth aspect, an embodiment of the present invention provides a base station, including a memory and a processor, where the memory is connected to the processor; and the memory stores an execution instruction; and when the base station runs, the processor communicates with the memory, and the processor executes the execution instruction, so that the base station executes the method according to any one of the first aspect.

According to a fourteenth aspect, an embodiment of the present invention provides a user equipment (UE), including a memory and a processor, where the memory is connected to the processor; and

the memory stores an execution instruction; and when the base station runs, the processor communicates with the memory, and the processor executes the execution instruction, so that the base station executes the method according to any one of the second aspect and the third aspect.

According to the channel boundary locating method, the base station, and the user equipment provided in the embodiments of the present invention, a non-time reference cell receives cell timing information delivered by a network side, and adjusts an HS-DPCCH boundary of non-time reference cell, where the cell timing information includes a non-time reference parameter, and the non-time reference parameter corresponds to a smallest timing difference between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell. This implements that the non-time reference cell accurately locates the HS-DPCCH boundary, so that the non-time reference cell can learn correct data transmission feedback information and CQI information, which improves reliability of downlink data transmission, and resolves a problem in the prior art that a non-time reference cell incorrectly locates an HS-DPCCH boundary, which eventually affects performance of downlink data transmission.

BRIEF DESCRIPTION OF DRAWINGS

To describe the technical solutions in the embodiments of the present invention or in the prior art more clearly, the following briefly introduces the accompanying drawings required for describing the embodiments or the prior art. Apparently, the accompanying drawings in the following description show some embodiments of the present invention, and persons of ordinary skill in the art may still derive other drawings from these accompanying drawings without creative efforts.

FIG. 1 is a flowchart of Embodiment 1 of a channel boundary locating method according to the present invention;

10 FIG. 1A is a first schematic diagram of a timing difference in Embodiment 1 of a channel boundary locating method according to the present invention;

FIG. 1B is a second schematic diagram of a timing difference in Embodiment 1 of a channel boundary locating method according to the present invention;

15 FIG. 2 is a flowchart of Embodiment 2 of a channel boundary locating method according to the present invention;

FIG. 3 is a flowchart of Embodiment 3 of a channel boundary locating method according to the present invention;

FIG. 4 is a flowchart of Embodiment 4 of a channel boundary locating method according to the present invention;

20 FIG. 5 is a flowchart of Embodiment 4 of a channel boundary locating method according to the present invention;

FIG. 6 is a flowchart of Embodiment 4 of a channel boundary locating method according to the present invention;

25 FIG. 7 is a schematic structural diagram of Embodiment 1 of a base station according to the present invention;

FIG. 8 is a schematic structural diagram of Embodiment 2 of a base station according to the present invention;

FIG. 9 is a schematic structural diagram of Embodiment 1 of a user equipment (UE) according to the present invention;

30 FIG. 10 is a schematic structural diagram of Embodiment 3 of a base station according to the present invention; and

FIG. 11 is a schematic structural diagram of Embodiment 2 of a user equipment (UE) according to the present invention.

DESCRIPTION OF EMBODIMENTS

To make the objectives, technical solutions, and advantages of the embodiments of the present invention clearer, the following clearly and completely describes the technical solutions in the embodiments of the present invention with reference to the accompanying drawings in the
5 embodiments of the present invention. Apparently, the described embodiments are some but not all of the embodiments of the present invention. All other embodiments obtained by persons of ordinary skill in the art based on the embodiments of the present invention without creative efforts shall fall within the protection scope of the present invention.

It should be noted that " $\lceil \cdot \rceil$ " and " $\lfloor \cdot \rfloor$ " in the present invention are symbols denoting rounding up and
10 rounding down, respectively, and a function of round() denotes a function of rounding off.

FIG. 1 is a flowchart of Embodiment 1 of a channel boundary locating method according to the present invention. This embodiment is executed by a base station, where the base station may be a base station of non-time reference cell, and the base station may be implemented by using software and/or hardware. As shown in FIG. 1, the method according to this embodiment may include:

15 Step 101: A base station of non-time reference cell receives cell timing information delivered by a network side, where the cell timing information includes a non-time reference parameter, and the non-time reference parameter Non-time Reference corresponds to a smallest timing difference between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell.

20 Step 102: The base station of non-time reference cell calculates boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to the non-time reference parameter.

Step 103: The base station of non-time reference cell acquires boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of
25 the HS-SCCH.

Specifically, the base station of non-time reference cell receives the cell timing information delivered by the network side, where the cell timing information includes the non-time reference parameter Non-time Reference, and the Non-time Reference refers to the smallest timing difference, that is, smallest T_{TX_diff} , between the downlink F-DPCH frame of time reference cell and the
30 HS-PDSCH subframe of time reference cell; calculates the boundary information of the HS-SCCH according to the non-time reference parameter; and eventually obtains the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH.

Optionally, the calculating boundary information HS-SCCH CFN_DRX n of a high speed

shared control channel (HS-SCCH) according to the non-time reference parameter includes:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840 \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor;$$

T_{TX_diff2} is equal to a smallest timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell; and

T_{TX_diff1} is equal to the Non-time Reference.

Specifically, the boundary information, that is, HS-SCCH CFN_DRX n, of the HS-SCCH starts at the start time of the HS-SCCH subframe, where the HS-SCCH subframe is the HS-SCCH subframe behind τ_{DRX} chips after the start time of F-DPCH CFN n, τ_{DRX} meets $-3840 \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840$, and T_0 is 1024 chips, where

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor;$$

T_{TX_diff2} is equal to the smallest timing difference between the downlink F-DPCH frame of non-time reference cell and the HS-PDSCH subframe of non-time reference cell; and

T_{TX_diff1} is equal to the Non-time Reference.

Optionally, the calculating boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to the non-time reference parameter includes:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and

T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor ;$$

T_{TX_diff1} is equal to the Non-time Reference; and

if T_{TX_diff3} is less than or equal to 7680×1.5 , less than or equal to 7680×2 , or less than or equal to 7680×2.5 , T_{TX_diff2} is equal to T_{TX_diff3} ; and if T_{TX_diff3} is greater than or equal to 7680×1.5 , greater than or equal to 7680×2 , or greater than or equal to 7680×2.5 , T_{TX_diff2} is equal to $T_{TX_diff3} - 38400$, where

T_{TX_diff3} is equal to a timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell, and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff3} and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to the Non-time Reference are in a same HS-DPCCH subframe.

Specifically, the HS-PDSCH subframe corresponding to T_{TX_diff3} is the HS-PDSCH subframe that is used for calculating the timing difference between the downlink F-DPCH frame of non-time reference cell and the HS-PDSCH subframe of non-time reference cell, and the HARQ-ACK field corresponding to the HS-PDSCH subframe and the HARQ-ACK field corresponding to the HS-PDSCH subframe corresponding to the Non-time Reference are in the same HS-DPCCH subframe.

Optionally, the calculating boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to the non-time reference parameter includes:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0

is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2} - 0.9}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1} - 0.9}{2560} - 0.9}{3} \right\rfloor; \text{ and}$$

if T_{TX_diff3} is less than or equal to 7680×1.5 , less than or equal to 7680×2 , or less than or equal to 7680×2.5 , T_{TX_diff2} is equal to T_{TX_diff3} , and T_{TX_diff1} is equal to the Non-time Reference; and if T_{TX_diff3} is greater than or equal to 7680×1.5 , greater than or equal to 7680×2 , or greater than or equal to 7680×2.5 , T_{TX_diff2} is equal to a smallest timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell, and T_{TX_diff1} is equal to the Non-time Reference plus 7680, where

T_{TX_diff3} is a timing difference between the downlink F-DPCH frame of non-time reference cell and the HS-PDSCH subframe of non-time reference cell, and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff3} and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to the Non-time Reference are in a same HS-DPCCH subframe.

Optionally, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

when a UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 - |T_{TX_diff2} - T_{TX_diff1}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

Specifically, when the UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, the boundary information of the HS-DPCCH subframe that is closest in time to $1280 - |T_{TX_diff2} - T_{TX_diff1}|$ chips after the start time of HS-SCCH CFN_DRX n is determined as the boundary information of the HS-DPCCH; in this case, T_{TX_diff1} is less than T_{TX_diff2} .

It should be noted that if $1280 - |T_{TX_diff2} - T_{TX_diff1}|$ chips is a positive value, calculation is performed backwards from the start time of HS-SCCH CFN_DRX n; and if $1280 - |T_{TX_diff2} - T_{TX_diff1}|$ chips is a negative value, calculation is performed forwards from the start time of HS-SCCH CFN_DRX n.

Optionally, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

when a UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 + |T_{TX_diff2} - T_{TX_diff1}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

Specifically, when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, the boundary information of the HS-DPCCH subframe that is closest in time to $1280 + |T_{TX_diff2} - T_{TX_diff1}|$ chips after the start time of HS-SCCH CFN_DRX n is determined as the boundary information of the HS-DPCCH; in this case, T_{TX_diff1} is greater than T_{TX_diff2} .

Optionally, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 + T_{TX_diff1} - T_{TX_diff2}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH

CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

Specifically, because values of T_{TX_diff1} and T_{TX_diff2} are different depending on different modes in which the UE is configured and on whether a longer HARQ processing time is required, which mode the UE is configured in can be indicated without using an absolute value, that is, the boundary information of the HS-DPCCH subframe that is closest in time to $1280 + T_{TX_diff1} - T_{TX_diff2}$ chips after the start time of HS-SCCH CFN_DRX n can be directly determined as the boundary information of the HS-DPCCH.

In this embodiment of the present invention, DRX_OFFSET may be calculated by using the foregoing manners in either of cases in which F-DPCH frames of time reference cell and the non-time reference cell are aligned with each other and not aligned with each other. Therefore, accurate boundary information of an HS-SCCH may be obtained in either of the cases in which F-DPCH frames are aligned with each other and not aligned with each other, thereby obtaining accurate boundary information of an HS-DPCCH. FIG. 1A is a first schematic diagram of a timing difference in Embodiment 1 of the channel boundary locating method according to the present invention, and FIG. 1B is a second schematic diagram of a timing difference of Embodiment 1 of the channel boundary locating method according to the present invention. As shown in FIG. 1A, the F-DPCH frames of time reference cell and the non-time reference cell are aligned with each other. In the figure, HS-DPCCH 1 and F-DPCH 1 represent an HS-DPCCH and an F-DPCH of time reference cell, respectively; and HS-DPCCH 2 and F-DPCH 2 represent an HS-DPCCH and an F-DPCH of non-time reference cell, respectively.

As shown in FIG. 1A, $T_{TX_diff1} = T_{TX_diff2} \pm \tau_{DIFF}$, where τ_{DIFF} is a timing difference between matching HS-PDSCH subframes of time reference cell and the non-time reference cell;

$$\text{DRX_OFFSET is } \left\lfloor \frac{\frac{T_{TX_diff2} - 0.9}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1} - 0.9}{2560} - 0.9}{3} \right\rfloor; \text{ and boundary information of an}$$

HS-DPCCH that is closest in time to $1280 - |T_{TX_diff2} - T_{TX_diff1}|$ or $1280 + T_{TX_diff2} - T_{TX_diff1}$ chips after the start time of HS-SCCH CFN_DRX n is determined as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n.

As shown in FIG. 1B, the F-DPCH frames of time reference cell and the non-time reference cell are not aligned with each other. In the figure, HS-DPCCH 1 and F-DPCH 1 represent an HS-DPCCH and an F-DPCH of time reference cell, respectively; and HS-DPCCH 2 and F-DPCH 2 represent an HS-DPCCH and an F-DPCH of non-time reference cell, respectively.

$$T_{TX_diff1} = T_{TX_diff2} \pm \tau_{DIFF} + (\tau_{F-DPCH2} - \tau_{F-DPCH1}) \quad (1), \text{ where}$$

$\tau_{F-DPCH1}$ and $\tau_{F-DPCH2}$ represent timing of F-DPCHs of time reference cell and the non-time reference cell, respectively; and

$$\text{DRX_OFFSET is } \left\lfloor \frac{\frac{T_{TX_diff2} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1} - 0.9}{2560}}{3} \right\rfloor.$$

5 According to formula (1), it may be obtained that

$$\tau_{DIFF} = |T_{TX_diff2} - T_{TX_diff1} + \tau_{F-DPCH2} - \tau_{F-DPCH1}| \quad \text{because}$$

$$\begin{aligned} & |T_{TX_diff2} - T_{TX_diff1}| - |\tau_{F-DPCH2} - \tau_{F-DPCH1}| \leq |T_{TX_diff2} - T_{TX_diff1} + \tau_{F-DPCH2} - \tau_{F-DPCH1}| \leq \\ & |T_{TX_diff2} - T_{TX_diff1}| + |\tau_{F-DPCH2} - \tau_{F-DPCH1}| \end{aligned} ,$$

and a maximum value of $|\tau_{F-DPCH2} - \tau_{F-DPCH1}|$ is equal to 128 chips.

Therefore, $|T_{TX_diff2} - T_{TX_diff1}| - 128 \leq |T_{TX_diff2} - T_{TX_diff1} + \tau_{F-DPCH2} - \tau_{F-DPCH1}| \leq |T_{TX_diff2} - T_{TX_diff1}| + 128$, that is,

10 $|T_{TX_diff2} - T_{TX_diff1} + \tau_{F-DPCH2} - \tau_{F-DPCH1}|$ and $|T_{TX_diff2} - T_{TX_diff1}|$ are different by 128 chips at most, where 128 chips are much shorter than a length of half a subframe.

In practice, an accurate value of τ_{DIFF} cannot be obtained easily, and HS-DPCCH CFN_DRX is defined as "a subframe closest in time" in the description; therefore, $|T_{TX_diff2} - T_{TX_diff1}|$ may be used to replace τ_{DIFF} calculated according to formula (1). That is, $1280 - |T_{TX_diff2} - T_{TX_diff1}|$ or $1280 + |T_{TX_diff2} - T_{TX_diff1}|$ is used in HS-DPCCH CFN_DRX, so that no boundary error occurs, and fairly accurate boundary information of the HS-DPCCH can be obtained.

15 In this embodiment, a non-time reference cell receives cell timing information delivered by a network side, and adjusts an HS-DPCCH boundary of non-time reference cell, where the cell timing information includes a non-time reference parameter, and the non-time reference parameter corresponds to a smallest timing difference between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell. This implements that the non-time reference cell accurately locates the HS-DPCCH boundary, so that the non-time reference cell can learn correct data transmission feedback information and CQI information, which improves reliability of downlink data transmission, and resolves a problem in the prior art that a non-time reference cell incorrectly locates an HS-DPCCH boundary, which eventually affects performance of downlink data transmission.

FIG. 2 is a flowchart of Embodiment 2 of a channel boundary locating method according to the present invention. This embodiment is executed by a base station, where the base station may be a

base station of non-time reference cell, and the base station may be implemented by using software and/or hardware. As shown in FIG. 2, the method according to this embodiment may include:

Step 201: A base station of non-time reference cell calculates boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference T_{TX_diff} between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference τ_{DIFF} between an HS-PDSCH subframe of time reference cell and the HS-PDSCH subframe of non-time reference cell.

Step 202: The base station of non-time reference cell acquires boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

Optionally, the calculating boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference T_{TX_diff} between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference τ_{DIFF} between an HS-PDSCH subframe of time reference cell and the HS-PDSCH subframe of non-time reference cell includes:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

when a user equipment (UE) is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, DRX_OFFSET is

$$\left\lfloor \frac{T_{TX_diff}}{2560} - 0.9 \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \tau_{DIFF}}{2560} - 0.9 \right\rfloor, \quad \left\lfloor \frac{T_{TX_diff}}{2560} - 0.9 \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor,$$

$$\begin{aligned}
& \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor, & \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \text{round}\left(\frac{\tau_{DIFF}}{256}\right) \times 256}{2560} - 0.9 \right\rfloor, \\
& \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\left\lfloor \frac{T_{TX_diff} - \frac{\tau_{DIFF}}{256}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor, & \text{or} \\
& \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\left\lfloor \frac{T_{TX_diff} - \frac{\tau_{DIFF}}{256}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor; \text{ or}
\end{aligned}$$

when a user equipment (UE) is configured in multiple-input multiple-output mode and
5 the UE indicates requiring a longer HARQ processing time, DRX_OFFSET is

$$\begin{aligned}
& \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} + \tau_{DIFF} - 0.9}{2560}}{3} \right\rfloor, & \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor, \\
& \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor, & \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \text{round}\left(\frac{\tau_{DIFF}}{256}\right) \times 256}{2560} - 0.9 \right\rfloor, \\
& \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\left\lfloor \frac{T_{TX_diff} + \frac{\tau_{DIFF}}{256}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor, & \text{or}
\end{aligned}$$

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\left\lceil \frac{T_{TX_diff} + \frac{\tau_{DIFF}}{256}}{2560} \right\rceil \times 256 - 0.9}{3} \right\rfloor$$

Optionally, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

when the UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 - \tau_{DIFF}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

Optionally, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 + \tau_{DIFF}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

In this embodiment, an implementation principle and a technical effect are similar to those in Embodiment 1 of the method, which are not described repeatedly in this embodiment.

FIG. 3 is a flowchart of Embodiment 3 of a channel boundary locating method according to the present invention. This embodiment is executed by a base station, where the base station may be a base station of non-time reference cell, and the base station may be implemented by using software and/or hardware. As shown in FIG. 3, the method according to this embodiment may include:

Step 301: A base station of non-time reference cell calculates boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference $T_{TX_diff,B}$ between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference $T_{TX_diff,A}$ between a downlink

F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell.

Step 302: The base station of non-time reference cell acquires boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

5 Optionally, the calculating boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference $T_{TX_diff,B}$ between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference $T_{TX_diff,A}$ between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell includes:

10 aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and
 15 n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff,B}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff,A}}{2560} - 0.9}{3} \right\rfloor; \text{ a hybrid automatic retransmission}$$

20 request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to $T_{TX_diff,B}$ and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to $T_{TX_diff,A}$ are in a same HS-DPCCH subframe; and $|T_{TX_diff,B} - T_{TX_diff,A}| < 7680$ or $|T_{TX_diff,B} - T_{TX_diff,A}| \leq 3840$.

25 Optionally, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

when a user equipment (UE) is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 - |T_{TX_diff,B} - T_{TX_diff,A}|$ chips after the start time of the
 30 boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary

information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

Optionally, the acquiring the boundary information of the HS-DPCCH according to the
5 boundary information of the HS-SCCH includes:

when a user equipment (UE) is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 + |T_{TX_diff,B} - T_{TX_diff,A}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the
10 boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

Optionally, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

15 determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 + T_{TX_diff,A} - T_{TX_diff,B}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

20 In this embodiment, an implementation principle and a technical effect are similar to those in Embodiment 1 of the method, which are not described repeatedly in this embodiment.

FIG. 4 is a flowchart of Embodiment 4 of a channel boundary locating method according to the present invention. This embodiment is executed by a user equipment (UE), and the UE may be implemented by using software and/or hardware. As shown in FIG. 4, the method according to this
25 embodiment may include:

Step 401: A user equipment (UE) calculates boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a smallest timing difference between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell.

30 Step 402: The UE acquires boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

Optionally, the calculating boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a smallest timing difference between a downlink

F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell includes:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and

5 T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor;$$

T_{TX_diff2} is equal to a smallest timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell; and

T_{TX_diff1} is equal to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell.

Optionally, the calculating boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a smallest timing difference between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell includes:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and

T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor;$$

T_{TX_diff1} is equal to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell; and

if T_{TX_diff3} is less than or equal to 7680×1.5 , less than or equal to 7680×2 , or less than or equal to 7680×2.5 , T_{TX_diff2} is equal to T_{TX_diff3} ; and if T_{TX_diff3} is greater than or equal to 7680×1.5 , greater than or equal to 7680×2 , or greater than or equal to 7680×2.5 , T_{TX_diff2} is equal to $T_{TX_diff3} - 38400$, where

T_{TX_diff3} is a timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell, and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff3} and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff1} are in a same HS-DPCCH subframe.

Optionally, the calculating boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a smallest timing difference between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell includes:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor; \text{ and}$$

if T_{TX_diff3} is less than or equal to 7680×1.5 , less than or equal to 7680×2 , or less than or equal to 7680×2.5 , T_{TX_diff2} is equal to T_{TX_diff3} , and T_{TX_diff1} is equal to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH

subframe of time reference cell; and if T_{TX_diff3} is greater than or equal to 7680×1.5 , greater than or equal to 7680×2 , or greater than or equal to 7680×2.5 , T_{TX_diff2} is equal to a smallest timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell, and T_{TX_diff1} is equal to 7680 plus the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell, where

T_{TX_diff3} is a timing difference between the downlink F-DPCH frame of non-time reference cell and the HS-PDSCH subframe of non-time reference cell, and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff3} and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell are in a same HS-DPCCH subframe.

Optionally, the acquiring boundary information of a high speed dedicated physical control channel (HS-DPCCH) of non-time reference cell according to the boundary information of the HS-SCCH includes:

when the UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 - |T_{TX_diff2} - T_{TX_diff1}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

Optionally, the acquiring boundary information of a high speed dedicated physical control channel (HS-DPCCH) of a non-reference cell according to the boundary information of the HS-SCCH includes:

when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 + |T_{TX_diff2} - T_{TX_diff1}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary

information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

Optionally, the acquiring boundary information of a high speed dedicated physical control channel (HS-DPCCH) of a non-reference cell according to the boundary information of the HS-SCCH includes:

determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 + T_{TX_diff1} - T_{TX_diff2}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

In this embodiment, an implementation principle and a technical effect are similar to those in Embodiment 1 of the method, which are not described repeatedly in this embodiment.

FIG. 5 is a flowchart of Embodiment 5 of a channel boundary locating method according to the present invention. This embodiment is executed by a user equipment (UE), and the UE may be implemented by using software and/or hardware. As shown in FIG. 5, the method according to this embodiment may include:

Step 501: A user equipment (UE) calculates boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference T_{TX_diff} between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference τ_{DIFF} between a matching HS-PDSCH subframe of time reference cell and the HS-PDSCH subframe of non-time reference cell.

Step 502: The UE acquires boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

Optionally, the calculating boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference T_{TX_diff} between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference τ_{DIFF} between a matching HS-PDSCH subframe of time reference cell and the HS-PDSCH subframe of non-time reference cell includes:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and

T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n , where

when the UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer

HARQ processing time, DRX_OFFSET is $\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} - \tau_{DIFF}}{2560} - 0.9}{3} \right\rfloor$,

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \left\lceil \frac{\tau_{DIFF}}{256} \right\rceil \times 256}{2560} - 0.9 \right\rfloor,$$

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \text{round}\left(\frac{\tau_{DIFF}}{256}\right) \times 256}{2560} - 0.9 \right\rfloor, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor, \text{ or}$$

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\left\lceil \frac{T_{TX_diff} - \frac{\tau_{DIFF}}{256} \right\rceil \times 256}{2560} - 0.9 \right\rfloor; \text{ or}$$

when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, DRX_OFFSET is

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} + \tau_{DIFF}}{2560} - 0.9}{3} \right\rfloor, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor,$$

$$\begin{aligned}
& \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} + \left\lceil \frac{\tau_{DIFF}}{256} \right\rceil \times 256}{2560} - 0.9}{3} \right\rfloor, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} + \text{round}\left(\frac{\tau_{DIFF}}{256}\right) \times 256}{2560} - 0.9}{3} \right\rfloor, \\
& \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{\left\lfloor \frac{T_{TX_diff} + \frac{\tau_{DIFF}}{256}}{2560} \right\rfloor \times 256}{2560} - 0.9}{3} \right\rfloor, \quad \text{or} \\
& \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{\left\lceil \frac{T_{TX_diff} + \frac{\tau_{DIFF}}{256}}{2560} \right\rceil \times 256}{2560} - 0.9}{3} \right\rfloor.
\end{aligned}$$

Optionally, the acquiring the boundary information of the HS-DPCCH according to the
5 boundary information of the HS-SCCH includes:

when the UE is not configured in multiple-input multiple-output mode, or when the UE
is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer
HARQ processing time, determining boundary information of an HS-DPCCH subframe that is
closest in time to $1280 - \tau_{DIFF}$ chips after the start time of the boundary information of the
10 HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is,
HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH
CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

Optionally, the acquiring the boundary information of the HS-DPCCH according to the
boundary information of the HS-SCCH includes:

15 when the UE is configured in multiple-input multiple-output mode and the UE indicates
requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH
subframe that is closest in time to $1280 + \tau_{DIFF}$ chips after the start time of the boundary information
of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH,
that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of
20 HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH
CFN_DRX.

In this embodiment, an implementation principle and a technical effect are similar to those in

Embodiment 1 of the method, which are not described repeatedly in this embodiment.

FIG. 6 is a flowchart of Embodiment 5 of a channel boundary locating method according to the present invention. This embodiment is executed by a user equipment (UE), and the UE may be implemented by using software and/or hardware. As shown in FIG. 6, the method according to this
5 embodiment may include:

Step 601: A user equipment (UE) calculates boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference $T_{TX_diff,B}$ between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference $T_{TX_diff,A}$ between a downlink F-DPCH frame of
10 time reference cell and an HS-PDSCH subframe of time reference cell.

Step 602: The UE acquires boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

Optionally, the calculating boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference $T_{TX_diff,B}$ between a downlink
15 F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference $T_{TX_diff,A}$ between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell includes:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start
20 time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of
25 discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff,B} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff,A} - 0.9}{2560}}{3} \right\rfloor; \text{ a hybrid automatic retransmission}$$

request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to $T_{TX_diff,B}$ and a hybrid automatic retransmission request acknowledgement
30 (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to $T_{TX_diff,A}$ are in a

same HS-DPCCH subframe; and $|T_{TX_diff,B} - T_{TX_diff,A}| < 7680$ or $|T_{TX_diff,B} - T_{TX_diff,A}| \leq 3840$.

Optionally, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

when the UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 - |T_{TX_diff,B} - T_{TX_diff,A}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

Optionally, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 + |T_{TX_diff,B} - T_{TX_diff,A}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

Optionally, the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH includes:

determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 + T_{TX_diff,A} - T_{TX_diff,B}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

In this embodiment, an implementation principle and a technical effect are similar to those in Embodiment 1 of the method, which are not described repeatedly in this embodiment.

FIG. 7 is a schematic structural diagram of Embodiment 1 of a base station according to the present invention. As shown in FIG. 7, the base station 70 in this embodiment includes a receiving module 701 and a processing module 702, where the receiving module 701 is configured to receive cell timing information delivered by a network side, where the cell timing information includes a

non-time reference parameter, and the non-time reference parameter Non-time Reference corresponds to a smallest timing difference between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell; and the processing module 502 is configured to calculate boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to the non-time reference parameter, where the processing module 502 is further configured to acquire boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

Optionally, the processing module 702 is further configured to:

align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$\text{where } DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor;$$

T_{TX_diff2} is equal to a smallest timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell; and

T_{TX_diff1} is equal to the Non-time Reference.

Optionally, the processing module 702 is further configured to:

align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$\text{DRX_OFFSET is } \left\lfloor \frac{\frac{T_{TX_diff2} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1} - 0.9}{2560}}{3} \right\rfloor;$$

T_{TX_diff1} is equal to the Non-time Reference; and

if T_{TX_diff3} is less than or equal to 7680×1.5 , less than or equal to 7680×2 , or less than or equal to 7680×2.5 , T_{TX_diff2} is equal to T_{TX_diff3} ; and if T_{TX_diff3} is greater than or equal to 7680×1.5 , greater than or equal to 7680×2 , or greater than or equal to 7680×2.5 , T_{TX_diff2} is equal to $T_{TX_diff3} - 38400$, where

T_{TX_diff3} is equal to a timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell, and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff3} and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to the Non-time Reference are in a same HS-DPCCH subframe.

Optionally, the processing module 702 is further configured to:

align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * \text{DRX_OFFSET} < 3840chips$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$\text{DRX_OFFSET is } \left\lfloor \frac{\frac{T_{TX_diff2} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1} - 0.9}{2560}}{3} \right\rfloor; \text{ and}$$

if T_{TX_diff3} is less than or equal to 7680×1.5 , less than or equal to 7680×2 , or less than or equal to 7680×2.5 , T_{TX_diff2} is equal to T_{TX_diff3} , and T_{TX_diff1} is equal to the Non-time Reference; and if T_{TX_diff3} is greater than or equal to 7680×1.5 , greater than or equal to 7680×2 , or

greater than or equal to 7680×2.5 , T_{TX_diff2} is equal to a smallest timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell, and T_{TX_diff1} is equal to the Non-time Reference plus 7680, where

T_{TX_diff3} is a timing difference between the downlink F-DPCH frame of non-time reference cell and the HS-PDSCH subframe of non-time reference cell, and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff3} and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to the Non-time Reference are in a same HS-DPCCH subframe.

10 Optionally, the processing module 702 is further configured to:

when a UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest

in time to $1280 - |T_{TX_diff2} - T_{TX_diff1}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

Optionally, the processing module 702 is further configured to:

when a UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH

subframe that is closest in time to $1280 + |T_{TX_diff2} - T_{TX_diff1}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

Optionally, the processing module 702 is further configured to:

determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 + T_{TX_diff1} - T_{TX_diff2}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

The base station according to this embodiment may be used to implement a technical solution of the method embodiment shown in FIG. 1; implementation principles and technical effects thereof are similar, and details are not described repeatedly in this embodiment.

FIG. 8 is a schematic structural diagram of Embodiment 2 of a base station according to the present invention. As shown in FIG. 8, the base station 80 in this embodiment includes a preprocessing module 801 and a processing module 802, where the preprocessing module 801 is configured to calculate boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference T_{TX_diff} between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference τ_{DIFF} between an HS-PDSCH subframe of time reference cell and the HS-PDSCH subframe of non-time reference cell; and the processing module 802 is configured to acquire boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

Optionally, the preprocessing module 801 is further configured to:
align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

when a user equipment (UE) is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, DRX_OFFSET is

$$\left\lfloor \frac{T_{TX_diff}}{2560} - 0.9 \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \tau_{DIFF}}{2560} - 0.9 \right\rfloor, \quad \left\lfloor \frac{T_{TX_diff}}{2560} - 0.9 \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor,$$

$$\begin{aligned}
& \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor, & \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \text{round}\left(\frac{\tau_{DIFF}}{256}\right) \times 256}{2560} - 0.9 \right\rfloor, \\
& \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\left\lfloor T_{TX_diff} - \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor, & , \text{ or} \\
& \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\left\lceil T_{TX_diff} - \frac{\tau_{DIFF}}{256} \right\rceil \times 256}{2560} - 0.9 \right\rfloor; \text{ or}
\end{aligned}$$

when a user equipment (UE) is configured in multiple-input multiple-output mode and
5 the UE indicates requiring a longer HARQ processing time, DRX_OFFSET is

$$\begin{aligned}
& \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \tau_{DIFF} - 0.9}{2560} \right\rfloor, & \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor, \\
& \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \left\lceil \frac{\tau_{DIFF}}{256} \right\rceil \times 256}{2560} - 0.9 \right\rfloor, & \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \text{round}\left(\frac{\tau_{DIFF}}{256}\right) \times 256}{2560} - 0.9 \right\rfloor, \\
& \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\left\lfloor T_{TX_diff} + \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor, & , \text{ or}
\end{aligned}$$

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\left\lceil \frac{T_{TX_diff} + \frac{\tau_{DIFF}}{256}}{256} \right\rceil \times 256}{2560} - 0.9 \right\rfloor$$

Optionally, the processing module 802 is further configured to:

when the UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 - \tau_{DIFF}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

Optionally, the processing module 802 is further configured to:

when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 + \tau_{DIFF}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

Optionally, the preprocessing module 801 is configured to calculate boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference $T_{TX_diff,B}$ between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference $T_{TX_diff,A}$ between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell; and

the processing module 802 is configured to acquire boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

Optionally, the preprocessing module 801 is further configured to:

align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of

F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff,B} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff,A} - 0.9}{2560}}{3} \right\rfloor; \text{ a hybrid automatic retransmission}$$

request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to $T_{TX_diff,B}$ and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to $T_{TX_diff,A}$ are in a same HS-DPCCH subframe; and $|T_{TX_diff,B} - T_{TX_diff,A}| < 7680$ or $|T_{TX_diff,B} - T_{TX_diff,A}| \leq 3840$.

Optionally, the processing module 802 is further configured to:

when a user equipment (UE) is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 - |T_{TX_diff,B} - T_{TX_diff,A}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

Optionally, the processing module 802 is further configured to:

when a user equipment (UE) is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 + |T_{TX_diff,B} - T_{TX_diff,A}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

Optionally, the processing module 802 is further configured to:

determine boundary information of an HS-DPCCH subframe that is closest in time to
 1280+ $T_{TX_diff,A} - T_{TX_diff,B}$ chips after the start time of the boundary information of the HS-SCCH,
 that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is,
 HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH
 5 CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

The base station according to this embodiment may be used to implement a technical solution
 of the method embodiment shown in FIG. 2 or FIG. 3; implementation principles and technical
 effects thereof are similar, and details are not described repeatedly in this embodiment.

FIG. 9 is a schematic structural diagram of Embodiment 1 of a user equipment (UE) according
 10 to the present invention. As shown in FIG. 7, the UE 90 in this embodiment includes a
 preprocessing module 901 and a processing module 902, where the preprocessing module 901 is
 configured to calculate boundary information HS-SCCH CFN_DRX n of a high speed shared
 control channel (HS-SCCH) according to a smallest timing difference between a downlink F-DPCH
 frame of time reference cell and an HS-PDSCH subframe of time reference cell; and the processing
 15 module 902 is configured to acquire boundary information of a high speed dedicated physical
 control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

Optionally, the preprocessing module 901 is further configured to:

align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe,
 where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of
 20 F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is
 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and
 n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of
 an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of
 25 discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n
 and F-DPCH CFN n, where

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor;$$

T_{TX_diff2} is equal to a smallest timing difference between a downlink F-DPCH frame of
 non-time reference cell and an HS-PDSCH subframe of non-time reference cell; and

30 T_{TX_diff1} is equal to the smallest timing difference between the downlink F-DPCH frame
 of time reference cell and the HS-PDSCH subframe of time reference cell.

Optionally, the preprocessing module 901 is further configured to:

align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor;$$

T_{TX_diff1} is equal to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell; and

if T_{TX_diff3} is less than or equal to 7680×1.5 , less than or equal to 7680×2 , or less than or equal to 7680×2.5 , T_{TX_diff2} is equal to T_{TX_diff3} ; and if T_{TX_diff3} is greater than or equal to 7680×1.5 , greater than or equal to 7680×2 , or greater than or equal to 7680×2.5 , T_{TX_diff2} is equal to $T_{TX_diff3} - 38400$, where

T_{TX_diff3} is a timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell, and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff3} and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff1} are in a same HS-DPCCH subframe.

Optionally, the preprocessing module 901 is further configured to:

align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1} - 0.9}{2560}}{3} \right\rfloor; \text{ and}$$

if T_{TX_diff3} is less than or equal to 7680×1.5 , less than or equal to 7680×2 , or less than or equal to 7680×2.5 , T_{TX_diff2} is equal to T_{TX_diff3} , and T_{TX_diff1} is equal to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell; and if T_{TX_diff3} is greater than or equal to 7680×1.5 , greater than or equal to 7680×2 , or greater than or equal to 7680×2.5 , T_{TX_diff2} is equal to a smallest timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell, and T_{TX_diff1} is equal to 7680 plus the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell, where

T_{TX_diff3} is a timing difference between the downlink F-DPCH frame of non-time reference cell and the HS-PDSCH subframe of non-time reference cell, and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff3} and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell are in a same HS-DPCCH subframe.

Optionally, the processing module 902 is further configured to:

when the UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 - |T_{TX_diff2} - T_{TX_diff1}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH

CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

Optionally, the processing module 902 is further configured to:

when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH

5 subframe that is closest in time to $1280 + |T_{TX_diff2} - T_{TX_diff1}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

10 Optionally, the processing module 902 is further configured to:

determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 + T_{TX_diff1} - T_{TX_diff2}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH

15 CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

Optionally, the preprocessing module 901 is configured to calculate boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference T_{TX_diff} between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference τ_{DIFF} between a matching

20 HS-PDSCH subframe of time reference cell and the HS-PDSCH subframe of non-time reference cell; and

the processing module 902 is configured to acquire boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

25 Optionally, the preprocessing module 901 is further configured to:

align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, where

30 CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of

discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_{DRX n} and F-DPCH CFN_n, where

when the UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer

$$\begin{aligned}
 5 \quad \text{HARQ processing time, DRX_OFFSET is } & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} - \tau_{DIFF}}{2560} - 0.9}{3} \right\rfloor, \\
 & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \left\lceil \frac{\tau_{DIFF}}{256} \right\rceil \times 256}{2560} - 0.9 \right\rfloor, \\
 & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \text{round}\left(\frac{\tau_{DIFF}}{256}\right) \times 256}{2560} - 0.9 \right\rfloor, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor, \text{ or} \\
 & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\left\lceil \frac{T_{TX_diff} - \frac{\tau_{DIFF}}{256}}{256} \right\rceil \times 256}{2560} - 0.9 \right\rfloor; \text{ or}
 \end{aligned}$$

when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, DRX_OFFSET is

$$\begin{aligned}
 10 \quad \text{requiring a longer HARQ processing time, DRX_OFFSET is } & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} + \tau_{DIFF}}{2560} - 0.9}{3} \right\rfloor, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor, \\
 & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \left\lceil \frac{\tau_{DIFF}}{256} \right\rceil \times 256}{2560} - 0.9 \right\rfloor, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \text{round}\left(\frac{\tau_{DIFF}}{256}\right) \times 256}{2560} - 0.9 \right\rfloor,
 \end{aligned}$$

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\left\lfloor \frac{T_{TX_diff} + \frac{\tau_{DIFF}}{256}}{2560} \right\rfloor \times 256}{3} - 0.9 \right\rfloor, \quad \text{or}$$

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\left\lceil \frac{T_{TX_diff} + \frac{\tau_{DIFF}}{256}}{2560} \right\rceil \times 256}{3} - 0.9 \right\rfloor.$$

Optionally, the processing module 902 is further configured to:

- when the UE is not configured in multiple-input multiple-output mode, or when the UE
- 5 is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 - \tau_{DIFF}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and
- 10 n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

Optionally, the processing module 902 is further configured to:

- when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 + \tau_{DIFF}$ chips after the start time of the boundary information
- 15 of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

- Optionally, the preprocessing module 901 is configured to calculate boundary information
- 20 HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference $T_{TX_diff,B}$ between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference $T_{TX_diff,A}$ between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell;
- and

- 25 the processing module 902 is configured to acquire boundary information of a high

speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

Optionally, the preprocessing module 901 is further configured to:

align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe,
 5 where the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, where

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of
 10 an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, where

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff,B} - 0.9}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff,A} - 0.9}{2560} - 0.9}{3} \right\rfloor; \text{ a hybrid automatic retransmission}$$

request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe
 15 corresponding to $T_{TX_diff,B}$ and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to $T_{TX_diff,A}$ are in a same HS-DPCCH subframe; and $|T_{TX_diff,B} - T_{TX_diff,A}| < 7680$ or $|T_{TX_diff,B} - T_{TX_diff,A}| \leq 3840$.

Optionally, the processing module 902 is further configured to:

when the UE is not configured in multiple-input multiple-output mode, or when the UE
 20 is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 - |T_{TX_diff,B} - T_{TX_diff,A}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of
 25 HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

Optionally, the processing module 902 is further configured to:

when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH
 30 subframe that is closest in time to $1280 + |T_{TX_diff,B} - T_{TX_diff,A}|$ chips after the start time of the

boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

5 Optionally, the processing module 902 is further configured to:

 determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 + T_{TX_diff,A} - T_{TX_diff,B}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, where n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

10 The UE according to the embodiment may be used to implement technical solutions of the method embodiments shown in FIG. 4 to FIG. 6; implementation principles and technical effects thereof are similar, and details are not described repeatedly in this embodiment.

 FIG. 10 is a schematic structural diagram of Embodiment 3 of a base station according to the present invention. As shown in FIG. 10, the base station 100 provided in this embodiment includes a

15 memory 1001 and a processor 1002, where the memory 1001 is connected to the processor 1002.

 The memory 1001 stores an execution instruction; when the base station 100 runs, the processor 1002 communicates with the memory 1001, and the processor 1002 invokes the execution instruction in the memory 1001 to execute technical solutions in the method embodiments shown in

20 FIG. 1 to FIG. 3. Implementation principles and technical effects thereof are similar, and details are not described repeatedly in this embodiment.

 FIG. 11 is a schematic structural diagram of Embodiment 2 of a user equipment (UE) according to the present invention. As shown in FIG. 11, the UE 110 provided in this embodiment includes a memory 1101 and a processor 1102, where the memory 1101 is connected to the

25 processor 1102. The memory 1101 stores an execution instruction; when the UE 110 runs, the processor 1102 communicates with the memory 1101, and the processor 1102 invokes the execution instruction in the memory 1101 to execute technical solutions in the method embodiments shown in FIG. 4 to FIG. 6. Implementation principles and technical effects thereof are similar, and details are not described repeatedly in this embodiment.

30 In the several embodiments provided in the present application, it should be understood that the disclosed device and method may be implemented in other manners. For example, the described device embodiment is merely exemplary. For example, the unit or module division is merely logical function division and may be other division in actual implementation. For example, a plurality of units or modules may be combined or integrated into another system, or some features may be

ignored or not performed. In addition, the displayed or discussed mutual couplings or direct couplings or communication connections may be implemented through some interfaces. The indirect couplings or communication connections between the devices or modules may be implemented in electronic, mechanical, or other forms.

5 The modules described as separate parts may or may not be physically separate, and parts displayed as modules may or may not be physical modules, may be located in one position, or may be distributed on a plurality of network units. Some or all of the modules may be selected according to actual needs to achieve the objectives of the solutions of the embodiments.

10 Persons of ordinary skill in the art may understand that all or some of the steps of the method embodiments may be implemented by a program instructing relevant hardware. The program may be stored in a computer-readable storage medium. When the program runs, the steps of the method embodiments are performed. The foregoing storage medium includes: any medium that can store program code, such as a ROM, a RAM, a magnetic disc, or an optical disc.

15 Finally, it should be noted that the foregoing embodiments are merely intended for describing the technical solutions of the present invention, but not for limiting the present invention. Although the present invention is described in detail with reference to the foregoing embodiments, persons of ordinary skill in the art should understand that they may still make modifications to the technical solutions described in the foregoing embodiments or make equivalent replacements to some or all technical features thereof, without departing from the scope of the technical solutions of the
20 embodiments of the present invention.

CLAIMS

1. A channel boundary locating method, comprising:

receiving, by a base station of non-time reference cell, cell timing information delivered by a network side, wherein the cell timing information comprises a non-time reference parameter, and
 5 the non-time reference parameter Non-time Reference corresponds to a smallest timing difference between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell;

calculating, by the base station of non-time reference cell, boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to the non-time
 10 reference parameter; and

acquiring, by the base station of non-time reference cell, boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

2. The method according to claim 1, wherein the calculating the boundary information
 15 HS-SCCH CFN_DRX n of the HS-SCCH according to the non-time reference parameter further comprises:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, wherein the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and

20 T_0 is 1024 chips, wherein

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH
 25 CFN n, wherein

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor ;$$

T_{TX_diff2} is equal to a smallest timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell; and

T_{TX_diff1} is equal to the Non-time Reference.

3. The method according to claim 1, wherein the calculating the boundary information HS-SCCH CFN_DRX n of the HS-SCCH according to the non-time reference parameter further comprises:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe,
 5 wherein the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, wherein

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, wherein

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1} - 0.9}{2560}}{3} \right\rfloor;$$

T_{TX_diff1} is equal to the Non-time Reference; and

15 if T_{TX_diff3} is less than or equal to 7680×1.5 , less than or equal to 7680×2 , or less than or equal to 7680×2.5 , T_{TX_diff2} is equal to T_{TX_diff3} ; and if T_{TX_diff3} is greater than or equal to 7680×1.5 , greater than or equal to 7680×2 , or greater than or equal to 7680×2.5 , T_{TX_diff2} is equal to $T_{TX_diff3} - 38400$, wherein

T_{TX_diff3} is equal to a timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell, and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff3} and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to the Non-time Reference are in a same HS-DPCCH subframe.

25 4. The method according to claim 1, wherein the calculating the boundary information HS-SCCH CFN_DRX n of the HS-SCCH according to the non-time reference parameter further comprises:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, wherein the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of

F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, wherein

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, wherein

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor; \text{ and}$$

if T_{TX_diff3} is less than or equal to 7680×1.5 , less than or equal to 7680×2 , or less than or equal to 7680×2.5 , T_{TX_diff2} is equal to T_{TX_diff3} , and T_{TX_diff1} is equal to the Non-time Reference; and if T_{TX_diff3} is greater than or equal to 7680×1.5 , greater than or equal to 7680×2 , or greater than or equal to 7680×2.5 , T_{TX_diff2} is equal to a smallest timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell, and T_{TX_diff1} is equal to the Non-time Reference plus 7680, wherein

T_{TX_diff3} is a timing difference between the downlink F-DPCH frame of non-time reference cell and the HS-PDSCH subframe of non-time reference cell, and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff3} and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to the Non-time Reference are in a same HS-DPCCH subframe.

5. The method according to any one of claims 2 to 4, wherein the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH further comprises:

when a user equipment (UE) is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH

subframe that is closest in time to $1280 \cdot |T_{TX_diff2} - T_{TX_diff1}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH

CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

6. The method according to any one of claims 2 to 4, wherein the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH further comprises:

when a user equipment (UE) is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 + |T_{TX_diff2} - T_{TX_diff1}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

7. The method according to any one of claims 2 to 4, wherein the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH further comprises:

determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 + T_{TX_diff1} - T_{TX_diff2}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

8. A channel boundary locating method, comprising:

calculating, by a base station of non-time reference cell, boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference T_{TX_diff} between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference τ_{DIFF} between an HS-PDSCH subframe of time reference cell and the HS-PDSCH subframe of non-time reference cell; and

acquiring, by the base station of non-time reference cell, boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

9. The method according to claim 8, wherein the calculating the boundary information HS-SCCH CFN_DRX n of the HS-SCCH according to the timing difference T_{TX_diff} between the downlink F-DPCH frame of non-time reference cell and the HS-PDSCH subframe of non-time

reference cell and the timing difference τ_{DIFF} between the HS-PDSCH subframe of time reference cell and the HS-PDSCH subframe of non-time reference cell further comprises:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, wherein the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of

- 5 F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, wherein

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous
10 reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, wherein

when a user equipment (UE) is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, DRX_OFFSET is

$$\begin{aligned}
 & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} - \tau_{DIFF}}{2560} - 0.9}{3} \right\rfloor, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9}{3} \right\rfloor, \\
 & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9}{3} \right\rfloor, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \text{round}\left(\frac{\tau_{DIFF}}{256}\right) \times 256}{2560} - 0.9}{3} \right\rfloor, \\
 & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9}{3} \right\rfloor, \quad \text{or} \\
 & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\left\lfloor \frac{T_{TX_diff} - \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9}{3} \right\rfloor; \text{ or} \\
 & 77
 \end{aligned}$$

when a user equipment (UE) is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, DRX_OFFSET is

$$\begin{aligned}
 & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} + \tau_{DIFF}}{2560} - 0.9}{3} \right\rfloor, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} + \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9}{3} \right\rfloor, \\
 & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} + \left\lceil \frac{\tau_{DIFF}}{256} \right\rceil \times 256}{2560} - 0.9}{3} \right\rfloor, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} + \text{round}\left(\frac{\tau_{DIFF}}{256}\right) \times 256}{2560} - 0.9}{3} \right\rfloor, \\
 & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{\left\lfloor \frac{T_{TX_diff} + \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9}{3}} \right\rfloor, \quad \text{or} \\
 & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{\left\lceil \frac{T_{TX_diff} + \frac{\tau_{DIFF}}{256} \right\rceil \times 256}{2560} - 0.9}{3}} \right\rfloor.
 \end{aligned}$$

10. The method according to claim 8 or 9, wherein the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH further comprises:

when the UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 - \tau_{DIFF}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

11. The method according to claim 8 or 9, wherein the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH further comprises:

when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH

subframe that is closest in time to $1280 + \tau_{DIFF}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

12. A channel boundary locating method, comprising:

calculating, by a base station of non-time reference cell, boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference $T_{TX_diff,B}$ between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference $T_{TX_diff,A}$ between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell; and

acquiring, by the base station of non-time reference cell, boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

13. The method according to claim 12, wherein the calculating the boundary information HS-SCCH CFN_DRX n of the high speed shared control channel (HS-SCCH) according to the timing difference $T_{TX_diff,B}$ between the downlink F-DPCH frame of non-time reference cell and the HS-PDSCH subframe of non-time reference cell and the timing difference $T_{TX_diff,A}$ between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell comprises:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, wherein the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, wherein

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, wherein

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff,B} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff,A} - 0.9}{2560}}{3} \right\rfloor; \text{ a hybrid automatic retransmission request}$$

acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to $T_{TX_diff,B}$ and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to $T_{TX_diff,A}$ are in a same HS-DPCCH subframe; and $|T_{TX_diff,B} - T_{TX_diff,A}| < 7680$ or $|T_{TX_diff,B} - T_{TX_diff,A}| \leq 3840$.

5 14. The method according to claim 12 or 13, wherein the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH comprises:

when a user equipment (UE) is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH

10 subframe that is closest in time to $1280 - |T_{TX_diff,B} - T_{TX_diff,A}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

15 15. The method according to claim 12 or 13, wherein the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH comprises:

when a user equipment (UE) is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determining boundary information of an

20 HS-DPCCH subframe that is closest in time to $1280 + |T_{TX_diff,B} - T_{TX_diff,A}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

25 16. The method according to claim 12 or 13, wherein the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH comprises:

determining boundary information of an HS-DPCCH subframe that is closest in time to

30 $1280 + T_{TX_diff,A} - T_{TX_diff,B}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

17. A channel boundary locating method, comprising:

calculating, by a user equipment (UE), boundary information HS-SCCH CFN_DRX n of a

high speed shared control channel (HS-SCCH) according to a smallest timing difference between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell; and

acquiring, by the UE, boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

18. The method according to claim 17, wherein the calculating the boundary information HS-SCCH CFN_DRX n of the HS-SCCH according to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell comprises:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, wherein the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, wherein

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, wherein

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor;$$

T_{TX_diff2} is equal to a smallest timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell; and

T_{TX_diff1} is equal to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell.

19. The method according to claim 17, wherein the calculating the boundary information HS-SCCH CFN_DRX n of the HS-SCCH according to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell comprises:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, wherein the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and

T_0 is 1024 chips, wherein

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, wherein

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor;$$

T_{TX_diff1} is equal to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell; and

10 if T_{TX_diff3} is less than or equal to 7680×1.5 , less than or equal to 7680×2 , or less than or equal to 7680×2.5 , T_{TX_diff2} is equal to T_{TX_diff3} ; and if T_{TX_diff3} is greater than or equal to 7680×1.5 , greater than or equal to 7680×2 , or greater than or equal to 7680×2.5 , T_{TX_diff2} is equal to $T_{TX_diff3} - 38400$, wherein

15 T_{TX_diff3} is a timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell, and an HARQ-ACK field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff3} and an HARQ-ACK field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff1} are in a same HS-DPCCH subframe.

20 20. The method according to claim 17, wherein the calculating the boundary information HS-SCCH CFN_DRX n of the HS-SCCH) according to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell comprises:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, wherein the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and
25 T_0 is 1024 chips, wherein

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH

CFN n, wherein

$$\text{DRX_OFFSET is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor; \text{ and}$$

if T_{TX_diff3} is less than or equal to 7680×1.5 , less than or equal to 7680×2 , or less than or equal to 7680×2.5 , T_{TX_diff2} is equal to T_{TX_diff3} , and T_{TX_diff1} is equal to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell; and if T_{TX_diff3} is greater than or equal to 7680×1.5 , greater than or equal to 7680×2 , or greater than or equal to 7680×2.5 , T_{TX_diff2} is equal to a smallest timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell, and T_{TX_diff1} is equal to 7680 plus the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell, wherein

T_{TX_diff3} is a timing difference between the downlink F-DPCH frame of non-time reference cell and the HS-PDSCH subframe of non-time reference cell, and an HARQ-ACK field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff3} and an HARQ-ACK field corresponding to the HS-PDSCH subframe corresponding to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell are in a same HS-DPCCH subframe.

21. The method according to any one of claims 18 to 20, wherein the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH comprises:

when the UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 - |T_{TX_diff2} - T_{TX_diff1}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

22. The method according to any one of claims 18 to 20, wherein the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH comprises:

when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 + \left| T_{TX_diff\ 2} - T_{TX_diff\ 1} \right|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

23. The method according to any one of claims 18 to 20, wherein the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH comprises:

determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 + T_{TX_diff\ 1} - T_{TX_diff\ 2}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

24. A channel boundary locating method, comprising:

calculating, by a user equipment (UE), boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference T_{TX_diff} between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference τ_{DIFF} between an HS-PDSCH subframe of time reference cell and the HS-PDSCH subframe of non-time reference cell; and

acquiring, by the UE, boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

25. The method according to claim 24, wherein the calculating the boundary information HS-SCCH CFN_DRX n of the HS-SCCH according to the timing difference T_{TX_diff} between the downlink F-DPCH frame of non-time reference cell and the HS-PDSCH subframe of non-time reference cell and the timing difference τ_{DIFF} between the HS-PDSCH subframe of time reference cell and the HS-PDSCH subframe of non-time reference cell comprises:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, wherein the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, wherein

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in

CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, wherein

- 5 when the UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer

$$\begin{aligned} \text{HARQ processing time, DRX_OFFSET is } & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} - \tau_{DIFF}}{2560} - 0.9}{3} \right\rfloor, \\ & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \left\lceil \frac{\tau_{DIFF}}{256} \right\rceil \times 256}{2560} - 0.9 \right\rfloor, \\ & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \text{round}\left(\frac{\tau_{DIFF}}{256}\right) \times 256}{2560} - 0.9 \right\rfloor, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor, \text{ or} \\ & \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\left\lceil \frac{T_{TX_diff} - \frac{\tau_{DIFF}}{256}}{256} \right\rceil \times 256}{2560} - 0.9 \right\rfloor; \text{ or} \end{aligned}$$

10 when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, DRX_OFFSET is

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} + \tau_{DIFF}}{2560} - 0.9}{3} \right\rfloor, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor,$$

$$\begin{aligned}
& \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} + \left\lceil \frac{\tau_{DIFF}}{256} \right\rceil \times 256}{2560} - 0.9}{3} \right\rfloor, & \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} + \text{round}\left(\frac{\tau_{DIFF}}{256}\right) \times 256}{2560} - 0.9}{3} \right\rfloor, \\
& \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{\left\lfloor \frac{T_{TX_diff} + \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9}{3}} \right\rfloor, & \text{or} \\
& \left\lfloor \frac{\frac{T_{TX_diff} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{\left\lceil \frac{T_{TX_diff} + \frac{\tau_{DIFF}}{256} \right\rceil \times 256}{2560} - 0.9}{3}} \right\rfloor.
\end{aligned}$$

26. The method according to claim 24 or 25, wherein the acquiring the boundary information
5 of the HS-DPCCH according to the boundary information of the HS-SCCH comprises:

when the UE is not configured in multiple-input multiple-output mode, or when the UE is
configured in multiple-input multiple-output mode and the UE indicates not requiring a longer
HARQ processing time, determining boundary information of an HS-DPCCH subframe that is
closest in time to $1280 - \tau_{DIFF}$ chips after the start time of the boundary information of the
10 HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is,
HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH
CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

27. The method according to claim 24 or 25, wherein the acquiring the boundary information
of the HS-DPCCH according to the boundary information of the HS-SCCH comprises:

15 when the UE is configured in multiple-input multiple-output mode and the UE indicates
requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH
subframe that is closest in time to $1280 + \tau_{DIFF}$ chips after the start time of the boundary information
of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH,
that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of
20 HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH
CFN_DRX.

28. A channel boundary locating method, comprising:

calculating, by a user equipment (UE), boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference $T_{TX_diff,B}$ between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference $T_{TX_diff,A}$ between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell; and

acquiring, by the UE, boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

29. The method according to claim 28, wherein the calculating the boundary information HS-SCCH CFN_DRX n of the HS-SCCH according to the timing difference $T_{TX_diff,B}$ between the downlink F-DPCH frame of non-time reference cell and the HS-PDSCH subframe of non-time reference cell and the timing difference $T_{TX_diff,A}$ between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell comprises:

aligning a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, wherein the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, wherein

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, wherein

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff,B}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff,A}}{2560} - 0.9}{3} \right\rfloor; \text{ a hybrid automatic retransmission request}$$

acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to $T_{TX_diff,B}$ and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to $T_{TX_diff,A}$ are in a same HS-DPCCH subframe; and $|T_{TX_diff,B} - T_{TX_diff,A}| < 7680$ or $|T_{TX_diff,B} - T_{TX_diff,A}| \leq 3840$.

30. The method according to claim 28 or 29, wherein the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH comprises:

when the UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer

HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 - |T_{TX_diff,B} - T_{TX_diff,A}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

31. The method according to claim 28 or 29, wherein the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH comprises:

when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 + |T_{TX_diff,B} - T_{TX_diff,A}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

32. The method according to claim 28 or 29, wherein the acquiring the boundary information of the HS-DPCCH according to the boundary information of the HS-SCCH comprises:

determining boundary information of an HS-DPCCH subframe that is closest in time to $1280 + T_{TX_diff,A} - T_{TX_diff,B}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

33. A base station, comprising:

a receiving module, configured to receive cell timing information delivered by a network side, wherein the cell timing information comprises a non-time reference parameter, and the non-time reference parameter Non-time Reference corresponds to a smallest timing difference between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell; and

a processing module, configured to calculate boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to the non-time reference parameter, wherein:

the processing module is further configured to acquire boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the

HS-SCCH.

34. The base station according to claim 33, wherein the processing module is further configured to:

align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, wherein the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, wherein

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, wherein

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor;$$

T_{TX_diff2} is equal to a smallest timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell; and

T_{TX_diff1} is equal to the Non-time Reference.

35. The base station according to claim 33, wherein the processing module is further configured to:

align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, wherein the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, wherein

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, wherein

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor;$$

T_{TX_diff1} is equal to the Non-time Reference; and

if T_{TX_diff3} is less than or equal to 7680×1.5 , less than or equal to 7680×2 , or less than or equal to 7680×2.5 , T_{TX_diff2} is equal to T_{TX_diff3} ; and if T_{TX_diff3} is greater than or equal to 7680×1.5 , greater than or equal to 7680×2 , or greater than or equal to 7680×2.5 , T_{TX_diff2} is equal to $T_{TX_diff3} - 38400$, wherein

T_{TX_diff3} is equal to a timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell, and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff3} and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to the Non-time Reference are in a same HS-DPCCH subframe.

36. The base station according to claim 33, wherein the processing module is further configured to:

align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, wherein the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, wherein

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, wherein

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor; \text{ and}$$

if T_{TX_diff3} is less than or equal to 7680×1.5 , less than or equal to 7680×2 , or less than or equal to 7680×2.5 , T_{TX_diff2} is equal to T_{TX_diff3} , and T_{TX_diff1} is equal to the Non-time Reference; and if T_{TX_diff3} is greater than or equal to 7680×1.5 , greater than or equal to 7680×2 , or greater than or equal to 7680×2.5 , T_{TX_diff2} is equal to a smallest timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell,

and T_{TX_diff1} is equal to the Non-time Reference plus 7680, wherein

T_{TX_diff3} is a timing difference between the downlink F-DPCH frame of non-time reference cell and the HS-PDSCH subframe of non-time reference cell, and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe
5 corresponding to T_{TX_diff3} and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to the Non-time Reference are in a same HS-DPCCH subframe.

37. The base station according to any one of claims 34 to 36, wherein the processing module is further configured to:

10 when a user equipment (UE) is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 - |T_{TX_diff2} - T_{TX_diff1}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary
15 information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

38. The base station according to any one of claims 34 to 36, wherein the processing module is further configured to:

20 when a user equipment (UE) is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 + |T_{TX_diff2} - T_{TX_diff1}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in
25 HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

39. The base station according to any one of claims 34 to 36, wherein the processing module is further configured to:

determine boundary information of an HS-DPCCH subframe that is closest in time to
30 $1280 + T_{TX_diff1} - T_{TX_diff2}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH

CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

40. A base station, comprising:

a preprocessing module, configured to calculate boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference T_{TX_diff} between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference τ_{DIFF} between an HS-PDSCH subframe of time reference cell and the HS-PDSCH subframe of non-time reference cell; and

a processing module, configured to acquire boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

41. The base station according to claim 40, wherein the preprocessing module is further configured to:

align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, wherein the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and

T_0 is 1024 chips, wherein

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH

CFN n, wherein

when a user equipment (UE) is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, DRX_OFFSET is

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} - \tau_{DIFF}}{2560} - 0.9}{3} \right\rfloor, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} - \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9}{3} \right\rfloor,$$

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} - \left\lceil \frac{\tau_{DIFF}}{256} \right\rceil \times 256}{2560} - 0.9}{3} \right\rfloor, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} - \text{round}\left(\frac{\tau_{DIFF}}{256}\right) \times 256}{2560} - 0.9}{3} \right\rfloor,$$

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\left\lfloor \frac{T_{TX_diff} - \frac{\tau_{DIFF}}{256}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor$$

, or

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\left\lceil \frac{T_{TX_diff} - \frac{\tau_{DIFF}}{256}}{256} \right\rceil \times 256}{2560} - 0.9 \right\rfloor$$

; or

when a user equipment (UE) is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, DRX_OFFSET is

$$5 \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lceil \left\lfloor \frac{\frac{T_{TX_diff} + \tau_{DIFF}}{2560} - 0.9}{3} \right\rfloor \right\rceil, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor,$$

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \left\lceil \frac{\tau_{DIFF}}{256} \right\rceil \times 256}{2560} - 0.9 \right\rfloor,$$

,

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \text{round}\left(\frac{\tau_{DIFF}}{256}\right) \times 256}{2560} - 0.9 \right\rfloor,$$

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\left\lceil \frac{T_{TX_diff} + \frac{\tau_{DIFF}}{256}}{256} \right\rceil \times 256}{2560} - 0.9 \right\rfloor,$$

, or

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\left\lceil \frac{T_{TX_diff} + \frac{\tau_{DIFF}}{256}}{256} \right\rceil \times 256}{2560} - 0.9 \right\rfloor.$$

42. The base station according to claim 40 or 41, wherein the processing module is further configured to:

when the UE is not configured in multiple-input multiple-output mode, or when the UE is

configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 - \tau_{DIFF}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

43. The base station according to claim 40 or 41, wherein the processing module is further configured to:

when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 + \tau_{DIFF}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

44. A base station, comprising:

a preprocessing module, configured to calculate boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference $T_{TX_diff,B}$ between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference $T_{TX_diff,A}$ between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell; and

a processing module, configured to acquire boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

45. The base station according to claim 44, wherein the preprocessing module is further configured to:

align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, wherein the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, wherein

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH

CFN n, wherein

$$\text{DRX_OFFSET is } \left\lfloor \frac{\frac{T_{TX_diff,B} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff,A} - 0.9}{2560}}{3} \right\rfloor; \text{ a hybrid automatic retransmission request}$$

acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to $T_{TX_diff,B}$ and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field
 5 corresponding to the HS-PDSCH subframe corresponding to $T_{TX_diff,A}$ are in a same HS-DPCCH subframe; and $|T_{TX_diff,B} - T_{TX_diff,A}| < 7680$ or $|T_{TX_diff,B} - T_{TX_diff,A}| \leq 3840$.

46. The base station according to claim 44 or 45, wherein the processing module is further configured to:

when a user equipment (UE) is not configured in multiple-input multiple-output mode, or
 10 when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 - |T_{TX_diff,B} - T_{TX_diff,A}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH
 15 CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

47. The base station according to claim 44 or 45, wherein the processing module is further configured to:

when a user equipment (UE) is configured in multiple-input multiple-output mode and the UE
 20 indicates requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 + |T_{TX_diff,B} - T_{TX_diff,A}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH
 25 CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

48. The base station according to claim 44 or 45, wherein the processing module is further configured to:

determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 + T_{TX_diff,A} - T_{TX_diff,B}$ chips after the start time of the boundary information of the HS-SCCH,
 30 that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is,

HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

49. A user equipment (UE), comprising:

5 a preprocessing module, configured to calculate boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a smallest timing difference between a downlink F-DPCH frame of time reference cell and an HS-PDSCH subframe of time reference cell; and

a processing module, configured to acquire boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

10 50. The UE according to claim 49, wherein the preprocessing module is further configured to:

align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, wherein the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, wherein

15 CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, wherein

20
$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1}}{2560} - 0.9}{3} \right\rfloor;$$

T_{TX_diff2} is equal to a smallest timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell; and

T_{TX_diff1} is equal to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell.

25 51. The UE according to claim 49, wherein the preprocessing module is further configured to:

align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, wherein the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, wherein

30 CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in

CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, wherein

$$5 \quad DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff2} - 0.9}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1} - 0.9}{2560} - 0.9}{3} \right\rfloor;$$

T_{TX_diff1} is equal to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell; and

if T_{TX_diff3} is less than or equal to 7680×1.5 , less than or equal to 7680×2 , or less than or equal to 7680×2.5 , T_{TX_diff2} is equal to T_{TX_diff3} ; and if T_{TX_diff3} is greater than or equal to 7680×1.5 , greater than or equal to 7680×2 , or greater than or equal to 7680×2.5 , T_{TX_diff2} is equal to $T_{TX_diff3} - 38400$, wherein

T_{TX_diff3} is a timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell, and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff3} and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff1} are in a same HS-DPCCH subframe.

52. The UE according to claim 49, wherein the preprocessing module is further configured to:
align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe,
wherein the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, wherein

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, wherein

$$\text{DRX_OFFSET is } \left\lfloor \frac{\frac{T_{TX_diff2} - 0.9}{2560}}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff1} - 0.9}{2560}}{3} \right\rfloor; \text{ and}$$

if T_{TX_diff3} is less than or equal to 7680×1.5 , less than or equal to 7680×2 , or less than or equal to 7680×2.5 , T_{TX_diff2} is equal to T_{TX_diff3} , and T_{TX_diff1} is equal to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell; and if T_{TX_diff3} is greater than or equal to 7680×1.5 , greater than or equal to 7680×2 , or greater than or equal to 7680×2.5 , T_{TX_diff2} is equal to a smallest timing difference between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell, and T_{TX_diff1} is equal to 7680 plus the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell, wherein

T_{TX_diff3} is a timing difference between the downlink F-DPCH frame of non-time reference cell and the HS-PDSCH subframe of non-time reference cell, and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to T_{TX_diff3} and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to the smallest timing difference between the downlink F-DPCH frame of time reference cell and the HS-PDSCH subframe of time reference cell are in a same HS-DPCCH subframe.

53. The UE according to any one of claims 50 to 52, wherein the processing module is further configured to:

when the UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 - |T_{TX_diff2} - T_{TX_diff1}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

54. The UE according to any one of claims 50 to 52, wherein the processing module is further configured to:

when the UE is configured in multiple-input multiple-output mode and the UE indicates

requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 + \left| T_{TX_diff2} - T_{TX_diff1} \right|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

55. The UE according to any one of claims 50 to 52, wherein the processing module is further configured to:

determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 + T_{TX_diff1} - T_{TX_diff2}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

56. A user equipment (UE), comprising:

a preprocessing module, configured to calculate boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference T_{TX_diff} between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of non-time reference cell and a timing difference τ_{DIFF} between an HS-PDSCH subframe of time reference cell and the HS-PDSCH subframe of non-time reference cell; and

a processing module, configured to acquire boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

57. The UE according to claim 56, wherein the preprocessing module is further configured to:

align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, wherein the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, wherein

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, wherein

when the UE is not configured in multiple-input multiple-output mode, or when the UE is

configured in multiple-input multiple-output mode and the UE indicates not requiring a longer

HARQ processing time, DRX_OFFSET is $\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} - \tau_{DIFF}}{2560} - 0.9}{3} \right\rfloor$,

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \left\lceil \frac{\tau_{DIFF}}{256} \right\rceil \times 256}{2560} - 0.9 \right\rfloor,$$

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \text{round}\left(\frac{\tau_{DIFF}}{256}\right) \times 256}{2560} - 0.9 \right\rfloor, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} - \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor, \text{ or}$$

$$5 \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\left\lceil \frac{T_{TX_diff} - \frac{\tau_{DIFF}}{256}}{256} \right\rceil \times 256}{2560} - 0.9 \right\rfloor; \text{ or}$$

when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, DRX_OFFSET is

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff} + \tau_{DIFF}}{2560} - 0.9}{3} \right\rfloor, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \left\lfloor \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9 \right\rfloor,$$

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \left\lceil \frac{\tau_{DIFF}}{256} \right\rceil \times 256}{2560} - 0.9 \right\rfloor, \quad \left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{T_{TX_diff} + \text{round}\left(\frac{\tau_{DIFF}}{256}\right) \times 256}{2560} - 0.9 \right\rfloor,$$

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\left\lfloor \frac{T_{TX_diff} + \frac{\tau_{DIFF}}{256} \right\rfloor \times 256}{2560} - 0.9}{3} \right\rfloor, \quad \text{or}$$

$$\left\lfloor \frac{\frac{T_{TX_diff}}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\left\lceil \frac{T_{TX_diff} + \frac{\tau_{DIFF}}{256} \right\rceil \times 256}{2560} - 0.9}{3} \right\rfloor.$$

58. The UE according to claim 56 or 57, wherein the processing module is further configured to:

- 5 when the UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 - \tau_{DIFF}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH
- 10 CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

59. The UE according to claim 56 or 57, wherein the processing module is further configured to:

- 15 when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 + \tau_{DIFF}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH
- 20 CFN_DRX.

60. A user equipment (UE), comprising:

- a preprocessing module, configured to calculate boundary information HS-SCCH CFN_DRX n of a high speed shared control channel (HS-SCCH) according to a timing difference $T_{TX_diff,B}$ between a downlink F-DPCH frame of non-time reference cell and an HS-PDSCH subframe of
- 25 non-time reference cell and a timing difference $T_{TX_diff,A}$ between a downlink F-DPCH frame of

time reference cell and an HS-PDSCH subframe of time reference cell; and

a processing module, configured to acquire boundary information of a high speed dedicated physical control channel (HS-DPCCH) according to the boundary information of the HS-SCCH.

61. The UE according to claim 60, wherein the preprocessing module is further configured to:

- 5 align a start time of HS-SCCH CFN_DRX n with a start time of an HS-SCCH subframe, wherein the HS-SCCH subframe is an HS-SCCH subframe behind τ_{DRX} chips in a start time of F-DPCH CFN n, τ_{DRX} meets $-3840chips \leq \tau_{DRX} - T_0 - 7680 * DRX_OFFSET < 3840chips$, and T_0 is 1024 chips, wherein

CFN_DRX is a connection frame number in a discontinuous reception (DRX) state, and n in CFN_DRX n is a serial number of CFN_DRX; F-DPCH CFN is a connection frame number of an F-DPCH, and n in CFN n is a serial number of CFN; DRX_OFFSET is an offset of discontinuous reception (DRX); and τ_{DRX} is a timing difference between HS-SCCH CFN_DRX n and F-DPCH CFN n, wherein

$$DRX_OFFSET \text{ is } \left\lfloor \frac{\frac{T_{TX_diff,B} - 0.9}{2560} - 0.9}{3} \right\rfloor - \left\lfloor \frac{\frac{T_{TX_diff,A} - 0.9}{2560} - 0.9}{3} \right\rfloor; \text{ a hybrid automatic retransmission request}$$

- 15 acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to $T_{TX_diff,B}$ and a hybrid automatic retransmission request acknowledgement (HARQ-ACK) field corresponding to the HS-PDSCH subframe corresponding to $T_{TX_diff,A}$ are in a same HS-DPCCH subframe; and $|T_{TX_diff,B} - T_{TX_diff,A}| < 7680$ or $|T_{TX_diff,B} - T_{TX_diff,A}| \leq 3840$.

62. The UE according to claim 60 or 61, wherein the processing module is further configured to:

when the UE is not configured in multiple-input multiple-output mode, or when the UE is configured in multiple-input multiple-output mode and the UE indicates not requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH subframe that is closest

- 25 in time to $1280 - |T_{TX_diff,B} - T_{TX_diff,A}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

63. The UE according to claim 60 or 61, wherein the processing module is further configured to:

when the UE is configured in multiple-input multiple-output mode and the UE indicates requiring a longer HARQ processing time, determine boundary information of an HS-DPCCH

subframe that is closest in time to $1280 + |T_{TX_diff,B} - T_{TX_diff,A}|$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

64. The UE according to claim 60 or 61, wherein the processing module is further configured to:

determine boundary information of an HS-DPCCH subframe that is closest in time to $1280 + T_{TX_diff,A} - T_{TX_diff,B}$ chips after the start time of the boundary information of the HS-SCCH, that is, HS-SCCH CFN_DRX n, as the boundary information of the HS-DPCCH, that is, HS-DPCCH CFN_DRX n, wherein n in HS-SCCH CFN_DRX n is a serial number of HS-SCCH CFN_DRX, and n in HS-DPCCH CFN_DRX n is a serial number of HS-DPCCH CFN_DRX.

65. A base station, comprising a memory and a processor, wherein the memory is connected to the processor; and

the memory stores an execution instruction; and when the base station runs, the processor communicates with the memory, and the processor executes the execution instruction, so that the base station executes the method according to any one of claims 1 to 16.

66. A user equipment (UE), comprising a memory and a processor, wherein the memory is connected to the processor; and

the memory stores an execution instruction; and when the base station runs, the processor communicates with the memory, and the processor executes the execution instruction, so that the base station executes the method according to any one of claims 17 to 32.