

"IMPROVEMENTS IN OR RELATING TO ELECTRONIC TIMEPIECES"

This invention relates to electronic timepieces and has for its object to provide improved electronic timepieces which are reliable, of relatively simple construction and relatively cheap and easy to manufacture, of relatively low electrical power consumption and which display time optically in a manner closely simulating the time display given by an ordinary timepiece with moving mechanical hands.

The time display means used in conventional known analog electronic timepieces can be roughly divided into two classes, namely: that in which time is displayed by moving mechanical hands and that in which time is optically displayed without using actual hands. Representative examples of the latter class are timepieces with a display device comprising light-emitting elements such as light-emitting diodes which are arranged round a circle and, with the lapse of time, are either turned on in a cumulative manner or are turned on one at a time in successive positions round the circle. However, people have been accustomed for so long to reading the time by looking at the positions of an hour hand and a longer minute hand (and an additional seconds hand in timepieces displaying seconds) that it is natural to want to read the time in this way. Accordingly, although optical displays such as the diode displays above mentioned may be regarded by some people as ornamentally satisfactory it is, in practice, very desirable that the time display given shall simulate closely that given by an ordinary

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timepiece with hands and which can be quickly read in the same way. Attempts have therefore been made to achieve this desirable object but, owing to the restrictions imposed by the electronic circuits employed and, more especially, the restrictions imposed by the display devices employed, these attempts have resulted in timepieces which are incapable of displaying time with sufficient accuracy - down to a minute or a second - and/or are complex and expensive to manufacture, and/or are not easy to read at a glance, and/or lack good reliability.

According to this invention an electronic timepiece which optically provides a time display simulating that given by an ordinary timepiece with time-displaying hands and which comprises a display device having a segment electrode system consisting of a predetermined plurality of segment electrodes extending in different directions each corresponding with the direction of extension of the hand of an ordinary timepiece in a different position of said hand and a co-operating common electrode system consisting of a plurality of groups of common electrodes, the electrodes in each group being positioned with respect to the segment electrodes to co-operate with a predetermined plurality of segment electrodes; connections each connecting together two segment electrodes in predetermined positions, one in each of a different plurality of electrodes co-operating with a respective group of common electrodes; means for generating time information signals; selection means for selecting first time unit information signals at a first given time; and second time unit information signals at a second given time; means for

generating a plurality of pulse signals of predetermined different voltages one of which is of a value sufficient to produce a display if applied between a segment electrode and a common electrode and another of which is a value insufficient to produce such a display if so applied; and means, controlled by said selection means, for utilising the generated pulse signals to apply, ~~at a given time,~~ between the segment electrode system and the common electrode system, pulse signals derived from the generated pulse signals and of sufficient value to produce a display; the whole arrangement and the shapes and dispositions of the segment electrodes and of the common electrodes being such that, ~~(at said given time)~~ the display produced simulates that which would be produced ~~at that time~~ by an ordinary timepiece with hands.

15 In one embodiment which optically produces a time display simulating that given by an ordinary timepiece with hour and minute hands the segment electrode system consists of 60 radial electrodes equally spaced round a circle, and the common electrode system consists of five similar electrodes arranged in an inner ring and surrounded by five similar electrodes arranged in an outer ring, each group of common electrodes consisting of one inner electrode and one outer electrode co-operating with twelve of the segment electrodes.

In another embodiment which optically produces a time display
25 simulating that given by an ordinary timepiece with hour minute

and second hands the segment electrode system consists of six similar electrodes arranged in an inner ring and surrounded by six similar electrodes arranged in an outer ring, each group of common electrodes consisting of one inner electrode and one outer electrode co-operating with ten of the segment electrodes.

The invention is illustrated in and further explained in connection with the accompanying drawings, in which:-

Figure 1 (which is shown in two parts, Figures 1A and 1B) is a diagrammatic block circuit representation of one embodiment of the invention;

Figure 2 is a plan view of the segment electrode system of a liquid crystal display device used in the embodiment of Figure 1;

Figure 3 is a plan view of the common electrode system of the display device the segment electrode system of which is shown in Figure 2;

Figure 4 is a diagram illustrating the output conversion circuit and the segment voltage supply circuit in the embodiment of Figure 1;

Figure 5 is a diagram illustrating the common voltage supply circuit in the embodiment of Figure 1;

Figure 6 is a voltage table for illustrating the operation of Figure 1,

Figure 7 is a view showing the nature of the hand-like display of time given by the display device illustrated by

Figures 2 and 3;

Figure 8 (which is shown in two parts Figures 8A and 8B) is a diagrammatic block circuit representation of a second embodiment of the invention;

5 Figure 9 is a plan view of the segment electrode system of a liquid crystal display device used in the embodiment of Figure 8;

10 Figure 10 is a plan view of the common electrode system of the display device the segment electrode system of which is shown in Figure 9;

Figure 11 is a diagram illustrating the output conversion circuit and the segment voltage supply circuit in the embodiment of Figure 8;

15 Figure 12 is a diagram illustrating the voltage selector in Figure 8;

Figure 13 is a block diagram illustrating the common voltage supply circuit in Figure 8;

Figure 14 is a voltage table for illustrating the operation of Figure 8; and

20 Figure 15 is a view showing the nature of the hand-like display of time given by the display device illustrated by Figures 9 and 10.

Referring to Figure 1 (Figures 1A and 1B) block 1 represents a crystal controlled time standard oscillator the output of which
25 is divided down in frequency by a multi-stage frequency divider 2

the reduced frequency output from which is fed to a duodecimal counter 3 counting digits of one minute. A divide-by-five counter 4 receives the carry output of the counter 3 and counts digits of a higher order of minutes. A duodecimal counter 5 and a divide-by-five counter 6 combine to count digits of one hour. All the above-mentioned counters produce binary coded decimal outputs. Gate circuits 7 and 8 having an AND logic function receive at terminals L_2 and L_3 respectively the Q_1 and $\overline{Q}_1$ outputs of a flip-flop circuit 9 and control the passage of the outputs of the counters 3 and 4 respectively. Gate circuits 10 and 11 also having an AND logic function also respectively receive the aforesaid outputs of the flip-flop circuit 9 and control the passage of the outputs of the counters 5 and 6. The outputs of the gate circuits 7 and 10 are fed to a decoder 14 via a gate circuit 12 and the outputs of the gate circuits 8 and 11 are fed to a decoder 15 via a gate circuit 13. The gate circuits 12 and 13 have an OR logic function. 16 is an output conversion circuit which operates to change the outputs from the decoder 14 to a different order to suit the wiring of the electrodes which are used in the timepiece display device (not shown in Figure 1) as will be explained later herein. A segment voltage supply circuit 17 sets voltages that are to be applied to segment electrodes in the display device used in the timepiece, and common voltage supply circuits 18a and 18b set voltages that are to be applied to common electrodes in said display device.

19 is a flip-flop circuit which is triggered by the Q_1 output of the flip-flop circuit 9, and produces outputs which control the on and off operations of electronic switching circuits 20 to 27 of the semiconductor type. 28 is an inverter, and 29 to 33 are AND gate circuits.

The display device is of the liquid crystal type and includes a segment electrode system, generally designated 34 in Figure 2, consisting of 60 radial segment electrodes 34a equally spaced round a circle. The first twelve of these electrodes are respectively connected to the terminals e_1 to e_{12} of the segment supply circuit 17. The remaining segment electrodes are connected as described below. The count order of the segment electrodes is in the clockwise direction starting with the segment electrode which is connected to the terminal e_1 as the first one. The 12th electrode is connected to the 13th; the 11th electrode is connected to the 14th; the 10th electrode is connected to the 15th....and so on, the 24th electrode being connected to the 1st. The said 24th electrode is also connected to the 25th; the 23rd electrode is connected to the 26th...the 13th electrode is connected to the 36th....and so on until all 60 electrodes are connected in this way.

The display device also includes a common electrode system, generally designated 35 in Figure 3 which co-operates with the segment electrode system 34 of Figure 2 and consists of five similar inner electrodes 35a and five similar outer electrodes 35b.

The radial spaces 35c which separate the individual common

electrodes 35a and 35b from one another radially are located between the 12th segment electrode and the 13th; between the 24th segment electrode and the 25th; between the 36th segment electrode and the 37th; between the 48th segment electrode and the 49th; and between the 60th segment electrode and the 1st (counting in the clockwise direction).

The segment electrode system is positioned over the common electrode system and a layer of liquid crystal material (not shown) is interposed between the two systems in a sealed housing (not shown) through which the display given can be observed.

Figure 4 shows in some detail the circuitry of the output conversion circuit 16 and the segment voltage supply circuit 17 of Figure 1. In Figure 4 references 36 to 50 denote gate circuits of which 38, 41, 44, 47 and 50 are OR gates and the remainder are AND gates; 51 to 60 are switching circuits which may be like those in Figure 1; and 61 to 65 are inverters.

Figure 5 shows in some detail the common voltage supply circuit 18a. In Figure 5 references 66 to 71 denote switching circuits which may be like those in Figure 1; and 72 to 74 are inverters.

The common voltage supply circuit 18b may be constructed in the same manner as above described for the common voltage circuit 18b.

There will now be described, by way of practical example, values of relative voltages to be produced at the terminals S_0 , S_1

of Figure 1 for application to the segment electrodes; values of voltages to be produced at the terminals C_0 , C_1 of Figure 1 for application to the common electrodes; and voltages to be applied between segment and common electrodes. Predetermined

5 voltages of relative values 0, v_0 , $2v_0$ and $3v_0$ are selectively applied to the segment electrodes and the common electrodes, it being assumed that there will be no display given by voltage difference between a segment electrode and a common electrode

10 beneath it if the voltage difference is smaller than $|v_0|$ but that a display is given if said voltage difference is $3|v_0|$ or more. On this assumption a voltage of $3v_0$ is applied to terminals 1_0 , 1_5 of the switching circuits 20, 25 (Figure 1); a voltage of $2v_0$ is applied to terminals 1_3 , 1_6 of switching circuits 23, 26; a voltage v_0 is applied to terminals 1_2 , 1_7 of switching circuits

15 22, 27; and a voltage 0 (zero) is applied to terminals 1_1 and 1_4 of switching circuits 21, 24. Therefore, when the switching circuits 20 to 27 are switched by the Q_2 and $\bar{Q}_2$ outputs of the flip-flop circuit 19, which is triggered by the output of the flip-flop circuit 9, the voltages produced at the terminals S_0 , S_1 ,

20 C_0 , C_1 of Figure 1 and between them will be as shown by the Table in Figure 6. In this Table the voltages V_s are those which may be assumed by the terminals S_0 , S_1 , and the voltages V_c are those which may be assumed by the terminals C_0 , C_1 . Among these two groups of voltages, those on the left are voltages that will be produced

25 at the terminals when the Q_2 output of the flip-flop circuit 19 has

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a logical value "1" (hereinafter referred to simply as logic "1"), and those on the right are voltages produced at the terminals when the output $\overline{Q}_2$ is logic "1". The voltages V_{s-c} represent voltage values between terminals S_0, S_1 and terminals C_0, C_1 . As will now
5 be apparent, a display may be "turned on" by a voltage produced between the terminals S_0 and C_0 .

In order to explain the operation of the timepiece there will now be described the operation of the counters 3 to 6 when they have counted a particular time - 10 minutes past 10, for
10 example. In this case the counts in the minute counters 3 and 4 will be "10" and "0", respectively, and the counts in the hour counters 5, 6 will be "2" and "4", respectively. The gate circuits 7 and 8 are opened for each "1" signal which periodically occurs in the Q_1 output of the flip-flop circuit 9 which is fed with
15 output from the frequency divider 2, whereby the minutes data in the counters 3, 4 is selected, and binary coded decimal values of "10" and "0" are produced in the outputs of the gate circuits 12, 13, respectively. A logic "1" is produced at terminals 2^1 and 2^3 of the gate circuit 12, and a logic "0" is produced at terminals
20 2^0 to 2^2 of the gate circuit 13. Therefore, the voltage level on the line $\overline{X}$ (Figures 1B and 4) is logic "1" and the voltage level on line X is logic "0".

The outputs from the gate circuits 12 and 13 are converted by the decoders 14, 15 respectively whereby logic "1" is produced
25 at the terminal "10" of decoder 14 and logic "1" is produced at the

terminal "0" of the decoder 15. Referring now to Figure 4, since the level on line $\bar{X}$ is logic "1", the output of the gate circuit 45 is also logic "1", and hence, the output of the gate circuit 47 is logic "1", the switching circuit 57 is turned ON, and voltage produced at the terminal S_0 is applied to the segment electrode terminal e_{11} . The outputs of the other gate circuits, i.e., the outputs of the gate circuits 38, 41, 44, ---50 are all logic "0" and hence the switching circuits 52, 54, 56 ----- 60 are turned ON, and voltage produced at the terminal S_1 is applied to the terminals e_1 to e_{10} , and to e_{12} .

Since the voltage level at terminal j_0 of the decoder 15 is logic "1", the switching circuit 66 of Figure 5 is turned ON, and voltage produced at the terminal C_0 is applied to the common electrode terminal g_1 . Also, since the switching circuits 69, ---71 are turned ON, voltage produced at the terminal C_1 is applied to the common electrode terminals g_2 to g_5 .

Since the Q_1 output of the flip-flop circuit 9 (Figure 1) is logic "1", the level at the output terminal y_0 of the gate circuit 29 becomes logic "1". Therefore, as will be seen from the common voltage supply circuit 18a shown in Figure 5 and which is constructed in the same manner as the common voltage supply circuit 18b, voltage produced at the terminal C_0 is applied to the common electrode terminal k_1 and voltage produced at the terminal C_1 is applied to the common electrode terminals k_2 to k_5 .

It will be seen, from the voltage relations shown by the

table in Figure 6, that a display will appear between a segment electrode connected to the terminal e_{11} and a common electrode connected to the terminals k_1 and g_1 . The hours data in the counters 5, 6 is selected at each periodic development of a logic "1" signal in the $\bar{Q}_1$ output of the flip-flop circuit 9 (Figure 1) so that a logic "1" signal is produced at a "2" terminal of the decoder 14 and a logic "1" signal is produced at a "4" terminal of the decoder 15. Since the level at the 2^0 terminal of the gate circuit 13 is logic "0", the voltage level on the line X is logic "0" and that at the line $\bar{X}$ is logic "1".

The output of the gate circuit 42 (Figure 4) is logic "1", so that the output of the gate circuit 44 is logic "1" and the switching circuit 55 is turned ON so that voltage produced at the terminal S_0 is applied to the terminal e_3 . Voltage produced at the terminal S_1 is applied to other "e" terminals. Further, since the level at terminal j_4 of the decoder 15 is logic "1", voltage produced at the terminal C_0 is applied to the terminal g_5 , and voltage produced at the terminal C_1 is applied to other "g" terminals g_1 to g_4 . Moreover since the Q_1 output of the flip-flop circuit 9 is logic "0", the outputs of the gate circuits 29 to 33 are all "0", and voltage produced at the terminal C_1 is applied to the terminals k_1 to k_5 .

Thus, the display portion consisting of a segment electrode connected to the terminal e_3 and a common electrode connected to the terminal g_5 , is turned ON.

Figure 7 shows the display given as above described and consisting of two radial display lines (indicated by black radial lines) one of which simulates an hour hand and the other of which simulates a minute hand, though the display is, of course optical and there are no actual mechanical hands. In line with the descriptions of operation given hereinbefore, the time displayed in Figure 7 is ten minutes past ten.

Figure 8 (which is shown in two parts, Figures 8A and 8B) illustrates an embodiment in which the optical display given simulates that which is given by a timepiece with three hands, namely hour, minute and second hands.

Referring to Figure 8 blocks 75 and 76 represent respectively a decimal counter and a divide-by-six counter for counting the seconds digits; 77 and 78 represent respectively a decimal counter and a divide-by-six counter for counting the minute digits; and 79 and 80 represent respectively a decimal counter and a divide-by-six counter for counting hour digits. These three counters produce binary coded decimal outputs. Block 81 represents a duodecimal counter. Block 82 is a timing pulse generator 82 successively producing pulses at terminals P_1 to P_3 in response to output pulses from the frequency divider 2 driven by the crystal controlled oscillator 1. Gate circuits 83 to 88 having an AND logic function are controlled by pulses that are successively fed to the terminals P_1 to P_3 . The outputs of gate circuits 89 and 90, which have an OR logic function are fed to decoders 91 and 92 which convert the

output codes. Block 93 represents an output conversion circuit for changing the order of the outputs of the decoder 91 responsive to output from the gate circuit 90. Block 94 represents a segment voltage supply circuit the construction of which will be described in some detail later.

Block 95 represents a common voltage supply circuit for selecting voltages to be applied to the common electrodes of a liquid crystal display device which will be described later. Block 96 is a flip-flop circuit; and 97 is a voltage selector which periodically produces predetermined voltages 0 , v_0 , $2v_0$ and $3v_0$ at the terminals S_0 , S_1 , C_0 and C_1 . 98 is an inverter. The same references denote the same parts in Figures 1 and 8.

Figures 9 and 10 illustrate respectively the segment electrode system 99 and the common electrode system 100 of the display device used in the embodiment of Figure 8, and the way in which the individual electrodes are connected. As will be seen from Figure 9 there are 60 radial segment electrodes 99a which are wired in a manner generally similar to that shown in Figure 2 with the exception, however, that, in Figure 9, the number of segment electrodes in any one group is 10 instead of 12.

Figure 10 shows the common electrode system. It consists of 6 similar inner electrodes 100a and 6 similar outer electrodes 100b arranged and shaped as shown, there being a pair of common electrodes 100a, 100b underneath and opposite 10 segment electrodes when the display device is in assembled condition with the common electrode

system underneath the segment electrode system with a layer of liquid crystal between the two systems in a sealed housing through which the display can be seen.

Figure 11 shows in some detail the output conversion circuit 93 and the segment voltage supply circuit 94. In Figure 11 101 to 110 are AND gate circuits; 111 to 115 are OR gate circuits; 116 to 125 are switching circuits which may be like those in Figure 1; and 126 to 130 are inverters.

Figure 12 is a diagram showing in some detail the voltage selector 97. In Figure 12 131 to 138 are switching circuits, and 139 is an inverter.

Figure 13 is a diagram showing in some detail the common voltage supply circuit 95. In Figure 13 140 to 145 are AND gate circuits; 146 to 155 are switching circuits which may be like those in Figure 1; and 156 to 160 are inverters.

Making the same assumption as was made in the description of the previously described embodiment as regards the electrode voltage differences required between a segment electrode and a common electrode to determine whether a display is given or not, the voltages which may be applied to the segment electrodes and the common electrodes are 0, v_0 , $2v_0$ and $3v_0$. Referring to Figure 12, a voltage 0 is applied to terminals 1_1 , 1_4 ; a voltage v_0 is applied to terminals 1_2 , 1_7 ; a voltage $2v_0$ is applied to terminals 1_3 , 1_6 ; and a voltage $3v_0$ is applied to terminals 1_0 , 1_5 . A logic "1" signal is periodically produced at the terminal P_1 of the timing.

pulse generator 82 (Figure 8A) and logics "1" and "0" are alternately produced at the Q output of the flip-flop circuit 96. Therefore, voltages 0 and $3v_0$ are alternately produced at the terminal S_0 ; voltages v_0 and $2v_0$ are alternately produced at the terminal S_1 ; voltages 0 and $3v_0$ are alternately produced at the terminal C_0 ; and voltages $2v_0$ and v_0 are alternately produced at the terminal C_1 . These voltage relations are shown by the table in Figure 14 which is of the same nature as the table in Figure 6. As will be seen from Figure 14, when voltages are applied to the terminals S_0 and C_0 , a corresponding part of the display is turned on.

The operation of the embodiment will now be described in a manner similar to that previously adopted to describe the operation of the first embodiment, the time chosen for exemplification being, however, 10 hours 0 minutes 5 seconds, i.e. when the counters 75 to 80 of Figure 10 have counted a time of 5 seconds past zero minute past 10 o'clock. In this case the count in the counter 75 is "5"; that in counter 76 is "0"; that in counter 77 is "0"; that in counter 78 is "0"; that in counter 79 is "0"; and that in counter 80 is "5". As pulses are periodically produced at the terminal P_1 of the timing pulse generator 82 (Figure 8A), the seconds digits gate circuits 83, 86 are opened, so that the seconds data in the counter 75 is fed to the gate circuit 89, and the seconds data in the counter 76 is fed to the gate circuit 80. Accordingly, a logic "1" is produced at the terminals of 2^0 and 2^2

of the gate circuit 89, and a logic "0" is produced at the terminals of 2^0 to 2^2 of the gate circuit 90. Consequently the voltage level on the line $\bar{h}$ (Figure 8B) is logic "1", the level on the line h is logic "0", and that at the terminal x_5 of the decoder 91 is logic "1". Referring to Figure 11, since the gate circuits 105 and 113 produce outputs of logic "1", voltage produced at the terminals S_0 appears at the terminal e_6 . Accordingly the switching circuits 117, ---119, 123, ---125 are turned ON and the voltage at the terminal S_1 is produced at each of other "e" terminals e_1 to e_5 and e_7 to e_{10} .

A logic "1" is produced at the terminal y_0 of the decoder 92 so that voltage at the terminal C_0 appears at the terminal k_1 (Figure 13). Further, since no pulse is present at the terminal P_3 of the timing pulse generator 82 (Figure 8A), in other words the level there is logic "0", the level at the terminal $\bar{P}_3$ is logic "1", and therefore the gate circuits 140 to 145 (Figure 13) are opened. Accordingly, the switching circuit 146 is turned ON, and voltage at the terminal C_0 appears at the terminal g_1 . Voltage at the terminal C_1 is applied to the other terminals k_2 to k_6 and g_2 to g_6 . As a result, the appropriate part of the display is turned on by voltage applied to the terminal e_6 and the terminals g_1 and k_1 .

Next, when pulses are periodically generated at the terminal P_2 of the timing pulse generator 82, gate circuits 84, 87 of Figure 8B are opened to permit the passage of the data "0" in the counters 77, 78 respectively. Therefore, the level at the terminal x_0 of the decoder 91 becomes logic "1"; that at

the terminal y_0 of the decoder 92 becomes logic "1", the level at $\bar{h}$ is logic "1", and the level at $\underline{h}$ is logic "0".

Therefore, the gate circuit 111 of Figure 11 produces a logic "1" output, the switching circuit 116 is turned ON, and
5 voltage at the terminal S_0 appears at terminal e_1 . Voltage at the terminal S_1 appears at the other "e" terminals e_2 to e_{10} .

The voltage produced at the terminal C_0 (see Figure 14) is applied to the terminals g_1, k_1 , and voltage produced at the terminal C_1 is applied to the other terminals g_2 to g_6 and k_2 to k_6 ,
10 and a portion of the display corresponding to the terminal e_1 and terminals g_1, k_1 is turned on.

Pulses which are periodically generated at the terminal P_3 of the timing pulse generator 82 cause the gate circuits 85, 88 (Figure 8B) to be opened, so that outputs from the counters 79, 80
15 respectively are allowed to pass through these gate circuits.

This causes voltage at the terminal S_0 to be applied to the terminal e_{10} of the segment voltage supply circuit 94. Voltage at the terminal C_0 is applied to the terminal k_6 of the common voltage supply circuit 95, and voltage at the terminal C_1 is
20 applied to the other terminals k_1 to k_5 . When a pulse is produced at P_3 , the outputs of the gate circuits 140 to 145 of Figure 15 are all logic "0" and hence voltage produced at the terminal C_1 is applied to the terminals g_1 to g_6 . Consequently a portion of the display corresponding with the terminals e_{10} and k_6 is turned
25 on. Figure 15 shows in manner similar to that adopted in Figure 7,

the simulated three hand (simulated hour minute and second hand) display given for the above exemplified time of 10 hours 0 minutes 5 seconds.

As will now be appreciated the invention provides an optical
5 display simulating an hour and minute hand display (in the first embodiment described herein) or an hour, minute and second hand display (in the second embodiment described herein) by means of an electro-optical display device having a segment electrode system and a co-operating common electrode system and in which the segment
10 electrodes are divided into groups, segment electrodes located at predetermined positions in each of the groups being common connected together, and pulses being selectively supplied, in response to time-divided display information, to hand simulating portions of the display device comprising segment electrodes and divided common
15 electrodes. In this way the number of terminals required for connection to the electrodes in the segment electrode system is much reduced compared with what would otherwise be necessary, resulting in increased reliability, increased ease of manufacture, reduced cost of manufacture, and much greater convenience in
20 connecting the display device itself to its operating circuitry. Other important advantages obtained are much reduced liability to "crosstalk" (production of visible displays in wrong positions adjacent the correct ones) increased speed of response and increased stability over a wide range of ambient temperatures. From the
25 viewpoint of the user, the display given is very convenient and

satisfactory, simulating closely, as it does, the display given by ordinary mechanical watch hands and enabling the time to be read quickly in a natural manner. Furthermore the consumption of electrical power is low because the display device is semi-
5 statically operated for each time information unit instead of being dynamically operated.

In addition, since the appropriate part of the display is turned on for each unit of time information, the quantity of information which is simultaneously displayed at any instant is
10 maintained constant notwithstanding that the total quantity of information may be high (for example displaying time down to seconds) so that inconveniently high preset operating voltage levels are not required.



C L A I M S

1. An electronic timepiece which optically provides a time display simulating that given by an ordinary timepiece with time-displaying hands and which comprises a display device having a segment electrode system consisting of a predetermined plurality of segment electrodes extending in different directions each corresponding with the direction of extension of the hand of an ordinary timepiece in a different position of said hand and a co-operating common electrode system consisting of a plurality of groups of common electrodes, the electrodes in each group being positioned with respect to the segment electrodes to co-operate with a predetermined plurality of segment electrodes; connections each connecting together two segment electrodes in predetermined positions, one in each of a different plurality of segment electrodes co-operating with a respective group of common electrodes; means for generating time information signals; selection means for selecting first time unit information signals at a first given time and second time unit information signals at a second given time; means for generating a plurality of pulse signals of predetermined different voltages one of which is of a value sufficient to produce a display if applied between a segment electrode and a common electrode and another of which is of a value insufficient to produce such a display if so applied; and means, controlled by said selection means, for utilising the generated pulse signals to apply between the segment electrode system and the common electrode system, pulse signals derived from the generated pulse signals and of sufficient



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value to produce a display; the whole arrangement and the shapes and dispositions of the segment electrodes and of the common electrodes being such that, ~~at said given time~~ the display produced simulates that which would be produced ~~at that time~~ by an ordinary timepiece with hands.

2. A timepiece as claimed in claim 1 which optically produces a time display simulating that given by an ordinary timepiece with hour and minute hands and in which the segment electrode system consists of 60 radial electrodes equally spaced round a circle, and the common electrode system consists of five similar electrodes arranged in an inner ring and surrounded by five similar electrodes arranged in an outer ring, each group of common electrodes consisting of one inner electrode and one outer electrode co-operating with twelve of the segment electrodes.

3. A timepiece as claimed in claim 2 and having a liquid crystal display device substantially as herein described with reference to Figures 2 and 3 and driven by an electronic circuit arrangement substantially as herein described with reference to Figure 1 (A and B).

4. A timepiece as claimed in claim 1 which optically produces a time display simulating that given by an ordinary timepiece with hour minute and second hands and in which the segment electrode system consists of six similar electrodes arranged in an inner ring and surrounded by six similar electrodes arranged in an outer ring, each group of common electrodes consisting of one inner electrode and one outer electrode co-operating with ten of

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the segment electrodes.

5. A timepiece as claimed in claim 4 and having a liquid crystal display device substantially as herein described with reference to Figure 9 and 10 and driven by an electronic circuit arrangement substantially as herein described with reference to Figure 8 (A and B).

6. An electronic timepiece comprising an optical display device having a number of separate display elements in the shape of hands and including electrodes comprised of a number of segment electrodes in the shape of hands arranged to extend radially from a point, and common electrodes formed in at least two concentric rings and divided into sector-like electrodes each of which is of the same arcuate extent and opposes a group of the segment electrodes, means comprised of circuit paths for connecting together a corresponding segment electrode in each of the groups without crossing one another, and liquid crystal display material between the segment electrodes and the common electrodes; time counting means receptive of clock pulses for generating a time-count output representing at least minutes and hours; a timing pulse generator for generating timing pulses; a selection circuit receptive of timing pulses for causing each time unit of the time count output to be in synchronisation with the timing pulses; first means for decoding one place of each time unit of the time-count-output generated by the selection circuit to logical values for selecting a set of connected corresponding segment electrodes; second means for decoding a second place of each time



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unit of the time-count-output generated by the selection circuit to logical values for selecting a sector-like electrode; a common voltage supply circuit for applying a pulsed voltage having an instantaneous value designated
5 by the second means to each sector-like electrode; and a segment voltage supply circuit for applying a pulsed voltage having such an instantaneous value relative to the pulsed voltage applied to the sector-like electrodes that the display elements are selectively turned ON and OFF when said
10 different pulsed voltages are applied to the sector-like electrodes.

7. An electronic timepiece comprising an optical display device having a number of separate display elements in the shape of hands and including electrodes comprised of a number of
15 segment electrodes in the shape of hands arranged to extend radially from a point, and common electrodes formed in at least two concentric rings and divided into sector-like electrodes each of which is of the same arcuate extent and opposes a group of segment electrodes, means
20 comprised of circuit paths for connecting together a corresponding segment electrode in each of the groups without crossing one another, and liquid crystal display material between the segment electrodes and the common electrodes; time counting means receptive of clock
25 pulses for generating a time-count-output representing at least minutes and hours; a timing pulse generator for generating timing pulses; a selection circuit receptive of timing pulses for causing each time unit of the time-count-output to be in synchronization with
30 the timing pulses; first means for decoding one place of each time unit of the time-count-output generated by the selection circuit to logical values for selecting a

set of connected corresponding segment electrodes; second means for decoding a second place of each time unit of the time-count-output generated by the selection circuit to logical values for selecting a sector-like electrode; a segment voltage supply circuit for applying selectively the voltages 0 , v_0 , $2v_0$ and $3v_0$ to the respective segment electrodes in accordance with the output from the second means; and a common voltage supply circuit for applying selectively the voltages 0 , v_0 , $2v_0$ and $3v_0$ to the respective sector-like electrodes, the whole arrangement being such that there is periodically applied to a display element to be turned ON a voltage $|3v_0|$ at a maximum between each segment electrode and each sector-like electrode and to a display element to be turned OFF there is periodically applied a voltage $|v_0|$ at a maximum between each segment electrode and each sector-like electrode.

8. Electronic timepieces substantially as herein described with reference to the accompanying drawings.

The text of the specification has been reproduced by photocopying the applicants original typescript. It may contain a few amendments which are difficult to read. The original typescript containing these amendments may be inspected on the premises of the Patent Office

