SUBSTRATE LEVEL 3D PACKAGE FOR SEMICONDUCTOR DEVICES

Abstract

Conventional practice for silicon device / component assembly on circuit board is to assemble the individually packaged semiconductor components using SMT lines. The circuit boards are fairly larger in size for these component assemblies due to thick population of components including discrete devices such as resistors, capacitors and inductors. These practices were very well accepted in the past, as the systems that were manufactured were fairly larger in size. We could assemble many components, even multiple numbers of same components to obtain more functionality such as memory and so on, on the same board and meet the consumer requirements.

However, In the recent past the consumer market is driven by miniaturized products due to portability, lower costs, and other numerous requirements by the consumers. Large sized products are no more accepted and hence there became a need for developing miniature sized products to meet the consumer market. Number of semiconductor industry including design houses, fab houses are continuously shrinking the device feature sizes and adding more and more functionality in single chips in the form of System on Chip (SOC), System in Package (SIP) and so on. At the same time packaging industry are also being driven by miniaturized packages with increased functionality per package.

This invention approach is expected to meet such a requirement of miniaturized product, as it offers increased functionality combined with reduced cost at very small foot prints on the circuit boards.

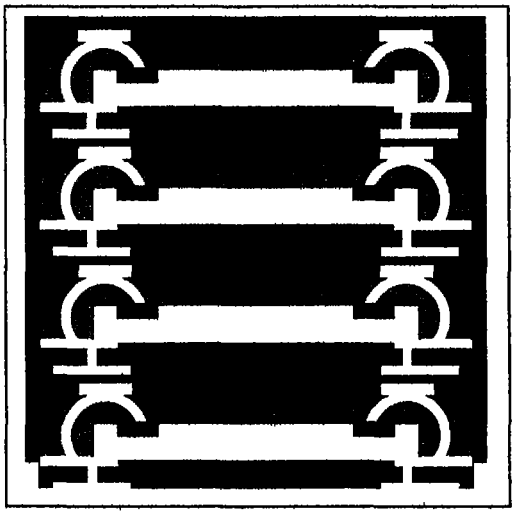


Figure: Substrate Level 3D package

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