CLAIMS

1. A quantum processing system, comprising:

a first set of control electronics operating at a first temperature;

a second set of control electronics comprising an arbitrary waveform generator communicatively coupled to the first set of control electronics and operating at a second controlled temperature that is at a cryogenic temperature that is lower than the first temperature, the second set of control electronics comprising:

one or more circuits configured to perform a write operation to one or more qubits; and

one or more circuits configured to perform a read operation to the one or more qubits; and

a qubit array comprising the one or more qubits and operating at a third controlled temperature that is lower than the second temperature, wherein the qubit array is controlled by the second set of control electronics.

2. The quantum processing system of claim 1, wherein the first temperature is substantially at room temperature.

3. The quantum processing system of any one of the preceding claims, further comprising a first set of interconnects between the first and second set of control electronics, configured to at least one of: control, monitor, or provide one or more reference signals to the second set of control electronics, including at least one of a voltage reference, a current reference, or a clock reference, which do not scale with a number of qubits in the qubit array.

4. The quantum processing system of any one of the preceding claims, further comprising a second set of interconnects between the second set of control electronics and the qubit array, configured to at least one of: monitor or provide dynamic signals to the one or more qubits of the qubit array, wherein there is one interconnect in the second set of interconnects for each of the one or more qubits of the qubit array.

5. The system of any one of the preceding claims, wherein the second set of control electronics comprises a plurality of write controllers, wherein each write controller comprises an independently programmable qubit control circuit.

6. The system of claim 5, further comprising a first signal processing element configured to process a common part of a waveform shape for amplitude and phase, wherein each write controller includes a second signal processing element that is configured to process a part that is individual to a qubit.

7. The system of claim 6, wherein each independently programmable element of a write controller is configured to process a unique combination of amplitude and phase of a waveform shape for a corresponding qubit in the qubit array.

8. The system of any one of claims 6 to 7, wherein:

the first signal processing element comprises a high-resolution digital to analog converter; and

the second signal processing element comprises a low-resolution digital to analog converter that is lower in resolution than the first signal processing element.

9. The system of any one of the preceding claims, wherein the qubit array comprises a plurality of clusters, each cluster being arranged to provide a maximum separation of a resonance frequency of its corresponding qubit to minimize a cross talk between adjacent clusters of the plurality of clusters.

10. The system of any one of the preceding claims, wherein the second set of control electronics is in complementary metal oxide semiconductor (CMOS) technology.

11. The system of any one of the preceding claims, wherein the second set of control electronics is further configured to provide a power management circuit for the qubit array.

12. The system of any one of the preceding claims, wherein the second controlled temperature is a cryogenic temperature that is between 1 to 4 Kelvin.

13. The system of any one of the preceding claims, wherein the third controlled temperature is a cryogenic temperature of approximately 240 mK.

14. The quantum processing system of any one of the preceding claims, wherein the qubit array is divided into groups, each group comprising a diverse set of center frequencies of qubits such that a cross talk between adjacent qubits is reduced.

15. The system of any one of the preceding claims, wherein at least one of the one or more circuits configured to perform the write operation comprises two separate multiplier mixers to obtain an upper and a lower sideband separately.

16. A method of controlling an array of qubits, comprising:

operating a first set of control electronics at a first temperature;

operating a second set of control electronics comprising an arbitrary waveform generator communicatively coupled to the first set of control electronics at a second controlled temperature that is at a cryogenic temperature that is lower than the first temperature, the second set of control electronics comprising:

one or more circuits configured to perform a write operation to one or more qubits; and

one or more circuits configured to perform a read operation to the one or more qubits; and

operating a qubit array comprising the one or more qubits at a third controlled temperature that is lower than the second temperature, wherein the qubit array is controlled by the second set of control electronics.

17. The method of claim 16, wherein:

the first temperature is substantially at room temperature;

the second controlled temperature is a cryogenic temperature that is between 1 to 4 Kelvin; and

the third controlled temperature is a cryogenic temperature of approximately 240 mK.

18. The method of any one of claims 16 to 17, further comprising:

providing a first set of interconnects between the first and second set of control electronics to at least one of: control, monitor, or provide one or more reference signals to the second set of control electronics, including at least one of a voltage reference, a current

reference, or a clock reference, which do not scale with a number of qubits in the qubit array; and

providing a second set of interconnects between the second set of control electronics and the qubit array to at least one of: monitor or provide dynamic signals to the one or more qubits of the qubit array, wherein there is one interconnect in the second set of interconnects for each of the one or more qubits of the qubit array.

19. The method of any one of claims 16 to 18, further comprising:

processing a common part of a waveform shape for amplitude and phase with a first signal processing element that is outside a plurality of write controllers; and

processing an individual portion of the waveform signal with a second signal processing element that is local to a write controller of the plurality of write controllers.

20. The method of any one of claims 16 to 19, dividing the qubit array into groups, each group comprising a diverse set of center frequencies of qubits such that a cross talk between adjacent qubits is reduced.