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(19)

(54) IMPROVEMENTS IN OR RELATING TO THE MANUFACTURE OF SEMICONDUCTOR DEVICES

(71) We FAIRCHILD CAMERA AND INSTRUMENT CORPORATION, of 464 Ellis Street, Mountain View, California 94042, United States of America, a corporation organised and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

This invention relates to a method of manufacturing semiconductor devices and to semiconductor devices manufactured by the method.

Conventional techniques for the fabrication of silicon gate integrated circuit structures typically involves the use of boron to form p+ regions in a monocrystalline silicon substrate. In one well-known process, a polycrystalline silicon island is formed on the surface of a region of thin silicon dioxide which has previously been formed on a substrate of monocrystalline silicon. The oxide overlying selected regions of the substrate wherein source or drain regions are desired is removed and boron oxide deposited. In many prior art processes these selected regions are chosen to be adjacent to the polycrystalline island. P+ conductivity type source or drain regions are formed where the boron diffuses into the silicon substrate. Conventionally the boron oxide is removed and a region of insulating material is formed for masking and etching of openings for electrical contact. Subsequently, electrical connections are made to desired regions through these openings.

Unfortunately, this procedure by which many prior art MOS circuits have been fabricated includes a number of deficiencies. First, it is difficult to obtain highly reliable electrical connections using metal deposited on the surface of the wafer. The principal reasons for this difficulty appear to be the abrupt edges of the polycrystalline silicon islands and the intersection of the thin gate oxide with the substantially thicker field oxide over which the metal connections must be formed. The abrupt change of direction which the deposited metal is required to assume causes cracks and gaps within the metal. Consequently, it is difficult to create a reliable electrical connection in a substantial number of structures. It is also difficult to form reliable electrical connections between the metal and polycrystalline silicon, and between the metal and source or drain regions. This difficulty is also apparently caused by the sharp edge of the opening in the oxide which the metal traverses.

Additionally, MOS circuits constructed in accordance with the prior art were susceptible to "staining" of the heavily doped source and drain region contact openings. Staining is a phenomenon well known in the art of semiconductor manufacture. The result of staining is to cause nonuniform, unpredictable penetration of the source or drain regions during formation of the metal connections with these regions.

Further, in some prior art semiconductor fabrication methods, the boron diffusion process and subsequent oxidations cause the creation of a thin layer of boron oxide on the p+ source or drain region surfaces beneath subsequently formed phosphorus oxide. Whereas the phosphorus oxide etches very rapidly, the boron oxide etches very slowly. Consequently, extended etching times are necessary to completely remove the boron oxide, especially the last approximately 200 Angstroms. The prolonged etch times necessary to remove the boron oxide cause excessive etching of other closely situated oxides and result in openings in the phosphorus oxide for electrical connections which are undesirably large, and which have excessively steep walls. These steep walls are prominent even though the oxide

etches at a higher rate at the surface, than in the interior.

In addition, the p+ region silicon surface tends to remain hydrophilic, even though the oxide is removed. Oxidized silicon is known to be hydrophilic, while silicon is hydrophobic. Because the transition from hydrophilic to hydrophobic is often used as a test of the completeness of an etching process, it is difficult to discern when sufficient etching has occurred. Further, if the slow etching boron oxide region is not completely removed, it is difficult to alloy metal electrical contact to the p+ source or drain regions.

This invention accordingly provides a method of manufacturing, in a body of semiconductor material having insulation on a surface hereof, a field effect semiconductor device having a source region separated from a drain region by a channel overlain by gate insulation on which lies a gate electrode together with electrical contacts to the source and drain regions, in which method the openings in the insulation for the contacts to the source and drain regions are formed by the steps of

forming openings for electrical connections through said insulation to expose selected portions of the top surfaces of said source and drain regions;

heating said semiconductor material to smooth the edges of said openings, thereby to prevent cracking of electrical contacts which are to cross said edges, and simultaneously to form a relatively thin region of an oxide of the dopant used to form said source and drain regions on the exposed selected portions of the top surfaces of the source and drain regions;

converting said oxide of the dopant predominantly to a selected material while simultaneously converting shallow surface layers of said source and drain regions to lightly-doped material of opposite conductivity type to the conductivity type of said source and drain regions, said lightly-doped material possessing an etch rate higher than the etch rate of said insulation; and,

removing said selected material from the surfaces of said source and drain regions exposed by said openings thereby to allow electrical contacts to be made to the source and drain regions.

Additionally, the invention provides a method of manufacturing, in a body of semiconductor material having an insulation layer on a surface thereof, a field effect semiconductor device having a source region separated from a drain region by a channel overlain by gate insulation and a conductive gate electrode, the method having the steps of forming the source and drain regions by diffusing a dopant from a layer of the oxide of the dopant formed over the surfaces of the source and drain regions;

forming an oxide of the semiconductor material at least over those portions of the surfaces of the source and drain regions underlying the oxide of the dopant by passing oxygen atoms through the oxide of the dopant;

forming a further layer of insulating material on the surface of the oxide of the dopant;

forming openings for electrical connections through said further layer of insulating material to expose portions of the top surfaces of said source and drain regions;

heat treating said wafer to smooth the edges of the openings in said further layer of insulating material thereby to prevent electrical connections to said source and drain regions from cracking at said edges and simultaneously forming a layer of the oxide of the dopant in said source and drain regions on at least the exposed surfaces of said source and drain regions;

converting said newly formed layer of the oxide of the dopant in said source and drain regions predominantly to a second selected material possessing a relatively faster etch rate than said insulation layer and further layer of insulating material; and,

removing the second selected material from the openings thereby to allow electrical contacts to be made to said source and drain regions.

The invention also provides a method of manufacturing a semiconductor device, the method comprising the steps of:

forming a first layer of insulating material on a selected surface of a substrate of semiconductor material;

removing a portion of said first layer of insulating material from a first selected region on the surface of said substrate;

forming a second layer of insulating material within said first selected region;

forming electrically conductive material in selected patterns over the top surfaces of said first layer of insulating material and said second layer of insulating material thereby to leave exposed selected portions of said second layer of insulating material;

removing said selected portions of said second layer of insulating material to thereby expose the top surfaces of second regions of said semiconductor material underlying said selected portions;

forming a layer of first selected material on the top surfaces of said second regions of semiconductor material, said conductive material and said first layer of insulating material, said first selected material containing a dopant for the formation of source and drain regions in said second regions of said semiconductor material;

forming source and drain regions in said semiconductor material by diffusing the

dopant from said first selected material into said second regions of said semiconductor material;

removing selected portions of said first selected material from said top surfaces of said second regions of said semiconductor material;

forming a third layer of insulating material on the surface of said semiconductor material and said first layer of insulating material, said third layer of insulating material being formed beneath the remaining portions of said first selected material;

forming a fourth layer of insulating material over the exposed top surfaces of the remaining portions of said first selected material;

forming openings for electrical connections through said fourth layer of insulating material to expose selected portions of the top surfaces of said source and drain regions;

heating said substrate and the attached materials to smooth the edges of said openings thereby to prevent electrical connections which will cross said edges from cracking, and simultaneously to form a relatively thin region of an oxide of the dopant used to form said source and drain regions on the exposed selected portions of the top surfaces of said source and drain regions;

convering said oxide of the dopant predominantly to a second selected material while simultaneously converting shallow surface layers of said source and drain regions to lightly-doped material of opposite conductivity type to the conductivity type of said source and drain regions, said lightly-doped material possessing an etch rate relatively higher than the etch rate of the insulating material remaining on said substrate; and

removing said second selected material from the surfaces of said source and drain regions exposed by said openings thereby to allow electrical contact to be made to said source and drain regions.

The invention will be readily understood from the following illustrative description and the accompanying drawing, in which:

Figures 1*a*, 1*b*, 1*c* and 1*d* are sectional side views of a semiconductor device in successive stages of manufacture in accordance with the invention.

Referring now to Figure 1*a*, a first layer of insulating material 11 (i.e. material 11*a* and 11*b*) is formed upon the surface of substrate 10 of wafer 8. The substrate 10 can be of N conductivity type monocrystalline silicon, while insulating material 11 is silicon dioxide. Insulating material 11 is removed from the surface of substrate 10 within a first region 9. Typically, this is accomplished by an etching process; however, other processes may also be employed. A second layer of insulating material 12 is then formed on substrate 10 throughout region 9, and may also be formed on insulating material 11.

This material 12 typically will be silicon dioxide and will be thinner than insulating material 11; however, other non-electrically-conductive materials of appropriate thickness may also be employed. Subsequently, a region of electrically conductive material 15 is formed on the surface of thin insulating material 12. To provide for electrical contact to other regions, a region of conductive material 15 may also be formed elsewhere on the surface of wafer 8, for example, on insulating material 11*b*, substrate 10, and region 18. Electrically conductive material 15*a* and 15*b* is formed by depositing a layer of material 15 across the surface of insulating materials 11 and 12, and then removing conductive material 15 from all portions of insulating materials 11 and 12, except at those selected regions where the material is desired, for example, as shown in Figure 1*a*. Conductive material 15 typically will be polycrystalline silicon, also known as polysilicon, although other electrical conductive materials may be also employed. Those regions of insulating material 12 not covered by patterned layer 15 are removed.

A layer of first selected material 14 is then formed across the surface of wafer 8. In one embodiment of this invention, the first selected material is boron oxide. The boron from the oxide will diffuse into the surface of substrate 10 to form regions 17 and 18. In general, the first selected material may be any insulating material which contains dopant for the source and drain regions.

Referring now to Figure 1*b*, all or selected portions of first selected material 14 are removed from substrate 10, for example at region 20. This removal will typically be accomplished by an etching process; however, other procedures may also be used. It should be noted that unlike the fabrication processes of the prior art, it is not necessary to remove all of the first selected material 14 from regions where electrical contact is desired. Any small amount remaining will be removed in a later step of the fabrication process. (Figure 1*b* shows a small amount remaining.) After removal of the selected region of first selected material 14, a third layer of insulating material 19 is formed on the surface of the underlying material, for example, insulating material 11, regions 17 and 18, and conductive material 15. The insulating material 19 typically will be silicon dioxide formed by an oxidation process, however, other materials may also be used. In carrying out this step, oxygen atoms easily

pass through any remaining material 14 to combine with semiconductor material 10 and thus form an oxide.

Referring now to Figure 1*c*, a fourth layer of insulating material 22 is formed on the surface of the wafer 8. The insulating material 22 may be the same as the insulating material 19; however, material 22 will have "flow" properties at elevated temperatures. Thus, elevated temperatures will soften the insulating material 22 so that it will flow like viscous liquid. After its formation, the layer of insulating material 22 is subjected to elevated temperatures (a heat treatment) which causes smoothing of non-uniformities. Openings such as the illustrated opening at region 24, for electrical connections to underlying material, are then made and the insulating material 22 is again subjected to elevated temperatures. This heat treatment causes smoothing of the edges 25 of the openings for electrical connections, which in prior art processes remain sharp. It should be noted that region 20 (Figure 1*b*) and region 24 (Figure 1*c*) need not be the same size. For example, for purposes of alignment ease it may be convenient for region 24 to be disposed entirely within region 20.

During the second heat treatment of the second insulating material 22, a relatively thin region of insulating material 21, typically a boron oxide, is formed in the contact opening, for example, on the surface of region 17.

Newly formed insulating material 21 is then converted to second selected material 21. For example, in one embodiment if the first selected material 14 is an oxide of boron, and the second selected material 21 is to be predominantly an oxide of phosphorus, a $POCl_3$ treatment well-known in semiconductor manufacture could be performed to convert the boron oxide to predominantly phosphorus oxide. During this $POCl_3$ treatment the surface of the source or drain regions 17 and 18 and the polycrystalline silicon gate are converted to lightly doped N- conductivity type material. Referring now to Figure 1*d*, the relatively thin region of second selected material 21 is removed by any desired process, for example, an etch. Electrical connections 23 may then be formed for providing electrical signals to wafer 8.

Second selected material 21 must be a material having chemical properties which are sufficiently different from those of the initially formed insulating materials and other materials on the substrate for it to be selectively removed without significantly affecting surrounding materials. For example, the second selected material may be fast etching compared to other materials in the structure.

Further, it may be desirable for the second selected material to contain dopant of opposite conductivity type to the first selected material. For example, in one embodiment, the conversion of the first selected material in region 24 to second selected material may cause the source region and drain region to be doped N conductivity type to a very shallow depth. This causes the surface of the source region and drain region to become hydrophobic when clean, thereby furnishing visible indication of when the etching process is complete. The N type surface layer causes no adverse effects as it is sufficiently shallow to allow electrical contact to the p+ regions to be made by alloying through the surface layer.

The above described manufacturing method provides numerous advantages over the prior art. The edges 25 of the openings for electrical connections in region 24 will be smoothly contoured because of the heat treatment of insulating material 22. This eliminates the need for achieving the contour during an etching process as in the prior art. Further, the size of the openings for electrical contact are also controlled with more precision than in the prior art. This is accomplished by the conversion of first selected material to second selected material. For example, in one embodiment, any remaining portion of first selected material 14 (see Figure 1*b*) plus additional insulating material which is formed beneath the first selected material is converted to a predominantly phosphorus oxide layer by means of a phosphorus diffusion, well-known in semiconductor manufacturing. This thin layer of predominantly phosphorus oxide may be then removed without additional masking step. This is possible because its etch rate is sufficiently great so only a minor amount of insulating material 22 surrounding the electrical contact openings is removed. This loss of insulating material 22 can be compensated for by forming insulating material 22 slightly thicker than that desired in the final structure.

Although the process of the invention as described with reference to Figures 1*a* to 1*d* includes a contact to only one of the source and drain regions, it will be evident that a contact is made in practice to each region, each contact being made in accordance with the invention.

WHAT WE CLAIM IS:—

1. A method of manufacturing, in a body of semi-conductor material having insulation on a surface thereof, a field effect semiconductor device having a source region separated from a drain region by a channel overlain by gate insulation on which lies a gate electrode together with electrical contacts to the source and drain regions, in which method the openings in

pass through any remaining material 14 to combine with semiconductor material 10 and thus form an oxide.

Referring now to Figure 1*c*, a fourth layer of insulating material 22 is formed on the surface of the wafer 8. The insulating material 22 may be the same as the insulating material 19; however, material 22 will have "flow" properties at elevated temperatures. Thus, elevated temperatures will soften the insulating material 22 so that it will flow like viscous liquid. After its formation, the layer of insulating material 22 is subjected to elevated temperatures (a heat treatment) which causes smoothing of non-uniformities. Openings such as the illustrated opening at region 24, for electrical connections to underlying material, are then made and the insulating material 22 is again subjected to elevated temperatures. This heat treatment causes smoothing of the edges 25 of the openings for electrical connections, which in prior art processes remain sharp. It should be noted that region 20 (Figure 1*b*) and region 24 (Figure 1*c*) need not be the same size. For example, for purposes of alignment ease it may be convenient for region 24 to be disposed entirely within region 20.

During the second heat treatment of the second insulating material 22, a relatively thin region of insulating material 21, typically a boron oxide, is formed in the contact opening, for example, on the surface of region 17.

Newly formed insulating material 21 is then converted to second selected material 21. For example, in one embodiment if the first selected material 14 is an oxide of boron, and the second selected material 21 is to be predominantly an oxide of phosphorus, a $POCl_3$ treatment well-known in semiconductor manufacture could be performed to convert the boron oxide to predominantly phosphorus oxide. During this $POCl_3$ treatment the surface of the source or drain regions 17 and 18 and the polycrystalline silicon gate are converted to lightly doped N- conductivity type material. Referring now to Figure 1*d*, the relatively thin region of second selected material 21 is removed by any desired process, for example, an etch. Electrical connections 23 may then be formed for providing electrical signals to wafer 8.

Second selected material 21 must be a material having chemical properties which are sufficiently different from those of the initially formed insulating materials and other materials on the substrate for it to be selectively removed without significantly affecting surrounding materials. For example, the second selected material may be fast etching compared to other materials in the structure.

Further, it may be desirable for the second selected material to contain dopant of opposite conductivity type to the first selected material. For example, in one embodiment, the conversion of the first selected material in region 24 to second selected material may cause the source region and drain region to be doped N conductivity type to a very shallow depth. This causes the surface of the source region and drain region to become hydrophobic when clean, thereby furnishing visible indication of when the etching process is complete. The N type surface layer causes no adverse effects as it is sufficiently shallow to allow electrical contact to the p+ regions to be made by alloying through the surface layer.

The above described manufacturing method provides numerous advantages over the prior art. The edges 25 of the openings for electrical connections in region 24 will be smoothly contoured because of the heat treatment of insulating material 22. This eliminates the need for achieving the contour during an etching process as in the prior art. Further, the size of the openings for electrical contact are also controlled with more precision than in the prior art. This is accomplished by the conversion of first selected material to second selected material. For example, in one embodiment, any remaining portion of first selected material 14 (see Figure 1*b*) plus additional insulating material which is formed beneath the first selected material is converted to a predominantly phosphorus oxide layer by means of a phosphorus diffusion, well-known in semiconductor manufacturing. This thin layer of predominantly phosphorus oxide may be then removed without additional masking step. This is possible because its etch rate is sufficiently great so only a minor amount of insulating material 22 surrounding the electrical contact openings is removed. This loss of insulating material 22 can be compensated for by forming insulating material 22 slightly thicker than that desired in the final structure.

Although the process of the invention as described with reference to Figures 1*a* to 1*d* includes a contact to only one of the source and drain regions, it will be evident that a contact is made in practice to each region, each contact being made in accordance with the invention.

WHAT WE CLAIM IS:—

1. A method of manufacturing, in a body of semi-conductor material having insulation on a surface thereof, a field effect semiconductor device having a source region separated from a drain region by a channel overlain by gate insulation on which lies a gate electrode together with electrical contacts to the source and drain regions, in which method the openings in

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the insulation for the contacts to the source and drain regions are formed by the steps of:

forming openings for electrical connections through said insulation to expose selected portions of the top surfaces of said source and drain regions;

heating said semiconductor material to smooth the edges of said openings, thereby to prevent cracking of electrical contacts which are to cross said edges, and simultaneously to form a relatively thin region of an oxide of the dopant used to form said source and drain regions on the exposed selected portions of the top surfaces of the source and drain regions;

converting said oxide of the dopant predominantly to a selected material while simultaneously converting shallow surface layers of said source and drain regions to lightly-doped material of opposite conductivity type to the conductivity type of said source and drain regions, said lightly-doped material possessing an etch rate higher than the etch rate of said insulation; and,

removing said selected material from the surfaces of said source and drain regions exposed by said openings thereby to allow electrical contacts to be made to the source and drain regions.

2. A method of manufacturing, in a body of semiconductor material having an insulation layer on a surface thereof, a field effect semiconductor device having a source region separated from a drain region by a channel overlain by gate insulation and a conductive gate electrode, the method having the steps of:

forming the source and drain regions by diffusing a dopant from a layer of the oxide of the dopant formed over the surfaces of the source and drain regions;

forming an oxide of the semiconductor material at least over those portions of the surfaces of the source and drain regions underlying the oxide of the dopant by passing oxygen atoms through the oxide of the dopant;

forming a further layer of insulating material on the surface of the oxide of the dopant;

forming openings for electrical connections through said further layer of insulating material to expose portions of the top surfaces of said source and drain regions;

heat treating said wafer to smooth the edges of the openings in said further layer of insulating material thereby to prevent electrical connections to said source and drain regions from cracking at said edges and simultaneously forming a layer of the oxide of the dopant in said source and drain regions on at least the exposed surfaces of said source and drain regions;

converting said newly formed layer of the oxide of the dopant in said source and drain regions predominantly to a second selected material possessing a relatively faster etch rate than said insulation layer and further layer of insulating material; and,

removing the second selected material from the openings thereby to allow electrical contacts to be made to said source and drain regions.

3. A method of manufacturing a semiconductor device according to claim 2 in which the second selected material comprises an oxide of phosphorus.

4. A method of manufacturing a semiconductor device according to claim 3 in which, during the conversion of the newly formed layer of the oxide of the dopant in the source and drain regions to the oxide of phosphorus, a shallow layer of N-type conductivity material is formed on the surfaces of the source and drain regions and the conductive gate electrode of the device.

5. A method of manufacturing a semiconductor device according to claim 2, 3 or 4 in which the surface of the source and drain regions is hydrophobic when the second selected material is removed thereby providing a visible indication of when the removal of said second selected material is completed.

6. A method of manufacturing a semiconductor device according to any preceding claim in which the dopant in the source and drain regions comprises boron.

7. A method of manufacturing a semiconductor device, the method comprising the steps of:

forming a first layer of insulating material on a selected surface of a substrate of semiconductor material;

removing a portion of said first layer of insulating material from a first selected region on the surface of said substrate;

forming a second layer of insulating material within said first selected region;

forming electrically conductive material in selected patterns over the top surfaces of said first layer of insulating material and said second layer of insulating material thereby to leave exposed selected portions of said second layer of insulating material;

removing said selected portions of said second layer of insulating material to thereby expose the top surfaces of second regions of said semiconductor material underlying said selected portions;

forming a layer of first selected material on the top surfaces of said second regions of semiconductor material, said conductive material and said first layer of insulating material, said first selected material containing a dopant for the formation of source

and drain regions in said second regions of said semiconductor material;

forming source and drain regions in said semiconductor material by diffusing the dopant from said first selected material into said second regions of said semiconductor material;

removing selected portions of said first selected material from said top surfaces of said second regions of said semiconductor material;

forming a third layer of insulating material on the surface of said semiconductor material and said first layer of insulating material, said third layer of insulating material being formed beneath the remaining portions of said first selected material;

forming a fourth layer of insulating material over the exposed top surfaces of the remaining portions of said first selected material;

forming openings for electrical connections through said fourth layer of insulating material to exposed selected portions of the top surfaces of said source and drain regions;

heating said substrate and the attached materials to smooth the edges of said openings thereby to prevent electrical connections which will cross said edges from cracking, and simultaneously to form a relatively thin region of an oxide of the dopant used to form said source and drain regions on the exposed selected portions of the top surfaces of said source and drain regions;

converting said oxide of the dopant predominantly to a second selected material while simultaneously converting shallow surface layers of said source and drain regions to lightly-doped material of opposite conductivity type to the conductivity type of said source and drain regions, said lightly-doped material possessing an etch rate relatively higher than the etch rate of the insulating material remaining on said substrate; and,

removing said second selected material from the surfaces of said source and drain regions exposed by said openings thereby to allow electrical contact to be made to said source and drain regions.

8. A method as claimed in claim 7 including, between the step of forming the fourth layer of insulating material and the step of forming openings for electrical connections, the step of heating said substrate and the attached materials to smooth out nonuniformities in selected ones of said attached materials.

9. A method of manufacturing a semiconductor device according to claim 7 or 8 in which the shallow surface layers of the source and drain regions are hydrophobic, thereby furnishing a visible indication of when the second selected material overlying the source and drain regions has been completely removed.

10. A method of manufacturing a semiconductor device according to claim 7, 8 or 9 in which the source and drain regions are of P-type conductivity and said second selected material is of an N-type conductivity.

11. A method of manufacturing a semiconductor device according to claim 10 in which boron is the P-type dopant used to give the source and drain regions a P-type conductivity and phosphorus is the N-type dopant used to convert the shallow surface layers of said source and drain regions to N-type conductivity.

12. A method of manufacturing a semiconductor device substantially as hereinbefore dscribed with reference to the accompanying drawings.

13. A semiconductor device when manufactured by a method according to any preceding claim.

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