CLAIMS

What is claimed is:

1. An apparatus, comprising:

a memory operation controller configured to receive memory instructions and decode the same to provide internal signals for performing memory operations for the memory instructions, the memory operation controller further configured to provide information indicative of a time for a variable latency period of a memory instruction during the variable latency period.

2. The apparatus of claim 1 wherein the information related to the time for the variable latency period is selected from a plurality of remaining times for the variable latency period.

3. The apparatus of claim 2 wherein the plurality of remaining times for the variable latency period comprises a short time, a normal time, and a long time.

4. The apparatus of claim 1 wherein the information related to the time for the variable latency period is provided from memory input/outputs.

5. The apparatus of claim 1 wherein the information related to the time for the variable latency period is indicated by a combination of logic states of signals provided by the memory.

6. The apparatus of claim 1 wherein the memory is configured to provide updated information during the variable latency period.

7. An apparatus, comprising:

a memory controller configured to provide memory instructions;

a memory coupled to the memory controller and configured to receive a write instruction therefrom and perform a memory operation responsive thereto, the memory further configured to provide an acknowledgement indicative of an end of a variable latency

period for the write instruction and wait a variable bus turnaround time after the acknowledgement before receiving write data.

8. The apparatus of claim 7 wherein the memory controller is configured to wait a bus turnaround time before providing write data to the memory, the bus turnaround time selected from a plurality of bus turnaround times.

9. The apparatus of claim 7 wherein the memory controller is configured to provide a bus turnaround time end indicator prior to providing write data to the memory.

10. The apparatus of claim 7 wherein the memory controller is configured to provide a bus turnaround time end indicator to the memory on an input/output prior to providing write data to the memory.

11. The apparatus of claim 10 wherein the memory controller is configured to maintain control over the input/output during the variable latency period.

12. The apparatus of claim 7 wherein the memory is configured to provide the acknowledgement to the memory controller on an input/output.

13. A method, comprising:

providing a memory instruction and an address to a memory;

receiving information indicative of a remaining time for a variable latency period for the memory instruction.

14. The method of claim 13 wherein the information indicative of the remaining time for the variable latency period includes a relatively short time, a normal time, or a relatively long time.

15. The method of claim 13, further comprising:

receiving updated information indicative of the remaining time for the variable latency period during the variable latency period.

16. The method of claim 13, further comprising:

managing operations with the memory based at least in part on the information indicative of the remaining time for the variable latency period for the memory instruction.

17. The method of claim 16 wherein managing operation with the memory comprises aborting an operation based at least in part on the information indicative of the remaining time for the variable latency period.

18. The method of claim 16 wherein managing operation with the memory comprises keeping a system bus busy until completion of a memory operation based at least in part on the information indicative of the remaining time for the variable latency period.

19. A method, comprising:

receiving at a memory a write instruction and an address to which write data is to be written;

providing an acknowledgement indicative of an end of a variable latency period for the write instruction; and

waiting a programmable bus turnaround time after the acknowledgement, wherein the programmable bus turnaround time is programmed in the memory; and

receiving the write data for the write instruction after the programmable bus turnaround time.

20. The method of claim 19 wherein the programmable bus turnaround time is a configurable bus turnaround time.

21. The method of claim 19 wherein the programmable bus turnaround time is a variable bus turnaround time.

22. The method of claim 19 wherein the programmable bus turnaround time is selected from one of a plurality of bus turnaround times.

23. The method of claim 19 wherein an end of the programmable bus turnaround time is indicated by a bus turnaround time end indicator.

24. The method of claim 19, further comprising:

receiving a bus turnaround time end indicator before receiving the write data.

25. The method of claim 24 wherein the bus turnaround time end indicator is provided to the memory on an input/output.

CLAIMS

1. A method, comprising:

receiving, at a memory, a write instruction and an address to which write data is to be written;

providing an acknowledgement indicative of an end of a variable latency period for the write instruction;

waiting a programmable bus turnaround time after the acknowledgement, wherein the programmable bus turnaround time is programmed in the memory; and

receiving the write data for the write instruction after the programmable bus turnaround time.

2. The method of claim 1 wherein the programmable bus turnaround time is a configurable bus turnaround time.

3. The method of claim 1 wherein the programmable bus turnaround time is a variable bus turnaround time.

4. The method of claim 1 wherein the programmable bus turnaround time is selected from one of a plurality of bus turnaround times.

5. The method of claim 1 wherein an end of the programmable bus turnaround time is indicated by a bus turnaround time end indicator.

6. The method of claim 1, further comprising:

receiving a bus turnaround time end indicator before receiving the write data.

7. The method of claim 6 wherein the bus turnaround time end indicator is provided to the memory on an input/output.

8. A method, comprising:

providing a memory instruction and an address to a memory;

receiving information indicative of a remaining time for a variable latency period for the memory instruction during the variable latency period;

receiving an acknowledgement indicative of an end of the variable latency period for the memory instruction;

waiting a programmable bus turnaround time after the acknowledgement, wherein the programmable bus turnaround time is programmed in the memory; and

providing data associated with the memory instruction after the programmable bus turnaround time.

9. The method of claim 8 wherein the information indicative of the remaining time for the variable latency period includes a relatively short time, a normal time, or a relatively long time.

10. The method of claim 8, further comprising:

receiving updated information indicative of the remaining time for the variable latency period during the variable latency period.

11. The method of claim 8, further comprising:

managing operations with the memory based at least in part on the information indicative of the remaining time for the variable latency period for the memory instruction.

12. The method of claim 11 wherein managing operation with the memory comprises aborting an operation based at least in part on the information indicative of the remaining time for the variable latency period.

13. The method of claim 11 wherein managing operation with the memory comprises keeping a system bus busy until completion of a memory operation based at least in part on the information indicative of the remaining time for the variable latency period.

14. An apparatus, comprising:

a memory controller configured to provide memory instructions;

a memory coupled to the memory controller and configured to receive a write instruction therefrom and perform a memory operation responsive thereto, the memory further configured to provide an acknowledgement indicative of an end of a variable latency period for the write instruction and wait a programmable bus turnaround time after the acknowledgement before receiving write data, wherein the programmable bus turnaround time is programmed in the memory.

15. The apparatus of claim 14 wherein the memory controller is configured to wait a bus turnaround time before providing write data to the memory, the bus turnaround time selected from a plurality of bus turnaround times.

16. The apparatus of claim 14 wherein the memory controller is configured to provide a bus turnaround time end indicator prior to providing write data to the memory.

17. The apparatus of claim 14 wherein the memory controller is configured to provide a bus turnaround time end indicator to the memory on an input/output prior to providing write data to the memory.

18. The apparatus of claim 17 wherein the memory controller is configured to maintain control over the input/output during the variable latency period.

19. The apparatus of claim 14 wherein the memory is configured to provide the acknowledgement to the memory controller on an input/output.