

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD OF THE SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

5 **[0001]** This application claims priority under 35 U.S.C. §119 to Korean Patent Application No. 10-2023-0041050 filed on March 29, 2023, which is incorporated herein by reference in its entirety.

BACKGROUND

10 **1. Technical Field**

[0002] Embodiments of the present disclosure relate to an electronic device, and more particularly, to a semiconductor device and a manufacturing method of the semiconductor device.

15 **2. Related Art**

[0003] The degree of integration of a semiconductor device is mainly determined by an area occupied by a unit memory cell. Recently, as the improvement in the degree of integration of a semiconductor device for forming memory cells in a single layer on a substrate reaches a limit,
20 a three-dimensional semiconductor device for stacking memory cells on a substrate has been proposed. Furthermore, to improve the operational reliability of such a semiconductor device, various structures and manufacturing methods have been developed.

SUMMARY

[0004] In an embodiment, a semiconductor device may include: a gate structure including drain select lines and word lines; source patterns; source select lines located between the gate structure and the source patterns; a first isolation structure extending between the source patterns and between the source select lines; a second isolation structure extending between the drain select lines; and channel structures extending into the source patterns through the gate structure and the source select lines.

[0005] In an embodiment, a semiconductor device may include: drain select lines; word lines stacked on the drain select lines; source patterns located on the word lines and each including first sidewalls; source select lines located between the word lines and the source patterns and each including second sidewalls aligned with the first sidewalls; and channel structures extending into the source patterns through the drain select lines, the word lines, and the source select lines.

[0006] In an embodiment, a manufacturing method of a semiconductor device may include: forming a source select layer on a substrate; forming a gate structure including word lines and drain select lines on the source select layer; at least partially removing the substrate so that the source select layer is exposed; forming a source layer on the source select layer; etching the source layer to form source patterns; and etching the source select layer to form source select lines

respectively located below the source patterns.

[0007] In an embodiment, a manufacturing method of a semiconductor device may include: forming a first wafer including a substrate, a source select layer, word lines, and drain select lines;
5 forming a second wafer including a peripheral circuit; bonding the first wafer and the second wafer to each other; at least partially removing the substrate so that the source select layer is exposed; forming a source layer on the source select layer; etching the source layer to form source patterns; and etching the source select layer to form source
10 select lines respectively located below the source patterns.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIGS. 1A and 1B are diagrams illustrating the structure of a semiconductor device in accordance with an embodiment.

15 **[0009]** FIG. 2 is a diagram illustrating the structure of a semiconductor device in accordance with an embodiment.

[0010] FIG. 3 is a perspective view illustrating the structure of a semiconductor device in accordance with an embodiment.

[0011] FIGS. 4A and 4B are diagrams illustrating the structure of a semiconductor device in accordance with an embodiment.
20

[0012] FIGS. 5A to 5I are diagrams for describing a manufacturing method of a semiconductor device in accordance with an embodiment.

[0013] FIGS. 6A to 6C are diagrams for describing a manufacturing method of a semiconductor device in accordance with an embodiment.

DETAILED DESCRIPTION

[0014] Various embodiments are directed to a semiconductor device having a stable structure and improved characteristics and a manufacturing method of the semiconductor device.

[0015] By stacking memory cells in three dimensions, it is possible to improve the degree of integration of a semiconductor device. According to the present technology, it is possible to provide a semiconductor device having a stable structure and improved reliability.

[0016] Hereafter, embodiments in accordance with the technical spirit of the present disclosure will be described with reference to the accompanying drawings.

[0017] FIGS. 1A and 1B are diagrams illustrating the structure of a semiconductor device in accordance with an embodiment.

[0018] Referring to FIGS. 1A and 1B, the semiconductor device may include a first wafer WF1 and a second wafer WF2, and may have a structure in which the first wafer WF1 and the second wafer WF2 are bonded to each other. The first wafer WF1 may include a cell array CA, and the second wafer WF2 may include a peripheral circuit PC. The cell array CA may include stacked memory cells. The peripheral circuit PC may include a circuit for driving the cell array CA. As an example, the peripheral circuit PC may include a page buffer, a row-decoder, and the like.

[0019] For reference, at least one of the first wafer WF1 and the

second wafer WF2 might not include a substrate. As an example, after bonding the first wafer WF1 and the second wafer WF2, a substrate of the first wafer WF1 may be removed. The substrate may be completely removed or a partially removed from the first wafer WF1.

5 **[0020]** A substrate of at least one of the first wafer WF1 and the second wafer WF2 may be formed after the bonding of the first wafer WF1 and the second wafer WF2. As an example, a source structure, a metal layer, etc. may serve as the substrate.

[0021] The semiconductor device may include a gate structure GST,
10 source patterns SP, and source select lines SSL. The semiconductor device may further include a dummy structure DST, an insulating layer 12, a first isolation structure IS1, a second isolation structure IS2, a slit structure SLS, channel structures CH, a substrate 10, the peripheral circuit PC, bit lines BL, a first interconnection structure IC1, a second
15 interconnection structure IC2, or a third interconnection structure IC3, or a combination thereof.

[0022] The gate structure GST may include gate lines and insulating layers 11 that are alternately stacked. The gate lines may include word lines WL and drain select lines DSL. The gate lines may each
20 include a conductive material such as polysilicon, tungsten (W), or molybdenum (Mo). The insulating layers 11 may each include an insulating material such as oxide, nitride, or air gap. The gate structure GST may be located between the source select lines SSL and the bit lines BL

[0023] The dummy structure DST may include sacrificial layers 16 and the insulating layers 11 that are alternately stacked. The sacrificial layers 16 may remain without being replaced with gate lines in a manufacturing process. The sacrificial layers 16 may each include a material having a high etching selectivity with respect to the insulating layers 11. As an example, the sacrificial layers 16 may each include nitride and the insulating layers 11 may each include oxide. The insulating layers 11 of the gate structure GST and the insulating layers 11 of the dummy structure DST may be connected to each other.

10 **[0024]** The source patterns SP may be located on the gate structure GST and may extend above the dummy structure DST. The source patterns SP may each include a conductive material such as polysilicon, tungsten (W), or molybdenum (Mo).

[0025] The source select lines SSL may be located between the source patterns SP and the gate structure GST. The source select lines SSL may be located below the source patterns SP, respectively. The source select lines SSL and the source patterns SP may be located or grouped in a one-to-one manner. The source select lines SSL may each have a shape corresponding to the source patterns SP. As an example, the source select lines SSL may be patterned together with the source patterns SP, and may each have substantially the same width as the source patterns SP.

20 **[0026]** The source select lines SSL may each include a conductive material such as polysilicon, tungsten (W), or molybdenum (Mo). As

an example, the source select lines SSL may each include the same material as the source patterns SP, and may each include polysilicon. As an example, the source select lines SSL may each include a material different from that of the source patterns SP and may each include metal, and the source patterns SP may each include polysilicon. FIGS. 1A and 1B illustrate that the source select lines SSL are arranged in a single layer; however, the source select lines SSL may be stacked in multiple layers.

[0027] The insulating layer 12 may be located between the source patterns SP and the source select lines SSL. The source patterns SP and the source select lines SSL may be insulated from each other by the insulating layer 12. The insulating layer 12 may include an insulating material such as oxide or nitride.

[0028] The channel structures CH may be located in the gate structure GST. The channel structures CH may extend into the source patterns SP through the gate structure GST and the source select lines SSL. The channel structure CH may include a channel layer 13. The channel structure CH may further include a memory layer 14 surrounding the channel layer 13 or an insulating core 15 within the channel layer 13, or a combination thereof.

[0029] The memory layer 14 may include a floating gate, polysilicon, a charge trap material, nitride, a variable resistance material, or the like. The memory layer 14 may be located between the channel layer 13 and the gate structure GST and between the channel layer 13 and

the source select line SSL. An end of the channel layer 13 might not be surrounded by the memory layer 14. The end of the channel layer 13 may be located in the source pattern SP and may be connected to the source pattern SP.

5 **[0030]** The channel structures CH may be connected between the source patterns SP and the bit lines BL. Memory cells may be located in regions where the channel structures CH and the word lines WL intersect with each other. Source select transistors may be located in regions where the channel structures CH and the source select lines
10 SSL intersect with each other. Drain select transistors may be located in regions where the channel structures CH and the drain select lines DSL intersect with each other. At least one source select transistor, a plurality of memory cells, and at least one drain select transistor sharing the channel structure CH may constitute one memory string.

15 **[0031]** The first isolation structure IS1 may extend between the source patterns SP and between the source select lines SSL. The source patterns SP located on the same level may be separated from each other by the first isolation structure IS1. The source select lines SSL located on the same level may be separated from each other by
20 the first isolation structure IS1.

[0032] As an example, the first isolation structure IS1 may be located at a boundary between memory blocks. The memory block may be a unit of an erase operation. The source patterns SP and the source select lines SSL may be separated in units of memory blocks by the first

isolation structure IS1. The source patterns SP and the source select lines SSL may be driven in units of memory blocks.

[0033] As an example, the first isolation structure IS1 may be located within the memory block. A sub-memory block may be a smaller unit
5 than the memory block. One memory block may include a plurality of sub-memory blocks. The source patterns SP and the source select lines SSL may be separated in units of sub-memory blocks by the first isolation structure IS1. Through this, a plurality of source patterns SP and a plurality of source select lines SSL may be included in one
10 memory block. The source patterns SP and the source select lines SSL may be driven in units of sub-memory blocks.

[0034] The first isolation structure IS1 may have a uniform width or may have different widths according to levels. The first isolation structure IS1 may have a tapered shape, and a portion of the first
15 isolation structure IS1 overlapping the source select line SSL may have a narrower width than a portion of the first isolation structure IS1 overlapping the source pattern SP. As an example, the first isolation structure IS1 may have a tapered shape in which a lower portion thereof has a narrower width than an upper portion thereof.

[0035] The second isolation structure IS2 may be located in the gate structure GST. The second isolation structure IS2 may extend between the drain select lines DSL. The drain select lines DSL located at the same level may be separated from each other by the second isolation structure IS2. The second isolation structure IS2 may be
20

located at the boundary between the memory blocks or within the memory block. The second isolation structure IS2 may be located in correspondence with the first isolation structure IS1. As an example, the first isolation structure IS1 may be located above the second isolation structure IS2, and the first isolation structure IS1 and the second isolation structure IS2 may be located to face each other with the word lines WL interposed therebetween.

[0036] The second isolation structure IS2 may have a uniform width or may have different widths according to levels. The second isolation structure IS2 may have a tapered shape, and a portion of the second isolation structure IS2 adjacent to the word line WL may have a narrower width than a portion of the second isolation structure IS2 adjacent to the bit line BL. As an example, the second isolation structure IS2 may have a tapered shape in which an upper portion thereof has a narrower width than a lower portion thereof. The first isolation structure IS1 and the second isolation structure IS2 may have tapered shapes in opposite directions.

[0037] The slit structure SLS may extend through the gate structure GST. The slit structure SLS may be located at a boundary between the memory blocks. The gate structure GST may be separated in units of memory blocks by the slit structure SLS. The slit structure SLS may extend into the source select line SSL. The slit structure SLS may be located in correspondence with the first isolation structure IS1, and may be connected to the first isolation structure IS1. As an example, the

first isolation structure IS1 may be located above the slit structure SLS, and a lower surface of the first isolation structure IS1 may come into contact with an upper surface of the slit structure SLS.

[0038] The slit structure SLS may have a uniform width or may have
5 different widths according to levels. The slit structure SLS may have a tapered shape, and a portion of the slit structure SLS adjacent to the source select line SSL may have a narrower width than a portion of the slit structure SLS adjacent to the word line WL. As an example, the slit structure SLS may have a tapered shape in which an upper portion
10 thereof has a narrower width than a lower portion thereof. The first isolation structure IS1 and the slit structure SLS may have tapered shapes in opposite directions.

[0039] The peripheral circuit PC may be located on the substrate 10. The cell array CA of the first wafer WF1 and the peripheral circuit PC of
15 the second wafer WF2 may be electrically connected to each other through the interconnection structure. The interconnection structure may include the first interconnection structure IC1, the second interconnection structure IC2, or the third interconnection structure IC3, or a combination thereof.

[0040] Referring to FIG. 1A, the first interconnection structure IC1
20 may extend through the dummy structure DST, and electrically connect the peripheral circuit PC and the source select lines SSL to each other. The first interconnection structure IC1 may include a contact plug, a wiring line, a bonding pad, and the like. By bonding the first bonding

pad BP1 of the first wafer WF1 to the second bonding pad BP2 of the second wafer WF2, the source select lines SSL of the first wafer WF1 and the peripheral circuit PC of the second wafer WF2 may be electrically connected to each other.

5 **[0041]** Referring to FIG. 1B, the second interconnection structure IC2 may extend through the dummy structure DST, and electrically connect the peripheral circuit PC and the source patterns SP to each other. The second interconnection structure IC2 may include a contact plug, a wiring line, a bonding pad, and the like. By bonding the first bonding
10 pad BP1 of the first wafer WF1 to the second bonding pad BP2 of the second wafer WF2, the source patterns SP of the first wafer WF1 and the peripheral circuit PC of the second wafer WF2 may be electrically connected to each other.

[0042] Referring to FIGS. 1A and 1B, the third interconnection
15 structure IC3 may include the bit lines BL connected to the channel structures CH, and electrically connect the bit lines BL and the peripheral circuit PC to each other. The third interconnection structure IC3 may include a contact plug, a wiring line, a bonding pad, and the like. By bonding the first bonding pad BP1 of the first wafer WF1 to
20 the second bonding pad BP2 of the second wafer WF2, the bit lines BL of the first wafer WF1 and the peripheral circuit PC of the second wafer WF2 may be electrically connected to each other. The source patterns SP and the source select lines SSL may serve as the substrate of the first wafer WF1.

[0043] According to the structure described above, the source patterns SP can be separated from each other by the first isolation structure IS1, and the source select lines SSL can be separated from each other by the first isolation structure IS1. The first isolation structure IS1 can be located at a boundary between memory blocks, and can drive the source pattern SP and the source select line SSL in units of memory blocks. The first isolation structure IS1 may be located within the memory block, and can drive the source pattern SP and the source select line SSL in units of sub-memory blocks. Through this, biases of the source pattern SP and the source select line SSL can be controlled in units of memory blocks or in units of sub-memory blocks, and operating characteristics of a source select transistor can be improved. It is also possible to improve disturbance of a program operation and a read operation.

[0044] FIG. 2 is a diagram illustrating the structure of a semiconductor device in accordance with an embodiment. Hereinafter, content previously described is not repeated.

[0045] Referring to FIG. 2, the semiconductor device may include a first wafer WF1 and a second wafer WF2, and may have a structure in which the first wafer WF1 and the second wafer WF2 are bonded to each other. The first wafer WF1 may include a cell array CA, and the second wafer WF2 may include a peripheral circuit PC.

[0046] The semiconductor device may include a gate structure GST, source patterns SP, a first isolation structure IS1, a second isolation

structure IS2, a slit structure SLS, channel structures CH, a substrate 20, the peripheral circuit PC, or bit lines BL, or a combination thereof.

[0047] The gate structure GST may include gate lines and insulating layers 21 that are alternately stacked. The gate lines may include word lines WL, drain select lines DSL, and source select lines SSL. The gate structure GST may be located between the source patterns SP and the bit lines BL. The source patterns SP may be located on the gate structure GST.

[0048] The source select lines SSL may be located below the source patterns SP, respectively. As an example, the source select lines SSL may each include the same material as or a different material from the source patterns SP. As an example, the source patterns SP may each include polysilicon, and the source select lines SSL may each include metal.

[0049] The channel structures CH may be located in the gate structure GST. The channel structures CH may extend into the source patterns SP through the drain select lines DSL, the word lines WL, and the source select lines SSL. The channel structure CH may include a channel layer 23. The channel structure CH may further include a memory layer 24 surrounding the channel layer 23 and an insulating core 25 within the channel layer 23.

[0050] The first isolation structure IS1 may be located in the gate structure GST. The first isolation structure IS1 may extend between the source patterns SP and between the source select lines SSL. The

source patterns SP located on the same level may be separated from each other by the first isolation structure IS1. The source select lines SSL located on the same level may be separated from each other by the first isolation structure IS1. The first isolation structure IS1 may
5 be located at a boundary between memory blocks or within the memory block.

[0051] The second isolation structure IS2 may be located in the gate structure GST. The second isolation structure IS2 may extend between the drain select lines DSL. The drain select lines DSL located
10 on the same level may be separated from each other by the second isolation structure IS2. The second isolation structure IS2 may be located at the boundary between the memory blocks or within the memory block. The second isolation structure IS2 may be located in correspondence with the first isolation structure IS1.

15 **[0052]** The slit structure SLS may extend through the gate structure GST. The slit structure SLS may be located at the boundary between the memory blocks. The gate structure GST may be separated in units of memory blocks by the slit structure SLS.

[0053] The peripheral circuit PC may be located on the substrate 10.
20 The cell array CA of the first wafer WF1 and the peripheral circuit PC of the second wafer WF2 may be electrically connected to each other through the interconnection structure. The third interconnection structure IC3 may include the bit lines BL, and may electrically connect the bit lines BL and the peripheral circuit PC to each other. The source

patterns SP may serve as the substrate of the first wafer WF1.

[0054] According to the structure described above, the source select lines SSL can be located in the gate structure GST. The source patterns SP can be separated from each other by the first isolation structure IS1. Furthermore, the first isolation structure IS1 can extend into the gate structure GST and separate the source select lines SSL from each other.

[0055] FIG. 3 is a perspective view illustrating the structure of a semiconductor device in accordance with an embodiment.

10 Hereinafter, content previously described is not repeated.

[0056] Referring to FIG. 3, a source pattern SP may include a first sidewall SW1, a source select line SSL may include a second sidewall SW2, and an insulating layer 32 may include a third sidewall SW3. The first sidewall SW1, the second sidewall SW2, and the third sidewall SW3 may contact a sidewall SW of a first isolation structure IS1.

15 **[0057]** The first sidewall SW1, the second sidewall SW2, and the third sidewall SW3 may be etched surfaces defined by an etching process for forming the first isolation structure IS1. The etched surface may have a vertical profile or an inclined profile. The second sidewall SW2 may be aligned with the first sidewall SW1. The first sidewall SW1 and the second sidewall SW2 may have substantially the same slope. The third sidewall SW3 may be aligned with the first sidewall SW1 and/or the second sidewall SW2. The third sidewall SW3 may have substantially the same slope as the first sidewall SW1 and/or the second sidewall

20

SW2.

[0058] FIGS. 4A and 4B are diagrams illustrating the structure of a semiconductor device in accordance with an embodiment. Hereinafter, descriptions may be made without repeating content already described above.

[0059] Referring to FIGS. 4A and 4B, the semiconductor device may include source patterns SP, source select lines SSL, drain select lines DSL, first isolation structures IS1, second isolation structures IS2, and a slit structure SLS.

10 **[0060]** Referring to FIG. 4A, the slit structure SLS may be located at a boundary between memory blocks MB. The second isolation structures IS2 may be located within the memory block MB. The first isolation structure IS1 may be located at the boundary between the memory blocks MB. Accordingly, the source patterns SP may be
15 separated in units of memory blocks MB, and may be driven in units of memory blocks MB. The source select lines SSL may be separated in units of memory blocks MB, and may be driven in units of memory blocks MB.

[0061] Referring to FIG. 4B, each memory block MB may include a
20 plurality of sub-memory blocks Sub_MB. The slit structure SLS may be located at the boundary between the memory blocks MB. The second isolation structures IS2 may be located within the memory block MB. The first isolation structures IS1 may be located at the boundary between the memory blocks MB and within the memory blocks MB.

Accordingly, the source patterns SP may be separated in units of sub-memory blocks Sub_MB, and may be driven in units of sub-memory blocks Sub_MB. The source select lines SSL may be separated in units of sub-memory blocks Sub_MB, and may be driven in units of sub-memory blocks Sub_MB.

[0062] According to the structure described above, the first isolation structures IS1 can be located in correspondence with the slit structures SLS, or can be located in correspondence with the slit structures SLS and the second isolation structure IS2. Accordingly, the source patterns SP and the source select lines SSL can be driven in units of memory blocks MB or in units of sub-memory blocks Sub_MB.

[0063] FIGS. 5A to 5I are diagrams for describing a manufacturing method of a semiconductor device in accordance with an embodiment. Hereinafter, descriptions may be made without repeating content already described above.

[0064] Referring to FIG. 5A, an insulating layer 41 may be formed on a substrate 40. The insulating layer 41 may include an insulating material such as oxide or nitride. A source select layer 42 may be formed on the substrate 40. The source select layer 42 may be located on the insulating layer 41, and the substrate 40 and the source select layer 42 may be insulated from each other by the insulating layer 41. The source select layer 42 may be used to form a source select line. The source select layer 42 may include a conductive material such as polysilicon, tungsten (W), or molybdenum (Mo). FIG. 5A illustrates

that the source select layer 42 is a single layer; however, the source select layer 42 may be stacked in multiple layers.

[0065] Subsequently, a stack ST may be formed on the source select layer 42. The stack ST may include first material layers 43 and second material layers 44 that are alternately stacked. The first material layers 43 may be used to form gate lines, and the second material layers 44 may be used to form insulating layers. As an example, the first material layers 43 may each include a sacrificial material such as nitride, and the second material layers 44 may each include an insulating material such as oxide. As an example, the first material layers 43 may each include a conductive material such as polysilicon or metal, and the second material layers 44 may each include an insulating material such as an oxide.

[0066] The first material layers 43 and the second material layers 44 may have substantially the same thickness or different thicknesses. As an example, the lowermost second material layer 44 among the second material layers 44 may have a thicker thickness than the other second material layers 44. Through this, it is possible to prevent or reduce damage to the first material layers 43 when the source select layer 42 is patterned in a subsequent process.

[0067] The stack ST may include a cell region CR and a contact region CTR. The cell region CR may be a region where memory cells are to be stacked and a memory string is to be located. The contact region CTR may be a region where an interconnection structure is to be

located. A bias may be transferred through the interconnection structure to drive the memory string.

[0068] Referring to FIG. 5B, channel structures CH may be formed in the stack ST. The channel structures CH may be located in the cell region CR of the stack ST. The channel structures CH may extend through the stack ST and the source select layer 42. The channel structures CH may extend into the substrate 40 through the insulating layer 41. As an example, first openings OP1 may be formed in the stack ST, and a memory layer 46, a channel layer 45, and an insulating core 47 may be formed in the first openings OP1. The memory layer 46 may include a blocking layer, a data storage layer, and a tunneling layer, or a combination thereof. The data storage layer may include a floating gate, polysilicon, a charge trap material, nitride, a variable resistance material, or the like. Electrode structures may be formed instead of the channel structures CH. The electrode structures may each include a vertical electrode layer instead of the channel layer 45.

[0069] Subsequently, a slit SL may be formed in the stack ST. The slit SL may extend through the stack ST. The slit SL may expose the source select layer 42 or may extend into the source select layer 42. The slit SL may also extend to the insulating layer 41 or the substrate 40. The slit SL may be located at a boundary between memory blocks, and the stack ST may be separated in units of memory blocks by the slit SL.

[0070] When the first openings OP1 are formed, the slits SL may be

formed together. In such a case, a sacrificial layer may be formed in the slit SL, and the channel structure CH may be formed in the first openings OP1. Subsequently, the slit SL may be reopened by removing the sacrificial layer.

5 **[0071]** Subsequently, the first material layers 43 may be replaced with third material layers 43A through the slit SL. As an example, conductive layers may be formed after the first material layers 43 are removed through the slits SL. Through this, a gate structure GST including the second material layers 44 and third material layers 43A
10 that are alternately stacked may be formed. The third material layers 43A may be gate lines. As an example, the third material layers 43A may be word lines or drain select layers. As an example, at least one uppermost third material layer 43A may be a drain select layer, and the other third material layers 43A may be word lines.

15 **[0072]** Some of the first material layers 43 may remain without being replaced with the third material layers 43A. The first material layers 43 may remain on at least a part of the contact region CTR. A dummy structure DST may be defined by the remaining first material layers 43. The dummy structure DST may be located in the contact region CTR.
20 The dummy structure DST may include the first material layers 43 and the second material layers 44 that are alternately stacked. The second material layers 44 of the gate structure GST and the second material layers 44 of the dummy structure DST may be connected to each other.

[0073] When the first material layers 43 each include a conductive

material, the first material layers 43 may also be used as gate lines. In such a case, the gate structure GST may include the first material layers 43 and the second material layers 44 that are alternately stacked. As an example, when the first material layers 43 each include
5 polysilicon, a silicidation process or the like may be performed to reduce the specific resistance of the first material layers 43.

[0074] Subsequently, a slit structure 48 may be formed in the slit SL. The slit structure 48 may extend into the source select layer 42 through the gate structure GST. The slit structure 48 may include an insulating
10 material such as oxide, nitride, or air gap. The slit structure 48 may also include a source contact structure and an insulating spacer surrounding sidewalls of the source contact structure.

[0075] Subsequently, a second isolation structure 49 may be formed. As an example, after a second opening OP2 is formed in the gate
15 structure GST, the second isolation structure 49 may be formed in the second opening OP2. The drain select layer may be separated into drain select lines by the second isolation structure 49. The second isolation structure 49 may extend between the drain select lines. The second isolation structure 49 may be located at the boundary between
20 the memory blocks or within the memory block. The second isolation structure 49 may include an insulating material such as oxide, nitride, or air gap. The second isolation structure 49 may have a shallower depth than the slit structure 48. The formation order of the second isolation structure 49 and the slit structure 48 may be changed. After

the second isolation structure 49 is formed, the slit structure 48 may be formed.

[0076] Subsequently, first contact plugs 50 and second contact plugs 51 may be formed in the dummy structure DST. The first contact plugs 50 and the second contact plugs 51 may be located in the contact region CTR. As an example, third openings OP3 may be formed in the dummy structure DST, and conductive layers may be formed in the third openings OP3, respectively. The first contact plugs 50 and the second contact plugs 51 may be used to form an interconnection structure electrically connecting a first wafer and a second wafer to each other. The first contact plugs 50 and the second contact plugs 51 may extend into the source select layer 42 through the dummy structure DST.

[0077] When the first openings OP1 or the slits SL are formed, the third openings OP3 may be formed together. In such a case, a sacrificial layer may be formed in the third openings OP3, and the channel structure CH may be formed in the first openings OP1 or the slit structure 48 may be formed in the slits SL. Subsequently, the third openings OP3 may be reopened by removing the sacrificial layer.

[0078] Referring to FIG. 5C, interconnection structures 52 to 54 and a first interlayer dielectric layer 56 may be formed. The interconnection structures 52 to 54 may be located in the first interlayer dielectric layer 56, and the first interlayer dielectric layer 56 may be a single layer or a multilayer. The first interlayer dielectric layer 56 may include an etch stop layer used when the interconnection structures 52

to 54 are formed. As an example, the first interlayer dielectric layer 56 may have a structure in which an oxide layer and an etch stop layer are alternately stacked.

[0079] The interconnection structure 52 electrically connected to the first contact plug 50 may be formed. The interconnection structure 53 electrically connected to the second contact plug 51 may be formed. The interconnection structure 54 connected to the channel structures CH may be formed. The interconnection structures 52 to 54 may each include a contact plug, a wiring line, and the like. As an example, the interconnection structure 54 may include bit lines connected to the channel structures CH.

[0080] Subsequently, first bonding pads 55 connected to the interconnection structures 52 to 54 may be formed. Through this, a first wafer WF1 including a cell array CA may be formed.

[0081] Referring to FIG. 5D, a peripheral circuit 61 may be formed on a substrate 60. The peripheral circuit 61 may include a page buffer, a row-decoder, a complementary metal-oxide semiconductor (CMOS) circuit, and the like.

[0082] Subsequently, interconnection structures 62 to 64 and a second interlayer dielectric layer 66 may be formed. The interconnection structures 62 to 64 may be located in the second interlayer dielectric layer 66, and the second interlayer dielectric layer 66 may be a single layer or a multilayer. The second interlayer dielectric layer 66 may include an etch stop layer used when the

interconnection structures 62 to 64 are formed. As an example, the second interlayer dielectric layer 66 may have a structure in which an oxide layer and an etch stop layer are alternately stacked. The interconnection structures 62 to 64 may be electrically connected to the peripheral circuit 61. Subsequently, second bonding pads 65 connected to the interconnection structures 62 to 64 may be formed. Through this, a second wafer WF2 including the peripheral circuit 61 may be formed.

[0083] Referring to FIG. 5E, the first wafer WF1 and the second wafer WF2 may be bonded to each other. The first bonding pad 55 and the second bonding pad 65 may be bonded to each other at a bonding interface IF. The first wafer WF1 may be reversed and bonded so that the first wafer WF1 is located above the second wafer WF2. Through this, the first wafer WF1 including the substrate 40, the source select layer 42, and the gate structure GST and the second wafer WF2 including the peripheral circuit 61 may be electrically connected to each other.

[0084] Subsequently, the substrate 40 may be at least partially removed. In consideration of subsequent processes, structural stability, and the like, only a part of the substrate 40 or the entire substrate 40 may be removed. As an example, after a rear surface of the substrate 40 is planarized or ground, the substrate 40 may be removed by performing a wet etching process. The planarization process may be performed using a chemical mechanical polish (CMP)

method. Through this, the insulating layer 41 may be exposed. Furthermore, the channel structure CH may protrude from the insulating layer 41.

5 **[0085]** Subsequently, the channel layer 45 may be exposed by etching the memory layer 46. As an example, the memory layer 46 may be removed by a dry cleaning process. Subsequently, the channel layer 45 may be doped with impurities. As an example, impurities may be implanted into the channel layer 45 by using an ion implantation process. Through this, a threshold voltage of a source select transistor
10 may be adjusted.

[0086] Referring to FIG. 5F, a source layer 67 may be formed. The source layer 67 may be formed by depositing a conductive material such as polysilicon or metal. As an example, after a polysilicon layer is deposited, a heat treatment process using a laser or the like may be
15 performed to activate the polysilicon layer. The source layer 67 may be directly connected to the channel layer 45.

[0087] Referring to FIGS. 5G and 5H, source patterns 67A and source select lines 42A may be formed. The source select lines 42A may be located below the source patterns 67A, respectively. Through this, the
20 source patterns 67A and the source select lines 42A may be separated in units of memory block or in units of sub-memory block.

[0088] First, referring to FIG. 5G, a mask pattern 68 may be formed on the source layer 67. Subsequently, the source patterns 67A may be formed by etching the source layer 67 using the mask pattern 68 as

an etching barrier. Subsequently, the source select lines 42A may be formed by etching the source select layer 42 using the mask pattern 68 and/or the source patterns 67A as an etching barrier. Fourth openings OP4 may be formed between the source patterns 67A and between the source select lines 42A. The fourth openings OP4 may be formed at the boundary between the memory blocks or within the memory block.

[0089] The fourth openings OP4 may have different depths, different shapes, and the like depending on positions. A fourth opening OP4A may be located in correspondence with the second isolation structure 49. The fourth opening OP4A and the second isolation structure 49 may be located to face each other with the word lines interposed therebetween. The fourth opening OP4A may be located at the boundary between the memory blocks or within the memory block. The fourth opening OP4A may have a depth by which the second material layer 44 is exposed. The source patterns 67A on both sides may be separated from each other and the source select lines 42A may be separated from each other by the fourth opening OP4A.

[0090] A fourth opening OP4B may be located in correspondence with the slit structure 48. The fourth opening OP4B may be located at the boundary between the memory blocks. The fourth opening OP4B may have a depth by which the slit structure 48 is exposed. As an example, a bottom surface of the fourth opening OP4B may be located between an upper surface and a lower surface of the source select line 42A or may be located in the gate structure GST.

[0091] When the fourth openings OP4 are formed, a portion of the source layer 67 and the source select layer 42 formed in the contact region CTR may be at least partially removed. Through this, the dummy structure DST may be at least partially exposed, and at least one of the first contact plugs 50 and the second contact plugs 51 may be exposed.

[0092] Referring to FIG. 5H, first isolation structures 69 may be formed in the fourth openings OP4, respectively. The first isolation structures 69 may extend between the source patterns 67A and between the source select lines 42A. The first isolation structures 69 may include an insulating material such as oxide, nitride, or air gap. The first isolation structures 69A may be located in correspondence with the second isolation structure 49. The first isolation structure 69B may be located in correspondence with the slit structure 48.

[0093] Referring to FIG. 5I, interconnection structures 72 and 73 and an interlayer dielectric layer 71 may be formed. The interconnection structures 72 and 73 may be located in the interlayer dielectric layer 71, and the interlayer dielectric layer 71 may be a single layer or a multilayer. The interconnection structure 72 may be electrically connected to the first contact plug 50, and the interconnection structure 73 may be electrically connected to the second contact plug 51.

[0094] Through this, a first interconnection structure IC1 of electrically connecting the source select lines 42A and the peripheral circuit 61 to each other may be formed. A bias may be individually

applied to the source select lines 42A through the first interconnection structure IC1, and the source select lines 42A may be individually driven. A second interconnection structure IC2 of electrically connecting the source patterns 67A and the peripheral circuit 61 to each other may be formed. A bias may be individually applied to the source patterns 67A through the second interconnection structure IC2, and the source patterns 67A may be individually driven.

[0095] According to the manufacturing method described above, after the first wafer WF1 and the second wafer WF2 are bonded to each other, the source layer 67 and the source select layer 42 may be patterned together. Accordingly, compared to a case where the source layer 67 and the source select layer 42 are patterned in separate processes, the number of mask patterns used in a manufacturing process can be reduced and the manufacturing cost can be reduced. Since the first wafer WF1 and the second wafer WF2 are bonded to each other, an interconnection structure can be simplified. Furthermore, the source layer 67 and the source select layer 42 may be separated in units of memory block or in units of sub-memory block. Accordingly, operating characteristics of the source select lines 42A can be improved, and disturbance of a program operation or a read operation can be improved.

[0096] FIGS. 6A to 6C are diagrams for describing a manufacturing method of a semiconductor device in accordance with an embodiment. Hereinafter, descriptions may be made without repeating content

already described above.

[0097] Referring to FIG. 6A, a first wafer WF1 may be formed. The first wafer WF1 may include a substrate 80, a source select layer 82SS, word lines 82W, drain select lines 82D, and channel structures CH. The
5 first wafer WF1 may further include a slit structure 88, a second isolation structure 89, a first interlayer dielectric layer 84, bit lines BL, or first bonding pads 83, or a combination thereof.

[0098] First, a gate structure GST may be formed on the substrate 80. The gate structure GST may include source select layers 82SS,
10 drain select lines 82D, and word lines 82W. As an example, the gate structure GST may include gate lines and insulating layers 81 that are alternately stacked. Among the gate lines, at least one uppermost gate line may be a drain select line 82D, at least one lowermost gate line may be the source select layer 82SS, and the other gate lines may
15 be the word lines 82W.

[0099] The channel structures CH may be located in the gate structure GST. The channel structures CH may extend into the substrate 80 through the drain select lines 82D, the word lines 82W, and the source select layer 82SS. The channel structures CH may each include a
20 channel layer 85, a memory layer 86, and an insulating core 87, or a combination thereof.

[00100] A slit structure 88 may be located in the gate structure GST. The gate structure GST may be separated in units of memory blocks by the slit structure 88. A second isolation structure 89 may be located

in the gate structure GST. The drain select lines 82D may be separated in units of memory blocks or in units of sub-memory blocks by the second isolation structure 89.

[00101] Subsequently, an interconnection structure including bit lines BL, the first interlayer dielectric layer 84, and the first bonding pads 83 may be formed.

[00102] Referring to FIG. 6B, a second wafer WF2 including a peripheral circuit 91 may be formed. The second wafer WF2 may include a substrate 90, the peripheral circuit 91, an interconnection structure 92, a second interlayer dielectric layer 94, and a second bonding pad 93, or a combination thereof.

[00103] Subsequently, the first wafer WF1 and the second wafer WF2 may be bonded to each other, and the substrate 80 may be at least partially removed. Through this, the gate structure GST may be exposed. The channel structure CH may protrude from a surface of the gate structure GST. The slit structures 88 may protrude from the surface of the gate structure GST. Alternatively, in the process of removing the substrate 80, the slit structures 88 may be etched and may be exposed by the surface of the gate structure GST. Subsequently, the memory layer 86 may be etched to expose the channel layer 85. Subsequently, a source layer 97 may be formed on the gate structure GST. The source layer 97 may be connected to the channel structures CH exposed by removing the substrate 80.

[00104] Referring to FIG. 6C, source patterns 97A may be formed by

etching the source layer 97. The source select layer 82SS may be etched to form source select lines 82S. Subsequently, first isolation structures 99 extending between the source patterns 97A and between the source select lines 82S may be formed. A first isolation structure
5 99A may be located in correspondence with the second isolation structure 89. A first isolation structure 99B may be located in correspondence with the slit structure 88.

[00105] According to the manufacturing method described above, the gate structure GST may be formed to include the source select lines
10 82S. After the first wafer WF1 and the second wafer WF2 are bonded to each other, the source patterns 97A and the source select lines 82S may be formed in units of memory blocks or in units of sub-memory blocks. Accordingly, operating characteristics of the source select lines 82S can be improved, and disturbance of a program operation or a read
15 operation can be improved.

[00106] Although embodiments according to the technical idea of the present disclosure have been described above with reference to the accompanying drawings, this is only for explaining the embodiments according to the concept of the present disclosure, and the present
20 disclosure is not limited to the above embodiments. Various types of substitutions, modifications, and changes for the embodiments may be made by those skilled in the art, to which the present disclosure pertains, without departing from the technical idea of the present disclosure defined in the following claims, and it should be construed

that these substitutions, modifications, and changes belong to the scope of the present disclosure.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:
 - a gate structure including drain select lines and word lines;
 - 5 source patterns;
 - source select lines located between the gate structure and the source patterns;
 - a first isolation structure extending between the source patterns and between the source select lines;
 - 10 a second isolation structure extending between the drain select lines; and
 - channel structures extending into the source patterns through the gate structure and the source select lines.
- 15 2. The semiconductor device of claim 1, wherein the source select lines are located below the source patterns, respectively.
3. The semiconductor device of claim 1, wherein the source patterns include first sidewalls and the source select lines include
20 second sidewalls aligned with the first sidewalls.
4. The semiconductor device of claim 3, further comprising:
 - insulating layers located between the source patterns and the source select lines and including third sidewalls aligned with the first

sidewalls and the second sidewalls.

5 5. The semiconductor device of claim 1, further comprising:
 a slit structure extending through the gate structure and
connected to the first isolation structure.

6. The semiconductor device of claim 5, wherein the slit
structure is located at a boundary between memory blocks.

10 7. The semiconductor device of claim 5, wherein the slit
structure extends into the source select line.

8. The semiconductor device of claim 5, wherein the first
isolation structure and the slit structure have tapered shapes that taper
15 in opposite directions from one another.

9. The semiconductor device of claim 1, wherein the second
isolation structure is located in correspondence with the first isolation
structure.

20

10. The semiconductor device of claim 9, wherein the first
isolation structure and the second isolation structure are located within
a memory block.

11. The semiconductor device of claim 1, further comprising:
a peripheral circuit;
a dummy structure located on the peripheral circuit; and
a first interconnection structure extending through the dummy
5 structure and electrically connecting the peripheral circuit and the
source select lines to each other.

12. The semiconductor device of claim 11, further comprising:
a second interconnection structure extending through the dummy
10 structure and electrically connecting the peripheral circuit and the
source patterns to each other.

13. The semiconductor device of claim 11, further comprising:
a third interconnection structure including bit lines connected to
15 the channel structures and connecting the bit lines and the peripheral
circuit.

14. The semiconductor device of claim 1, wherein the first
isolation structure and the second isolation structure have tapered
20 shapes that taper in opposite directions from one another.

15. A semiconductor device comprising:
drain select lines;
word lines stacked on the drain select lines;

source patterns located on the word lines and including first sidewalls;

source select lines located between the word lines and the source patterns and including second sidewalls aligned with the first sidewalls;

5 and

channel structures extending into the source patterns through the drain select lines, the word lines, and the source select lines.

16. The semiconductor device of claim 15, further comprising:
10 a first isolation structure extending between the source patterns and between the source select lines and located at a boundary between memory blocks or within the memory block.

17. The semiconductor device of claim 15, further comprising:
15 a second isolation structure extending between the drain select lines and located at a boundary between memory blocks or within the memory block.

18. The semiconductor device of claim 15, further comprising:
20 a slit structure extending through the drain select lines, the word lines, and the source select lines and located at a boundary between memory blocks.

19. The semiconductor device of claim 15, wherein the source

select lines have substantially the same width as the source patterns.

20. A manufacturing method of a semiconductor device, the manufacturing method comprising:

- 5 forming a source select layer on a substrate;
- forming a gate structure including word lines and drain select lines on the source select layer;
- at least partially removing the substrate to expose the source select layer;
- 10 forming a source layer on the source select layer;
- forming source patterns by etching the source layer; and
- forming source select lines by etching the source select layer, wherein the source select lines are located below the source patterns, respectively.

15

21. The manufacturing method of claim 20, further comprising:

 forming a first separation structure extending between the source patterns and between the source select lines.

20

22. The manufacturing method of claim 20, further comprising:

 forming a second isolation structure extending between the drain select lines.

23. The manufacturing method of claim 22, further comprising:

5 forming a first isolation structure extending between the source patterns and between the source select lines and located in correspondence with the second isolation structure.

24. The manufacturing method of claim 20, further comprising:

10 forming a slit structure extending into the source select layer through the gate structure.

25. The manufacturing method of claim 24, further comprising:

15 forming a first isolation structure extending between the source patterns and between the source select lines and located in correspondence with the slit structure.

26. The manufacturing method of claim 20, further comprising:

20 bonding a first wafer including the substrate, the source select layer, and the gate structure to a second wafer including a peripheral circuit.

27. The manufacturing method of claim 26, wherein the source layer and the source select layer are etched after the first wafer and the second wafer are bonded to each other.

5 28. The manufacturing method of claim 26, further comprising:

forming a first interconnection structure electrically connecting the peripheral circuit and the source select lines to each other.

10 29. The manufacturing method of claim 26, further comprising:

forming a second interconnection structure electrically connecting the peripheral circuit and the source patterns to each other.

15 30. The manufacturing method of claim 20, wherein the source layer and the source select layer are etched and separated in units of memory blocks or in units of sub-memory blocks.

20 31. The manufacturing method of claim 20, further comprising:

forming a mask pattern on the source layer,
wherein the source layer and the source select layer are etched using the mask pattern as an etching barrier.

32. A manufacturing method of a semiconductor device, the manufacturing method comprising:

forming a first wafer including a substrate, a source select layer, word lines, and drain select lines;

5 forming a second wafer including a peripheral circuit;

bonding the first wafer and the second wafer to each other;

at least partially removing the substrate so that the source select layer is exposed;

forming a source layer on the source select layer;

10 forming source patterns by etching the source layer; and

forming source select lines by etching the source select layer, wherein the source select lines are located below the source patterns, respectively.

15 33. The manufacturing method of claim 32, wherein forming the first wafer comprises:

forming the source select layer on the substrate; and

forming a gate structure including the word lines and the drain select lines on the source select layer.

20

34. The manufacturing method of claim 32, wherein forming the first wafer comprises:

forming a gate structure including the source select layer, the word lines, and the drain select lines on the substrate.

35. The manufacturing method of claim 32, further comprising:

forming a mask pattern on the source layer,

5 wherein the source layer and the source select layer are etched using the mask pattern as an etching barrier.