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(71) Applicant (for all designated States except US): **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL];
Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **COENEN, Mart**
[NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

(74) Agents: **ELEVELD, Koop, J.** et al.; Prof. Holstlaan 6,
NL-5656 AA Eindhoven (NL).

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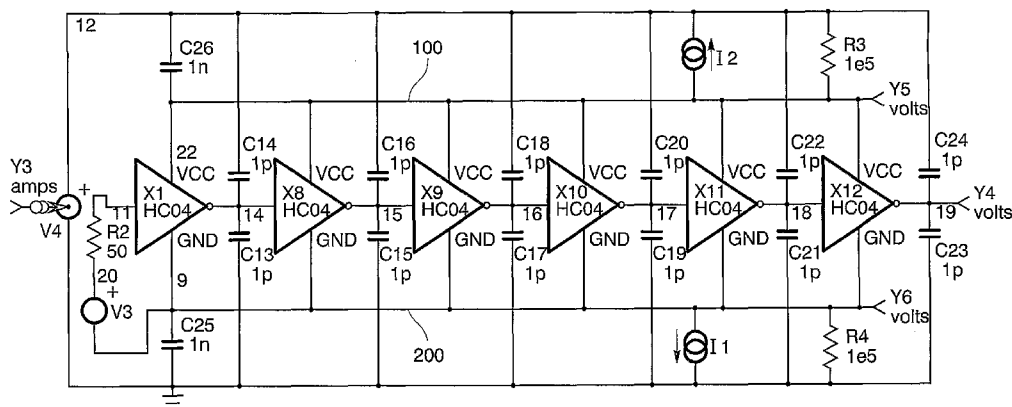
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(54) Title: ADIABATIC CMOS DESIGN



(57) Abstract: An integrated circuit comprising a plurality of CMOS modules (10) connected in series with each other, each module (10) being connected between first and second reference lines (Vdd, Vss). A first transistor (54) is provided between at least one of the modules (10) and the first reference line (Vdd) and a second transistor (52) is provided between one of the modules (10) and the second reference line (Vss) and capacitors (C25, C26) are provided in parallel with the transistors (52, 54) such that they are driven as current sources (I1, I2). As a result power dissipation and leakage current is reduced.