CLAIMS

1. A semiconductor structure, comprising:

a substrate, having a plurality of word line trenches and source/drain regions each adjacent to each word line trench; and

a plurality of word lines, each located in each word line trench and each comprising a first conductive layer, an ovonic threshold switching (OTS) gating material layer and a second conductive layer stacked in sequence, wherein, the first conductive layer is located at a bottom of the word line trench; a projection of the word line on a sidewall of the word line trench and a projection of a source/drain region on the sidewall of the word line trench have an overlapping region with a preset height; and in the case that a voltage applied to the word line is less than a preset voltage, a resistance of the OTS gating material layer is greater than a preset resistance, such that the first conductive layer and the second conductive layer are electrically disconnected.

2. The semiconductor structure according to claim 1, wherein a projection of at least part of the second conductive layer on the sidewall of the word line trench is located within the projection of the source/drain region on the sidewall of the word line trench.

3. The semiconductor structure according to claim 2, wherein a top of the first conductive layer is lower than a bottom of the source/drain region.

4. The semiconductor structure according to claim 2 or 3, wherein a top of the second conductive layer is flush with a top of the source/drain region.

5. The semiconductor structure according to claim 2, wherein the projection of the source/drain region on the sidewall of the word line trench covers a projection of the second conductive layer on the sidewall of the word line trench.

6. The semiconductor structure of claim 1, wherein the preset resistance is a critical resistance of electrical conduction of the first conductive layer and the second conductive layer.

7. The semiconductor structure according to any one of claims 1 to 3, wherein the OTS gating material layer comprises a first resistance and a second resistance, wherein the first resistance is greater than the second resistance; in the case that the OTS gating material layer is in a conductive state, the resistance of the OTS gating material layer is the second resistance; and in the case that the OTS gating material layer is in an off state, the resistance of the OTS gating material layer is the first resistance.

8. The semiconductor structure according to claim 7, wherein a conductive current of the OTS gating material layer is 10^{-4} A or more, and a conductive voltage is 1.2 V or more.

9. The semiconductor structure of claim 1, wherein the OTS gating material layer is a silicon telluride (SiTe) layer.

10. The semiconductor structure according to claim 7, wherein a thickness of the OTS gating material layer is 5 nm to 25 nm.

11. The semiconductor structure according to claim 10, wherein the thickness of the OTS gating material layer is 15nm.

12. The semiconductor structure according to any one of claims 1 to 3, wherein the first conductive layer and/or the second conductive layer is a conductive metal layer.

13. The semiconductor structure according to claim 12, wherein the first conductive layer and/or the second conductive layer is a tungsten (W) layer.

14. A manufacturing method of a semiconductor structure, comprising:

providing a substrate, on which a plurality of word line trenches and source/drain regions are formed, where each of the source/drain regions is adjacent to each of the word line trench;

forming a first conductive layer in each of the word line trench;

forming a OTS gating material layer on the first conductive layer; and

forming a second conductive layer on the OTS gating material layer, wherein the first conductive layer, the OTS gating material layer and the second conductive layer form a word line, and a projection of the word line on a sidewall of the word line trench and a projection of the source/drain region on the sidewall of the word line trench have an overlapping region with a preset height.