WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a stacked structure including a plurality of conductive layers and a plurality of interlayer insulating layers, which are alternately stacked on a substrate;

stepped grooves provided in the stacked structure, the stepped grooves having different depths from each other; and

an opening portion penetrating through the stacked structure to expose the substrate, the opening portion having at least one step on a sidewall thereof having a height corresponding to a depth difference between two of the stepped grooves.

2. The semiconductor memory device of claim 1, wherein the opening portion penetrates the stacked structure in a third direction and wherein the opening portion has a larger width in a first direction and in a second direction as the distance from the substrate increases in the third direction.

3. The semiconductor memory device of claim 1, wherein each of the stepped grooves includes a step structure with a plurality of steps, each of the steps having the same height as the vertical pitch of the conductive layers, and

a depth difference between the stepped grooves has a size of K

times of the vertical pitch of the conductive layers,

wherein K is a natural number which is greater than 2 and less than N + 1,

wherein each of the stepped grooves has a step structure including a plurality of steps, and N is the number of the steps included in the step structure.

4. The semiconductor memory device of claim 1, further comprising a slit separating the stacked structure into first and second memory blocks, and wherein the opening portion is connected to the slit.

5. The semiconductor memory device of claim 4, wherein the opening portion does not divide the interlayer insulating layers and the conductive layers of the first and second memory blocks.

6. The semiconductor memory device of claim 1,

wherein the substrate comprises a cell region where a plurality of channel layers penetrating the stacked structure is located and a first connection region where one end of the stacked structure is located, and

wherein the stepped grooves and the opening portion are disposed at the first connection region.

7. The semiconductor memory device of claim 1,

wherein the substrate comprises first and second cell regions

spaced apart from each other in a first direction where a plurality of channel layers penetrating the stacked structure is located, and a second connection region which is disposed between the first and the second cell regions, and

wherein the stepped grooves and the opening portion are disposed at the first connection region.

8. The semiconductor memory device of claim 7, further comprising a slit extending along the first direction and separating the stacked structure into first and second memory blocks, and

wherein the stepped grooves and the opening portion do not divide the interlayer insulating layers and the conductive layers of the first and second memory blocks.

9. The semiconductor memory device of claim 1, further comprising an insulating layer filling in the opening portion; and

a contact plug penetrating the insulating layer and connected to either the substrate or a lower wiring line provided over a base layer under-laying the substrate.

10. A semiconductor memory device comprising:

a memory structure including a plurality of channel layers protruding in a vertical direction on a substrate, a plurality of interlayer insulating layers and a plurality of conductive layers which are alternately

stacked along the channel layers on the substrate;

a logic structure disposed on a base layer under the substrate, the logic structure including a logic circuit and lower wiring lines electrically connected to the logic circuit;

stepped grooves provided in a stacked structure including the interlayer insulating layers and the conductive layers, the stepped grooves having different depths from each other;

an opening portion penetrating the stacked structure to contact the substrate and including steps on sidewalls, the steps having heights corresponding to depth differences between the stepped grooves; and

a contact plug penetrating an insulating layer filling in the opening portion, the contact plug contacting one of the lower wiring lines.

11. The semiconductor memory device of claim 10, wherein the substrate includes a plurality of cell regions and connection regions alternately disposed along a first direction on the substrate, and

wherein the channel layers are disposed in the cell region and the opening portion is disposed in one of the connection regions.

12. The semiconductor memory device of claim 11, wherein elements included in the logic circuit are distributively disposed at the plurality of cell regions,

wherein the lower wiring lines are connected to the elements included in the logic circuit, and

wherein the length of each of the lower wiring lines in the first direction is shorter than the length of each of the cell regions in the first direction.

13. A method of manufacturing a semiconductor device, the method comprising:

forming a pre-stack by alternately stacking first material layers and second material layers on a substrate;

forming a plurality of stepped grooves each having a step structure in the pre-stack;

recessing the stepped grooves to have different depths from each other;

forming an opening portion in the pre-stack, the opening portion having steps with heights corresponding to depth differences between the stepped grooves on sidewalls.

14. The method of claim 13, wherein the recessing the stepped grooves and the forming the opening portion are simultaneously performed.

15. The method of claim 13, wherein the forming of the stepped grooves includes:

forming a first mask pattern including a plurality of first openings on the pre-stack;

etching the pre-stack by using the first mask pattern; and

performing a trimming process widening the widths of the first openings,

wherein the etching of the pre-stack and the performing of the trimming process are alternately repeated.

16. The method of claim 15, wherein in the etching of the pre-stack, the etching depth corresponds to a vertical pitch of the first material layer.

17. The method of claim 13, wherein the forming of the opening portion includes;

forming a second mask pattern including second openings exposing at positions corresponding to at least one of the stepped grooves and the opening portion;

increasing depths of the stepped grooves exposed by the second mask pattern by a first depth and forming a trench of the first depth at a position corresponding to the opening portion, by first etching the pre-stack using the second mask pattern as an etch mask;

forming a third mask pattern including third openings exposing at least one of the stepped grooves and the trench; and

increasing depths of the trench and stepped grooves exposed by the third mask pattern by a second depth, by second etching the pre-stack using the third mask pattern as an etch mask.

18. The method of claim 17, wherein an area of the second opening of the second mask pattern exposing the stepped groove is larger than an entrance area of the stepped groove.

19. The method of claim 17, wherein an area of the third opening of the third mask pattern exposing the recessed stepped groove is larger than an entrance area of the recessed stepped groove, and the area of the third opening of the third mask pattern exposing the trench is larger than an entrance of the trench.

20. The method of claim 17, wherein the etching depths of the first etching and the second etching are K times the vertical pitch of the first material layer,

wherein K is a natural number which is greater than 2 and less than N + 1, and

wherein N is the number of steps of the step structure.

21. A semiconductor memory device comprising:

first and second memory blocks separated by a slit, each memory block including a stacked structure including a plurality of conductive layers and a plurality of interlayer insulating layers alternately stacked on a substrate;

a plurality of stepped grooves formed in a first connection region of

the stacked structure of each memory block, the stepped grooves having different depths from each other ; and

a plurality of opening portions penetrating through the stacked structure of each memory block to expose the substrate, the opening portions having at least one step on a sidewall thereof having a height corresponding to a depth difference between two of the stepped grooves and disposed between consecutive stepped grooves,

at least one contact plug extending through each of the opening portions to connect an upper wiring line formed above the stacked structure with a lower wiring line formed below the stacked structure.

Claims

1. A method of manufacturing a semiconductor device, the method comprising:

forming a pre-stack by alternately stacking first material layers and second material layers on a substrate;

forming a plurality of stepped grooves each having a step structure in the pre-stack;

recessing the stepped grooves to have different depths from each other;

forming an opening portion in the pre-stack, the opening portion having at least one step on a sidewall thereof having a same height as a depth difference between two of the stepped grooves.

2. The method of claim 1, wherein the recessing the stepped grooves and the forming the opening portion are simultaneously performed.

3. The method of claim 1, wherein the forming of the stepped grooves includes:

forming a first mask pattern including a plurality of first openings on the pre-stack;

etching the pre-stack by using the first mask pattern; and

performing a trimming process widening the widths of the first openings,

wherein the etching of the pre-stack and the performing of the trimming process are alternately repeated.

4. The method of claim 3, wherein in the etching of the pre-stack, the etching depth corresponds to a vertical pitch of the first material layer.

5. The method of claim 1, wherein the forming of the opening portion includes;

forming a second mask pattern including second openings exposing at positions corresponding to at least one of the stepped grooves and the opening portion;

increasing depths of the stepped grooves exposed by the second mask pattern by a first depth and forming a trench of the first depth at a position corresponding to the opening portion, by first etching the pre-stack using the second mask pattern as an etch mask;

forming a third mask pattern including third openings exposing at least one of the stepped grooves and the trench; and

increasing depths of the trench and stepped grooves exposed by the third mask pattern by a second depth, by second etching the pre-stack using the third mask pattern as an etch mask.

6. The method of claim 5, wherein an area of the second opening of the second mask pattern exposing the stepped groove is larger than an entrance area of the stepped groove.

7. The method of claim 5, wherein an area of the third opening of the third mask pattern exposing the recessed stepped groove is larger than an entrance area of the recessed stepped groove, and the area of the third opening of the third mask pattern exposing the trench is larger than an entrance of the trench.

8. The method of claim 5, wherein the etching depths of the first etching and the second etching are K times the vertical pitch of the first material layer,

wherein K is a natural number which is greater than 2 and less than N+1, and

wherein N is the number of steps of the step structure.