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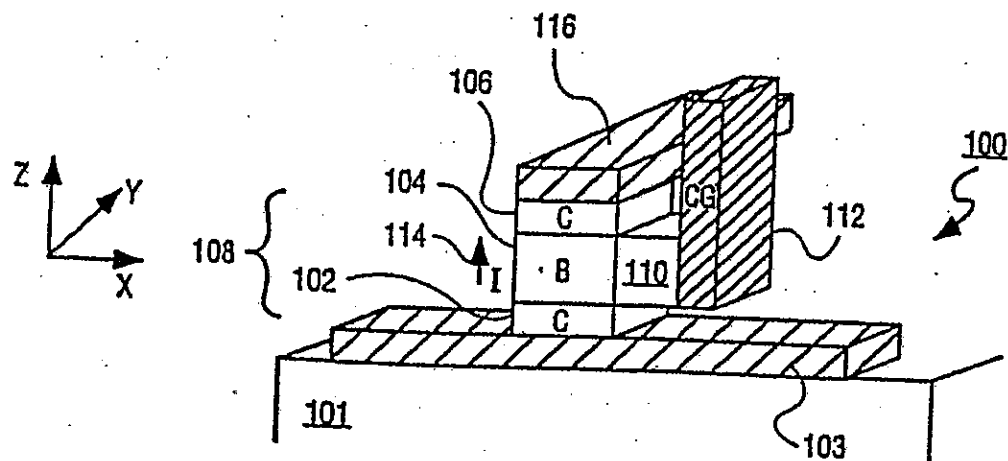


FIG. 1A

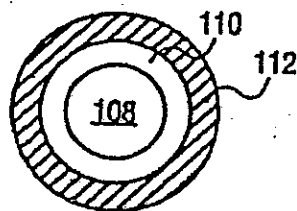


FIG. 1B

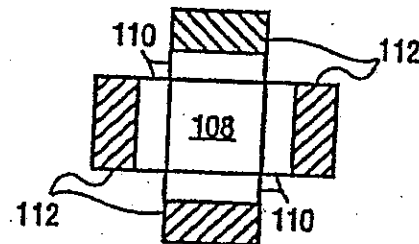


FIG. 1C

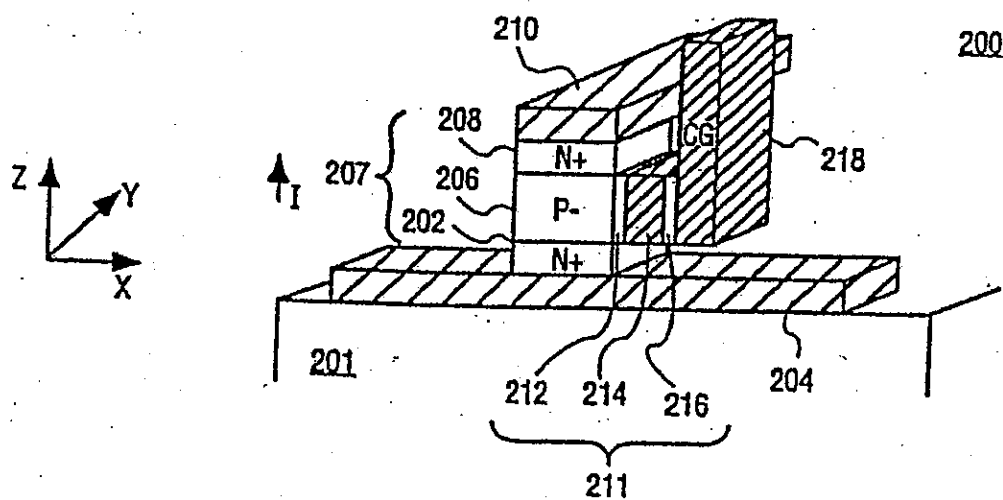
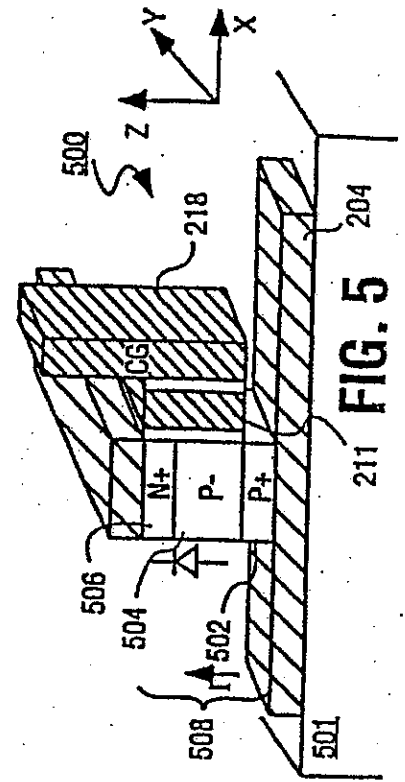
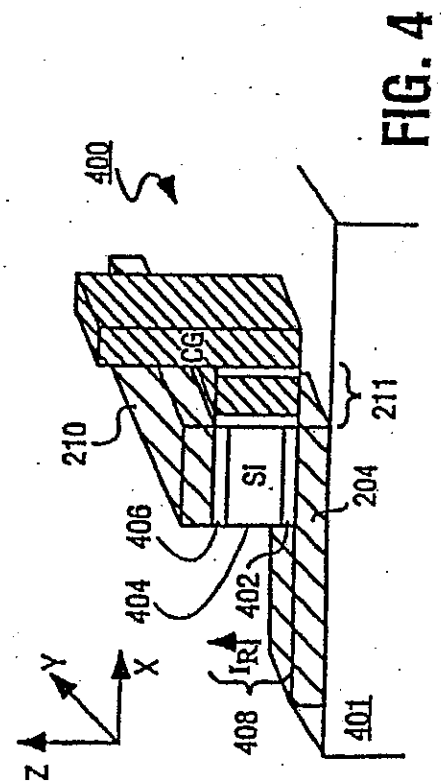
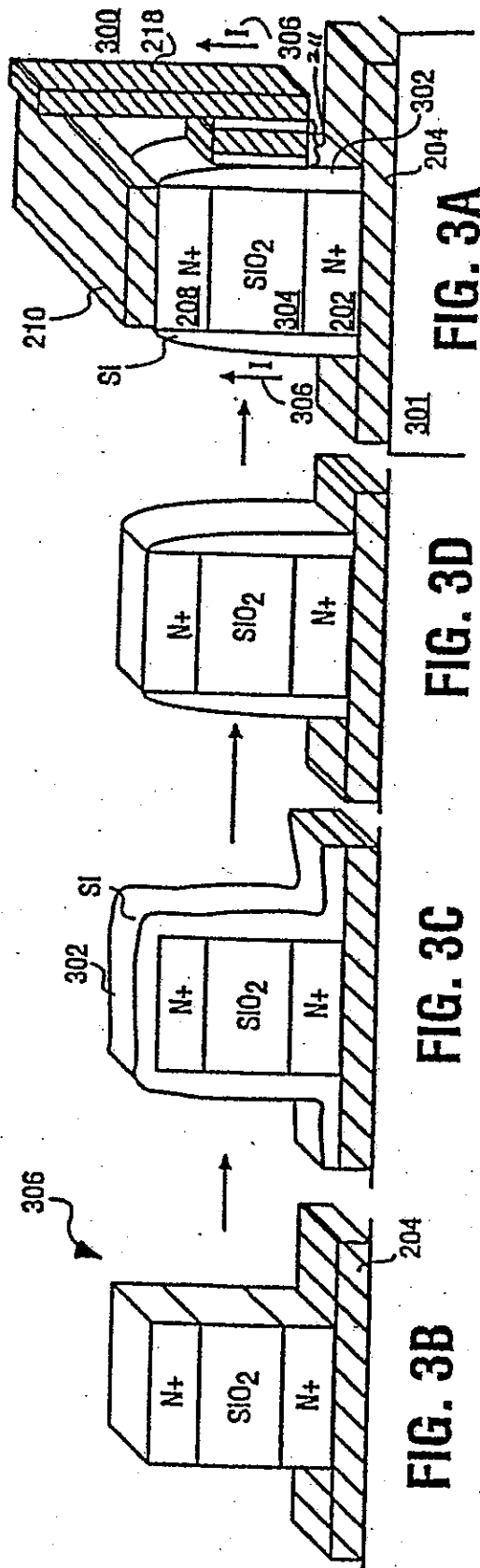


FIG. 2



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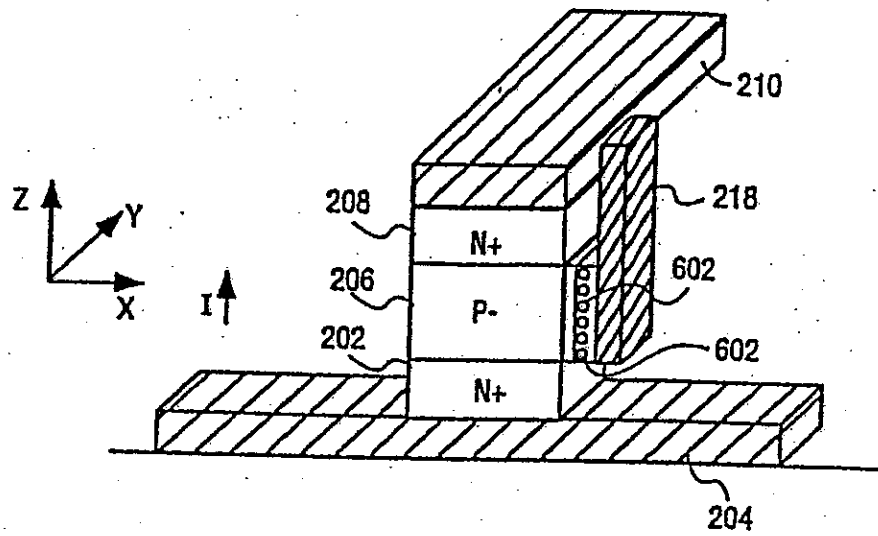


FIG. 6

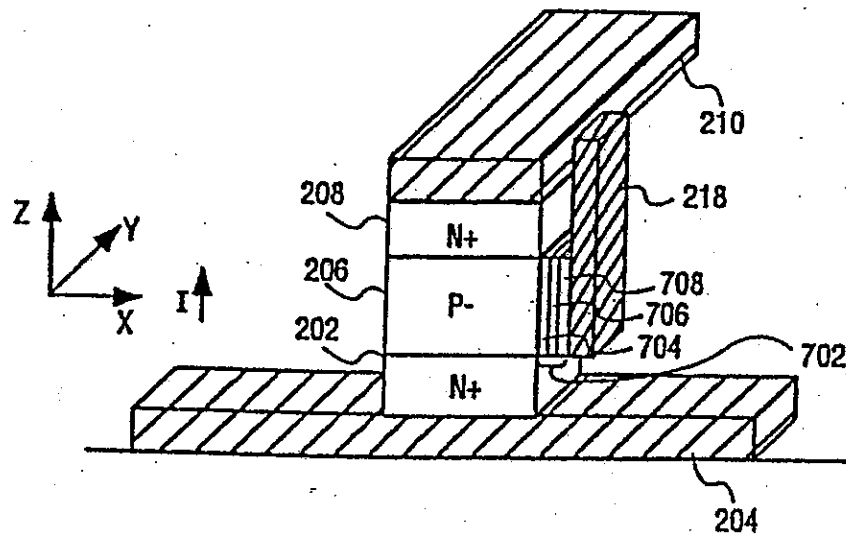


FIG. 7

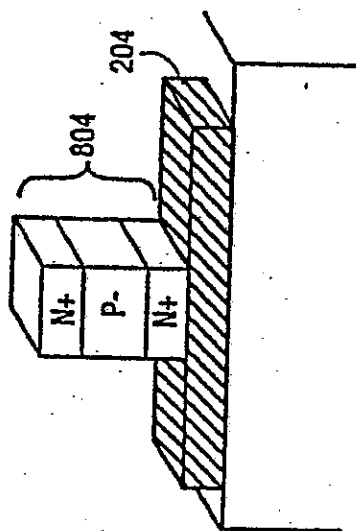


FIG. 8B

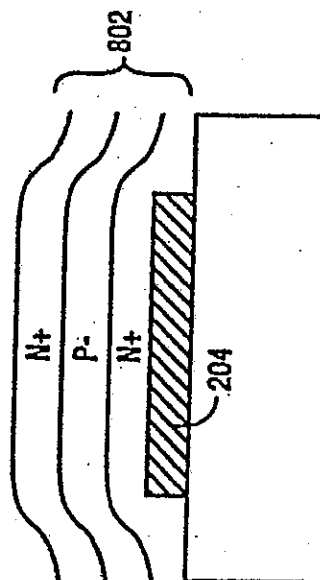


FIG. 8A

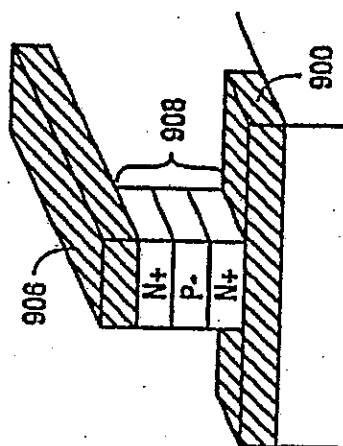


FIG. 9B

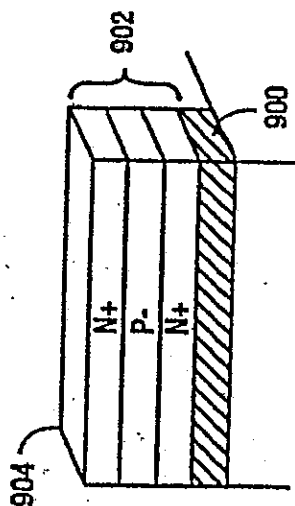


FIG. 9A

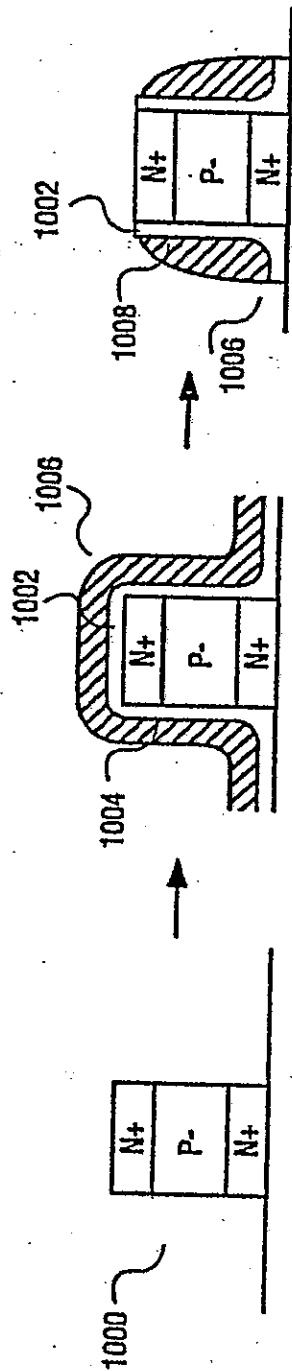


FIG. 10A

FIG. 10B

FIG. 10C

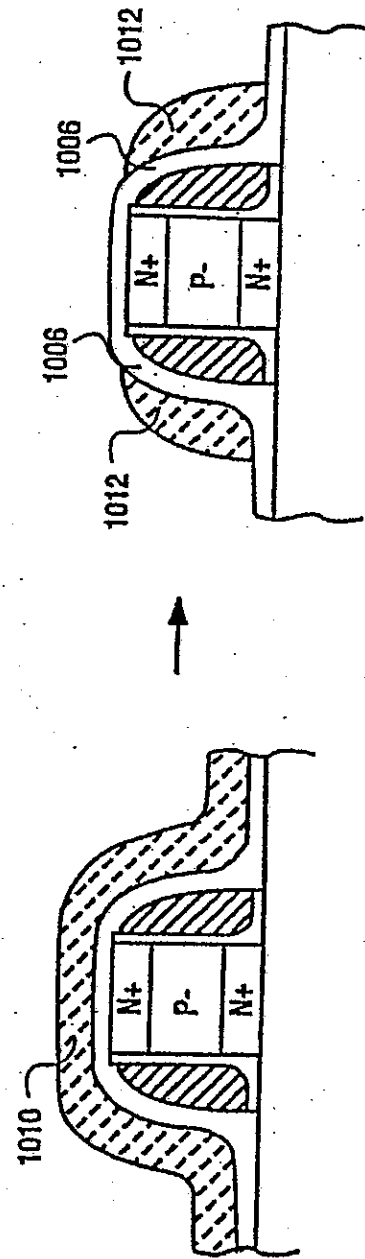


FIG. 10D

FIG. 10E

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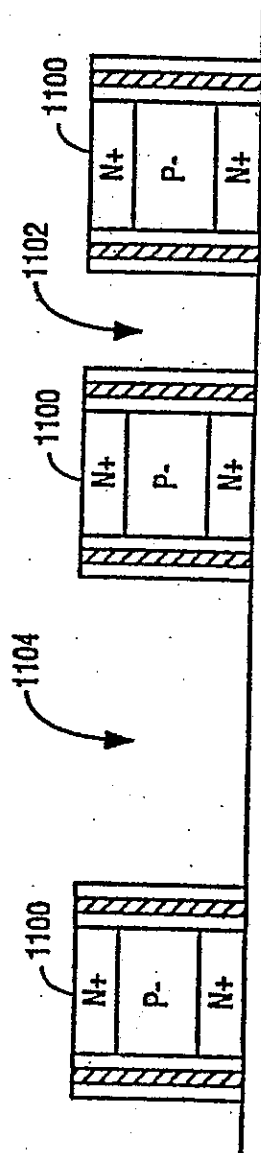


FIG. 11A

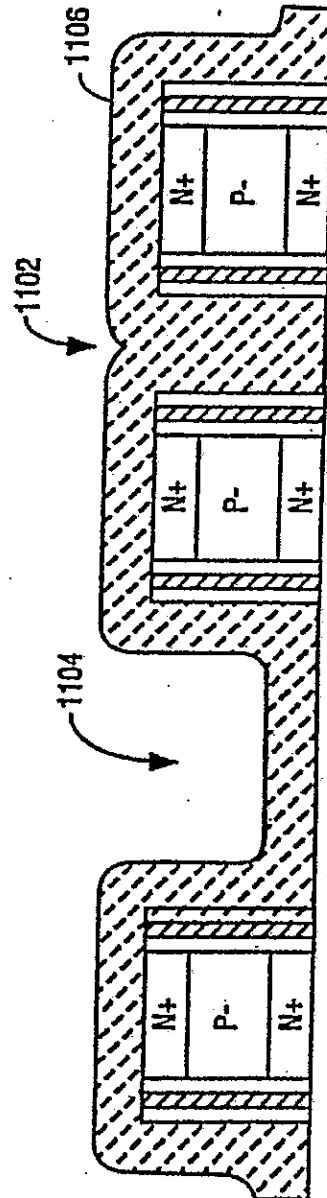


FIG. 11B

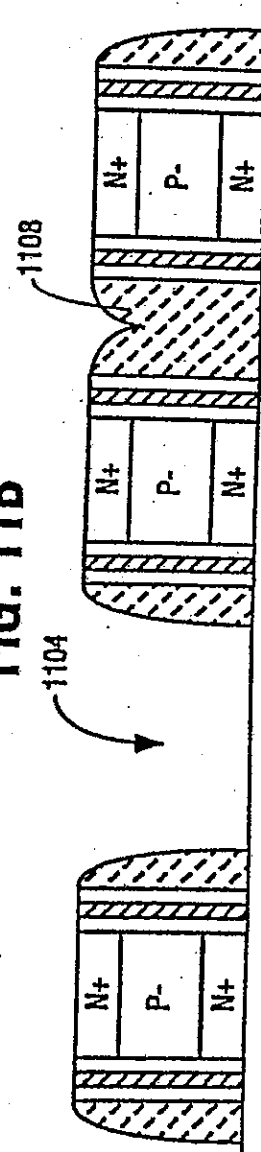


FIG. 11C

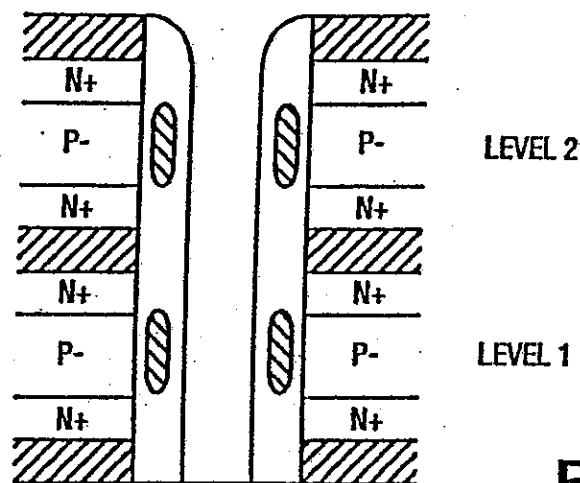


FIG. 12A

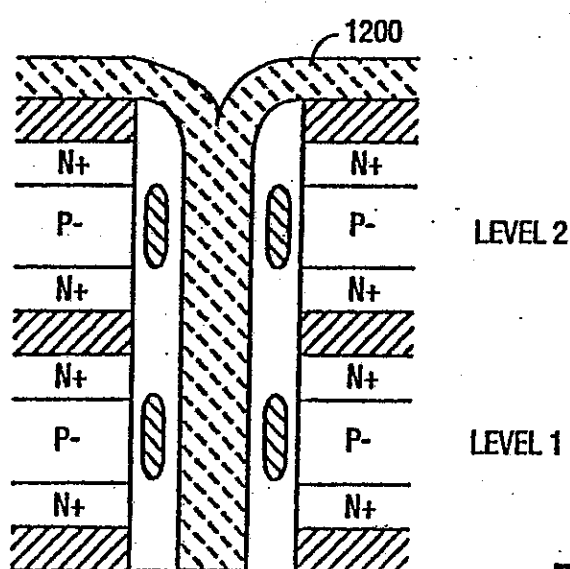


FIG. 12B

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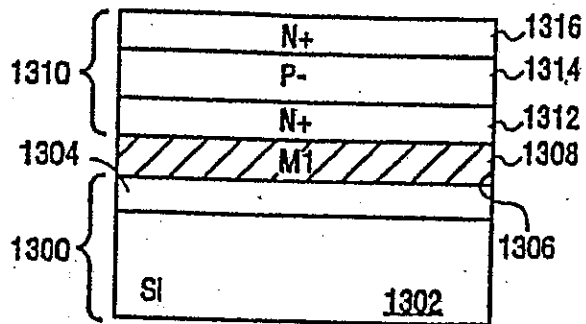


FIG. 13A

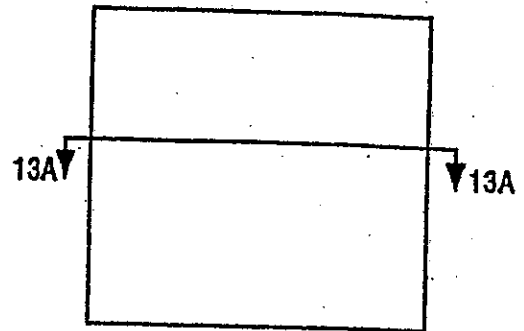


FIG. 13B

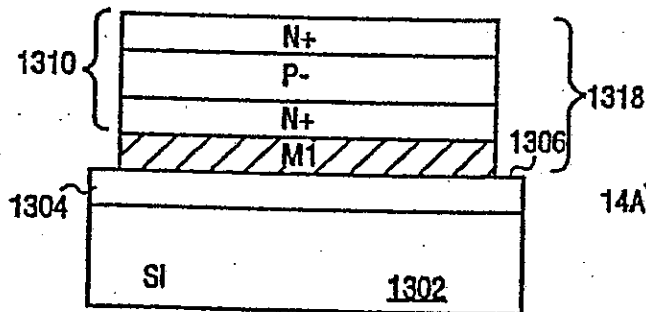


FIG. 14A

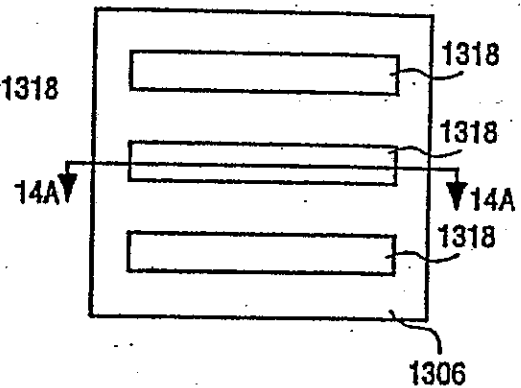


FIG. 14B

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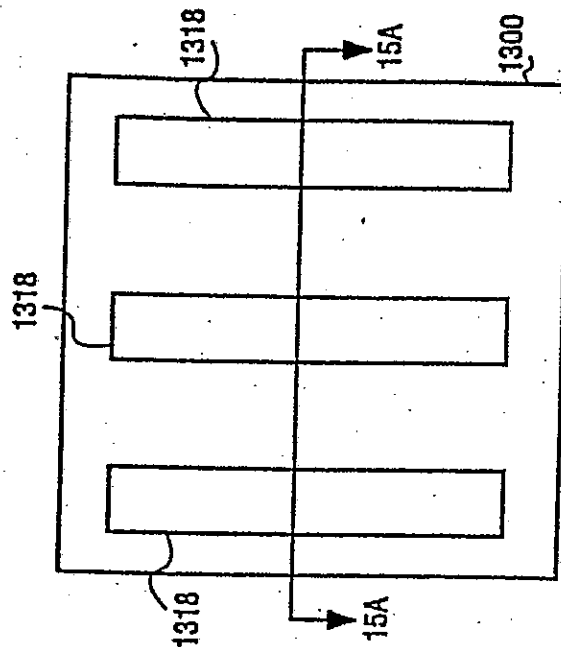


FIG. 15B

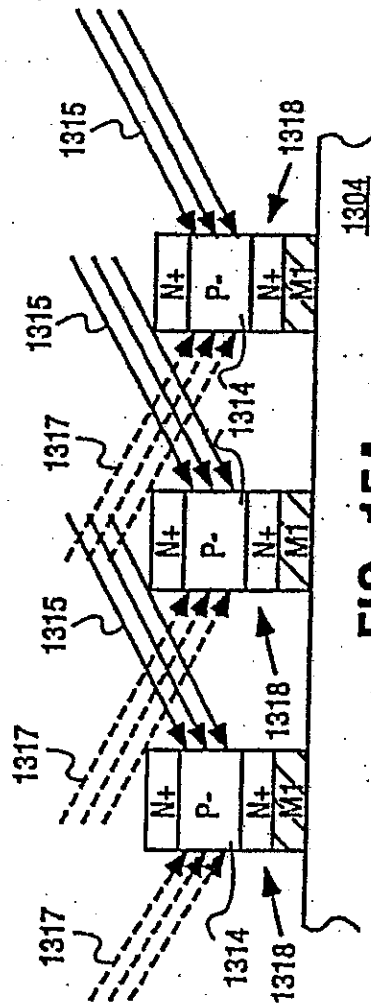


FIG. 15A

II/85 °

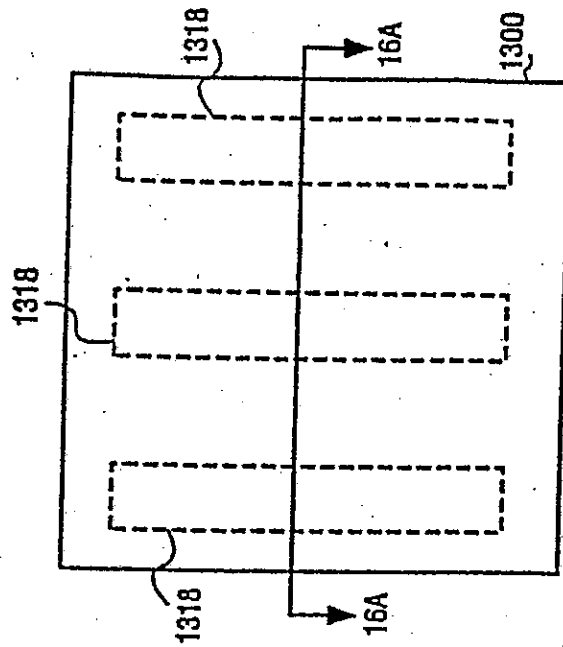


FIG. 16B

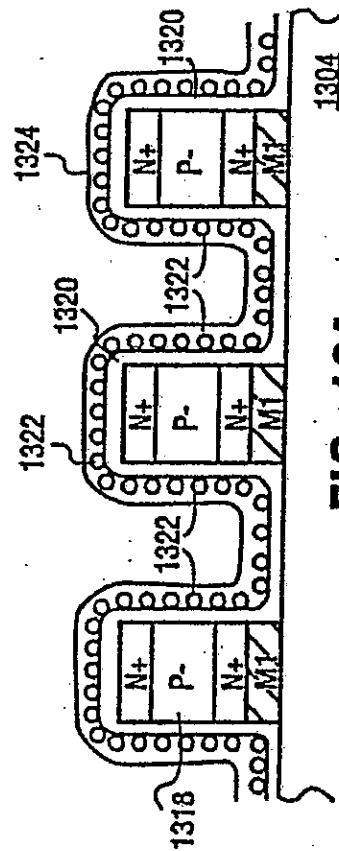


FIG. 16A

12/85

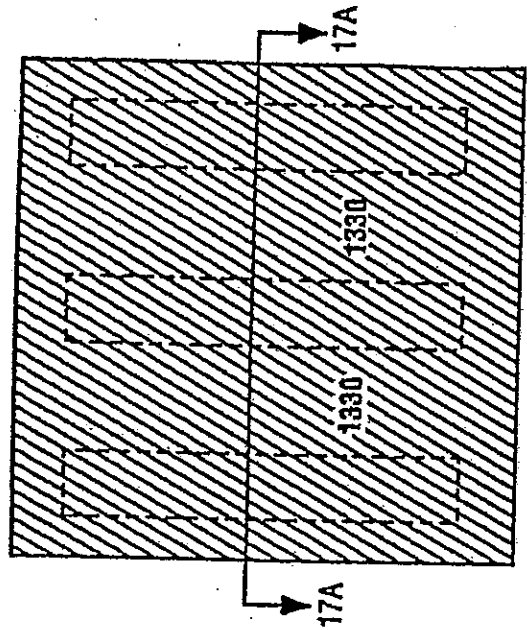


FIG. 17B

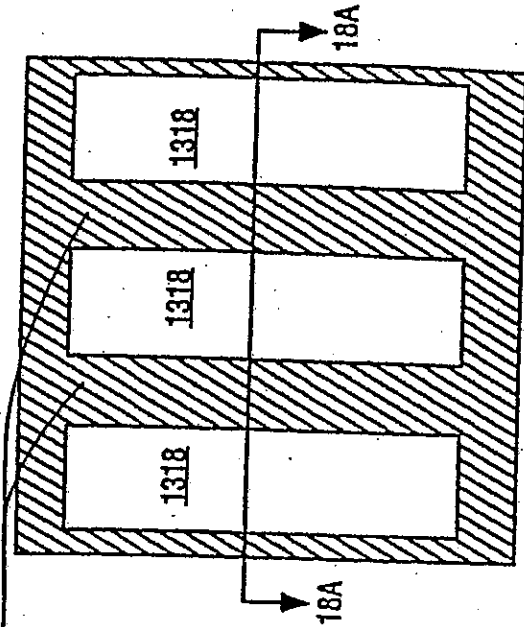


FIG. 18B

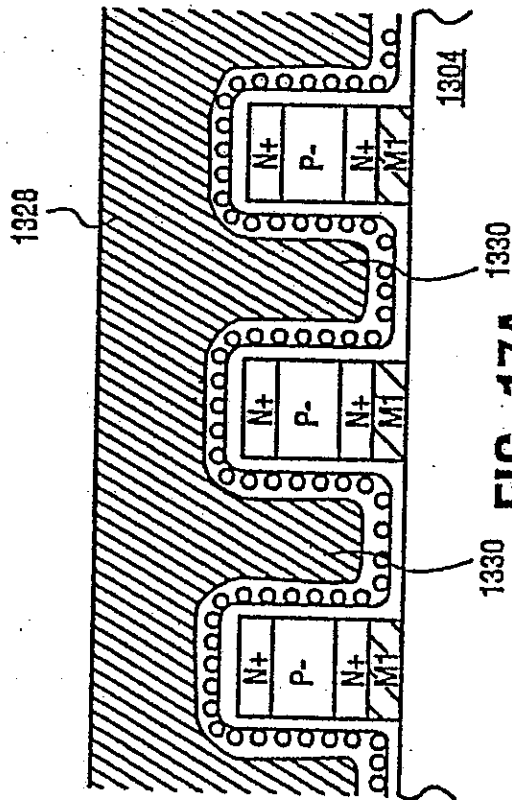


FIG. 17A

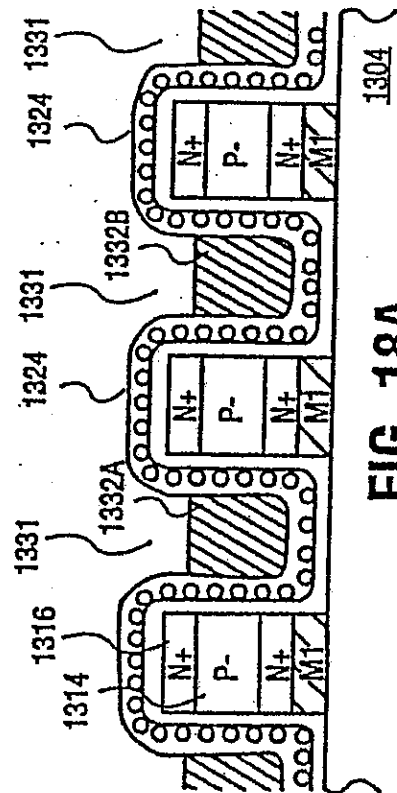


FIG. 18A

13 / 85 °

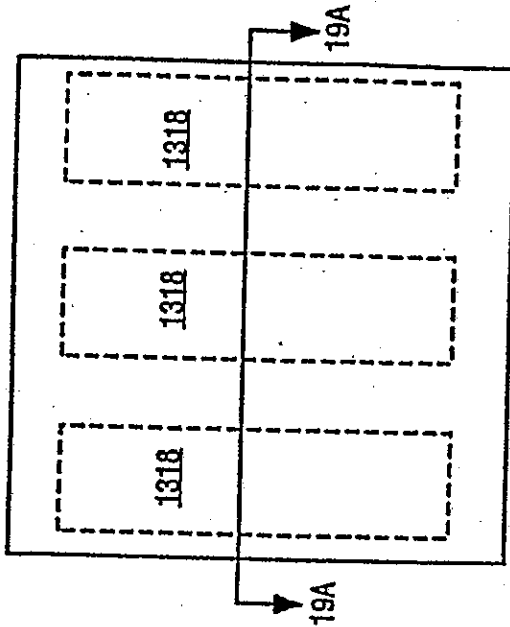


FIG. 19B

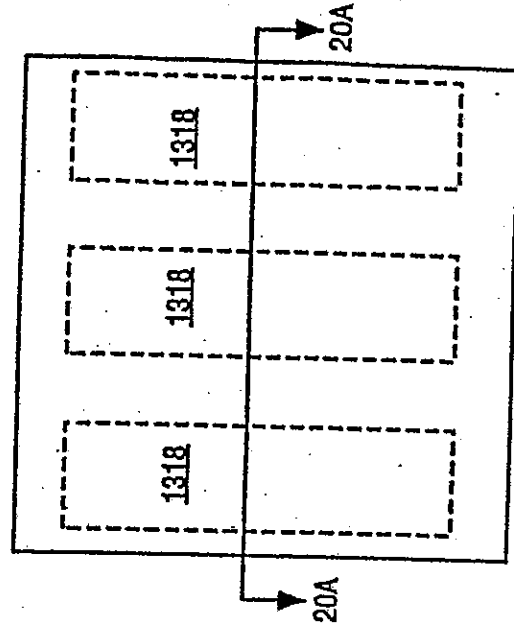


FIG. 20B

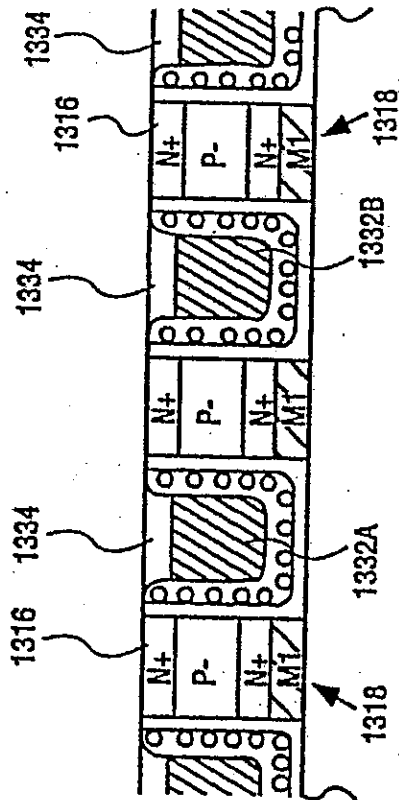


FIG. 19A

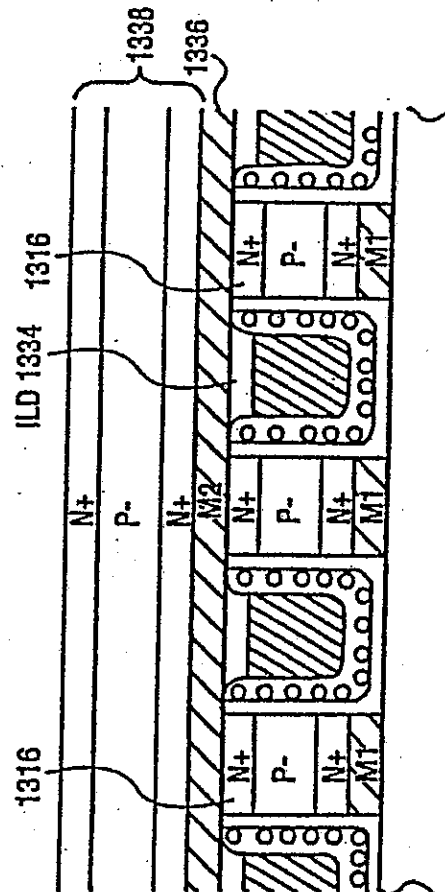


FIG. 20A

14/85 °

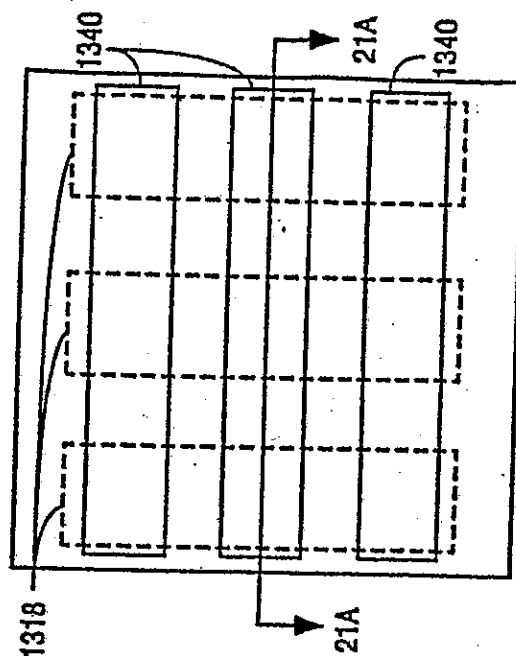


FIG. 21B

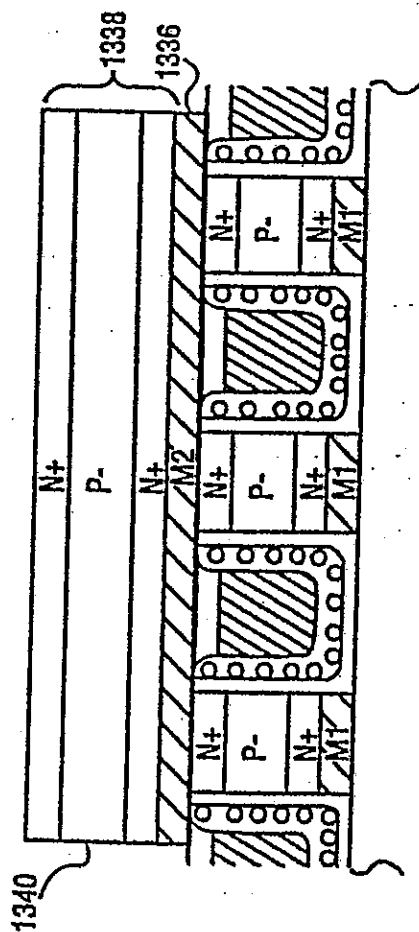


FIG. 21A

15/85 °

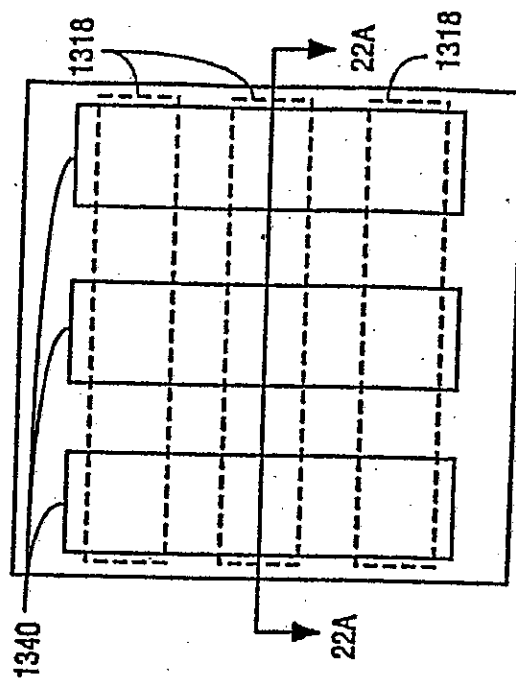


FIG. 22B

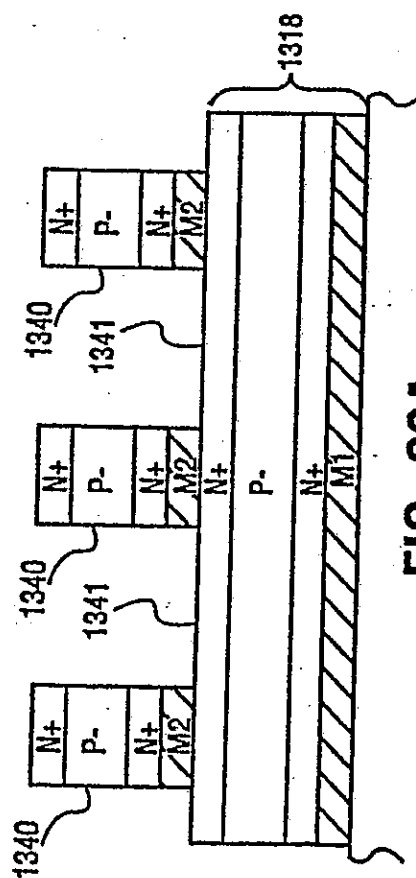


FIG. 22A

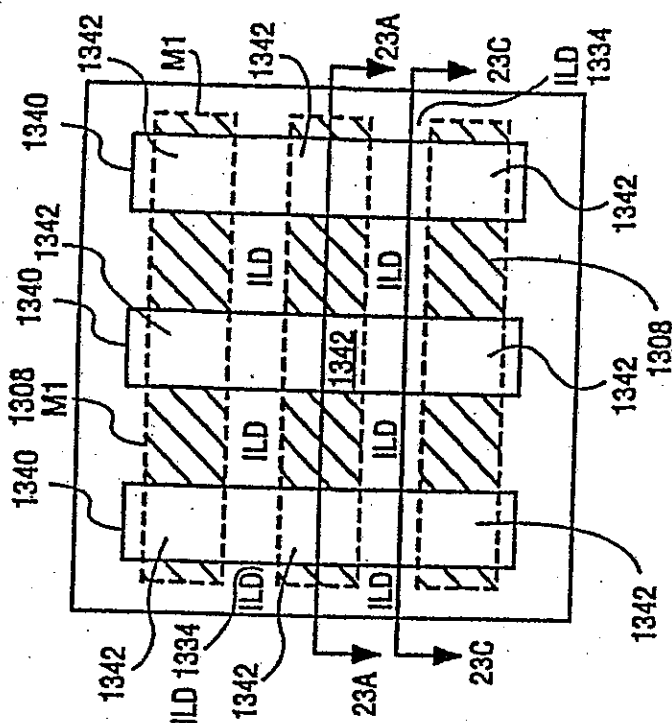


FIG. 23B

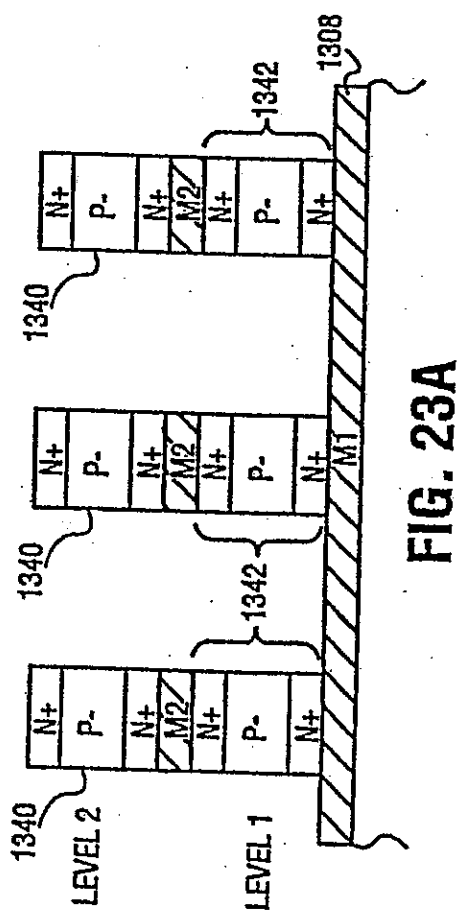


FIG. 23A

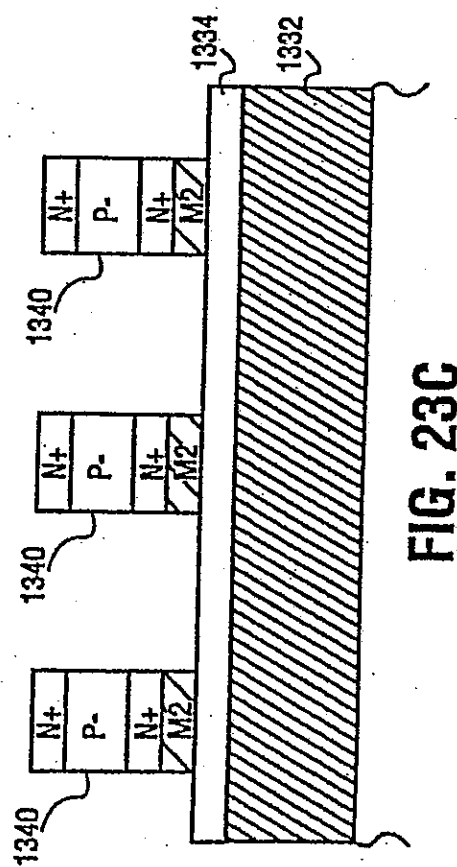


FIG. 23C

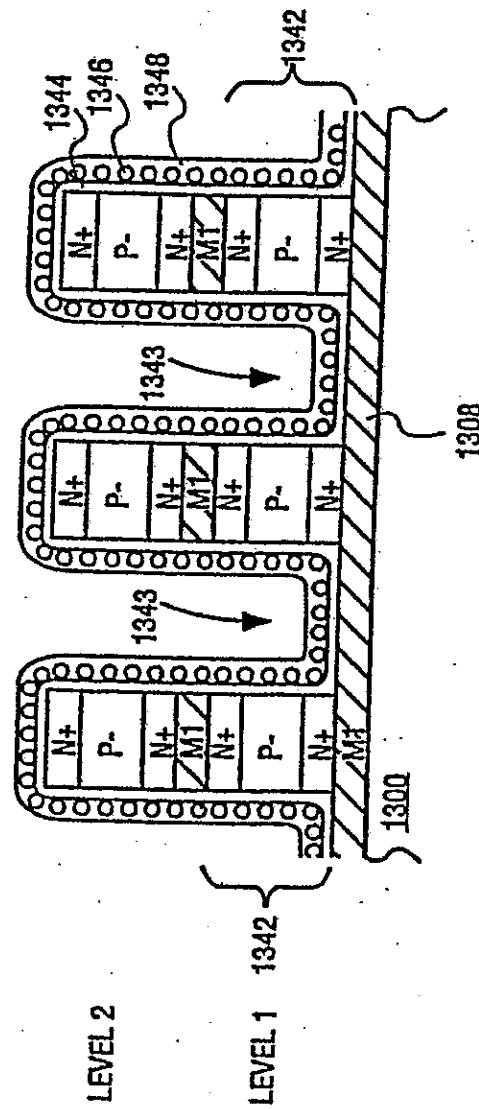


FIG. 24

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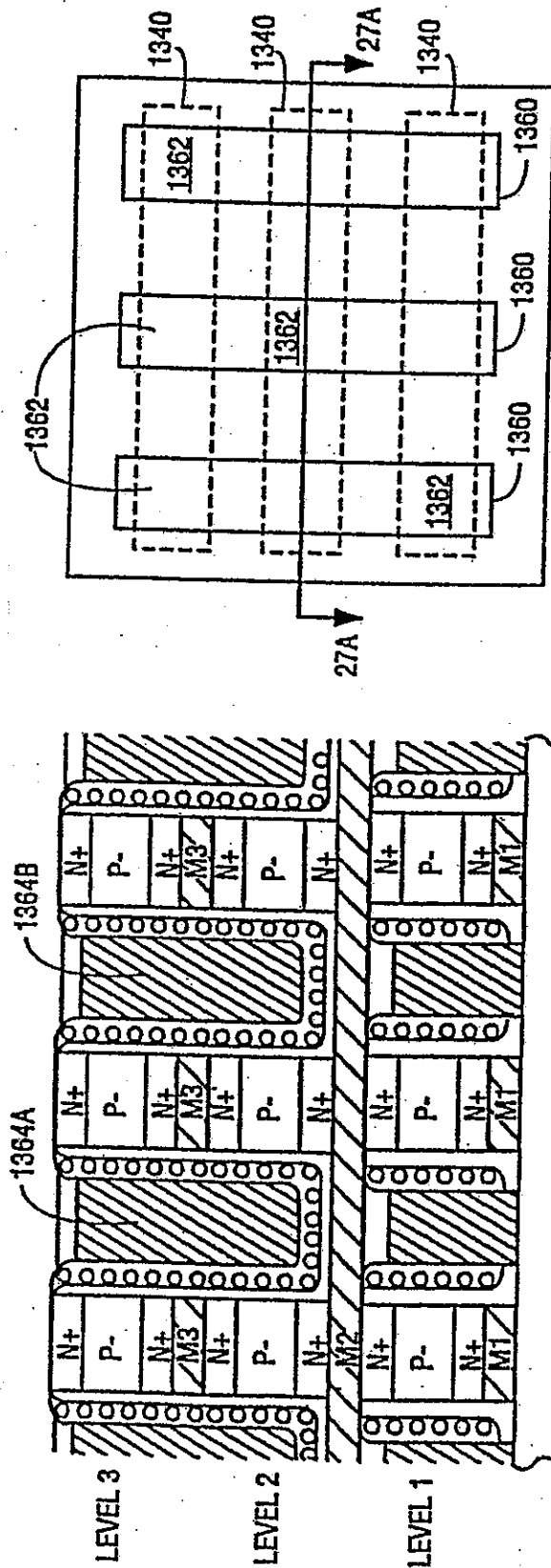


FIG. 27A

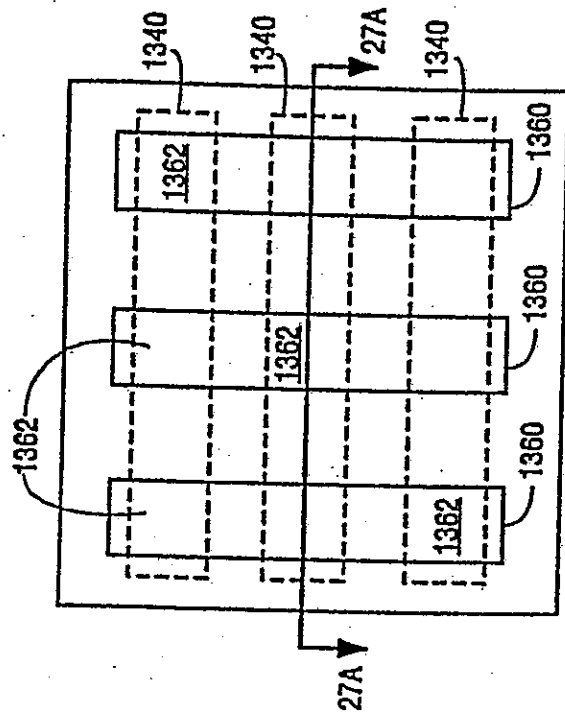


FIG. 27B

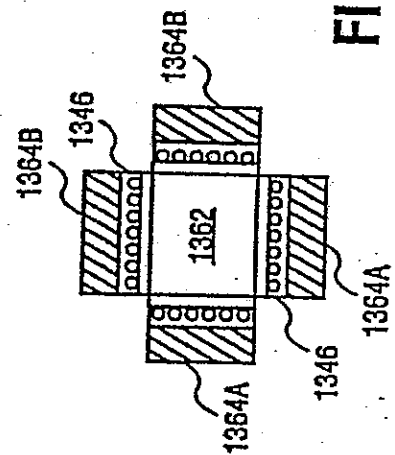


FIG. 28

20 / 85 °

FIG. 29A

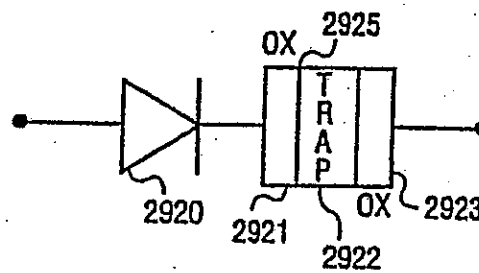
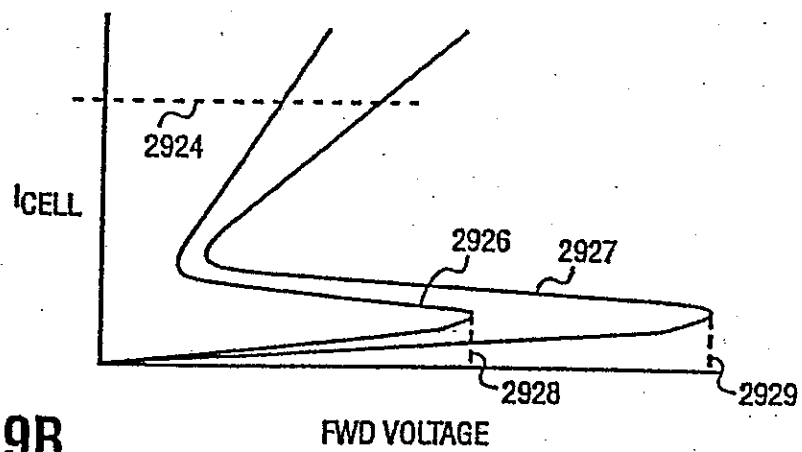


FIG. 29B



21/85°

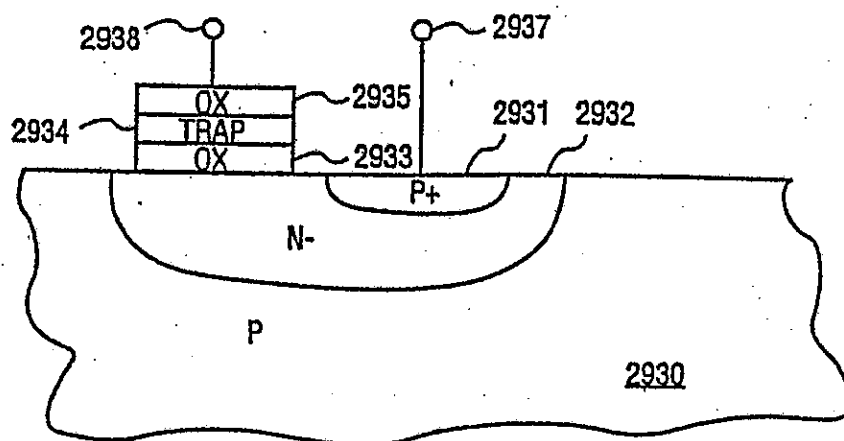


FIG. 30

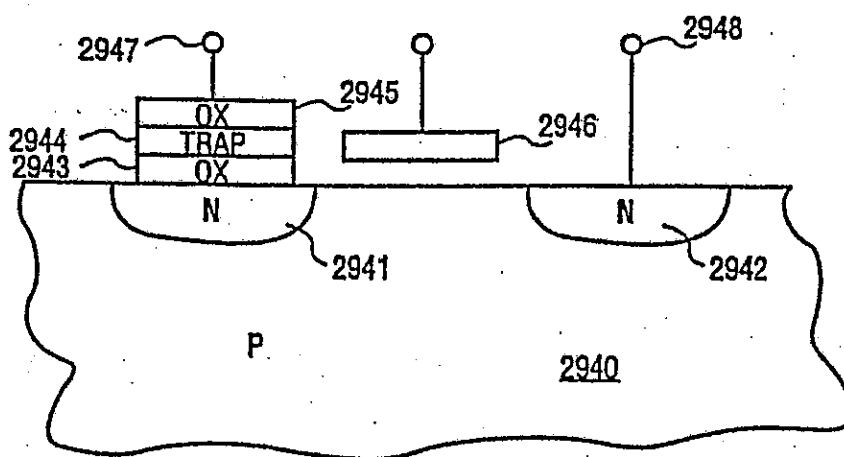
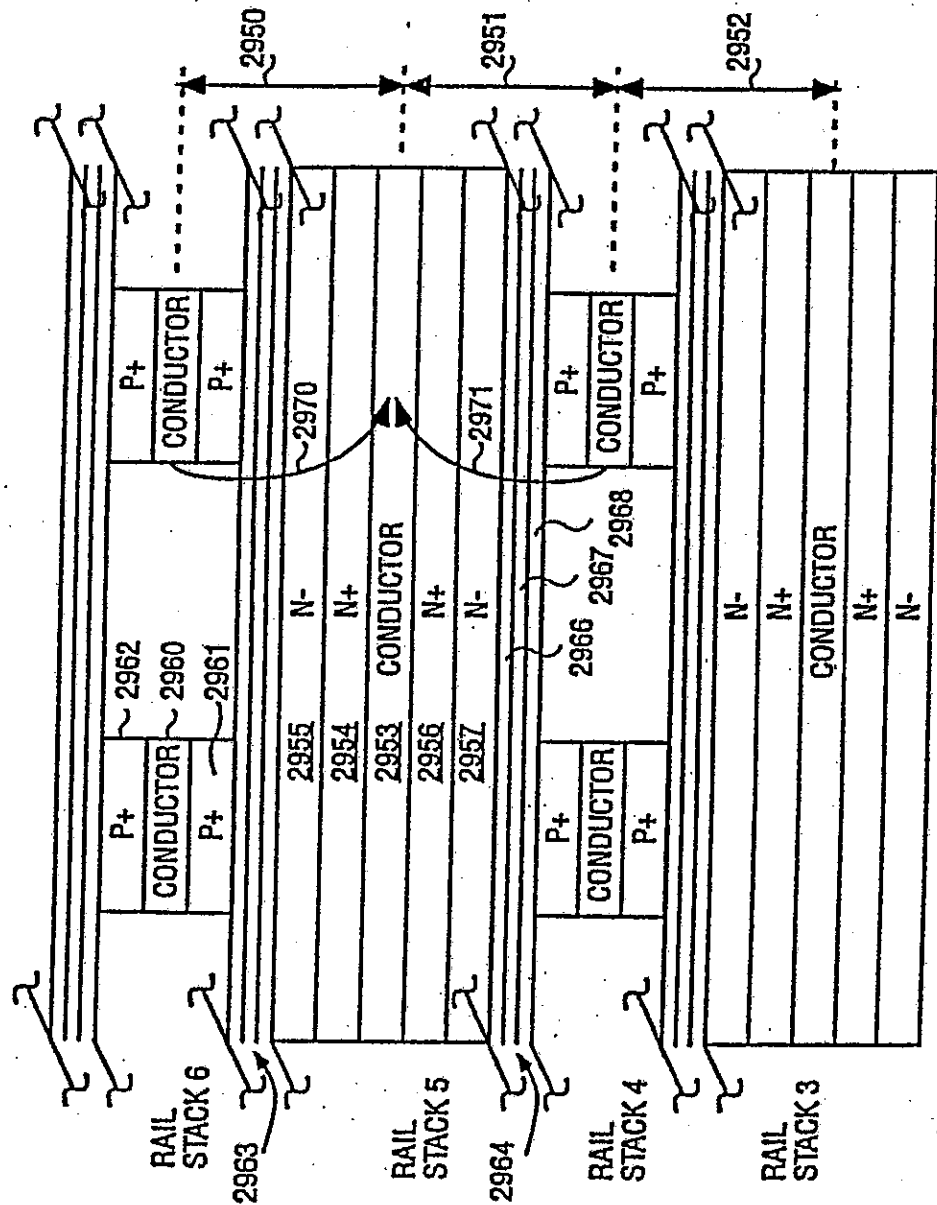


FIG. 31

22 / 85 °

FIG. 32



23/85

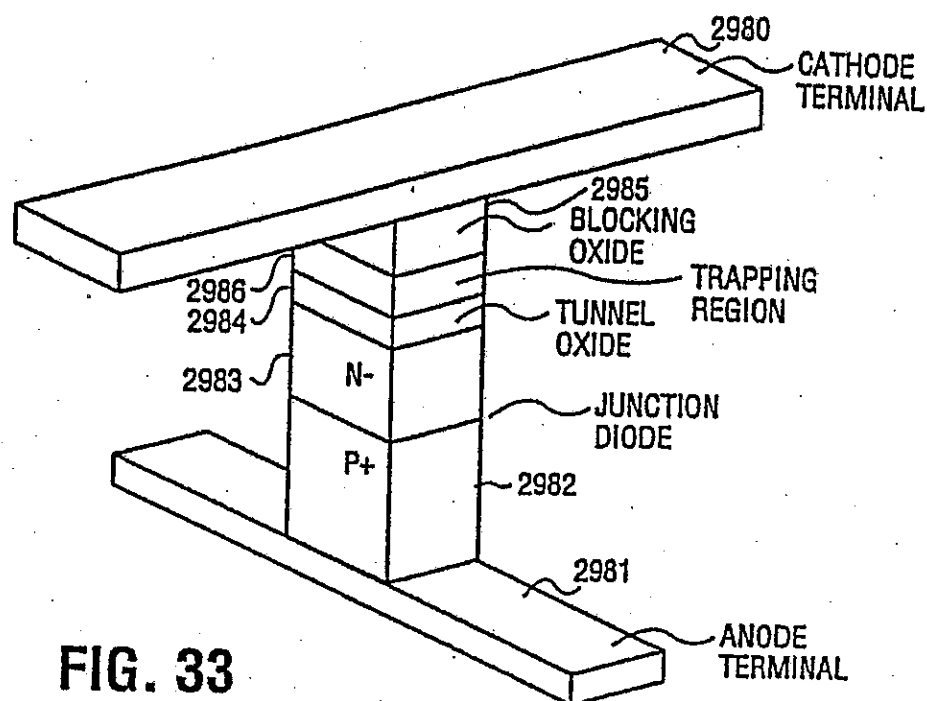


FIG. 33

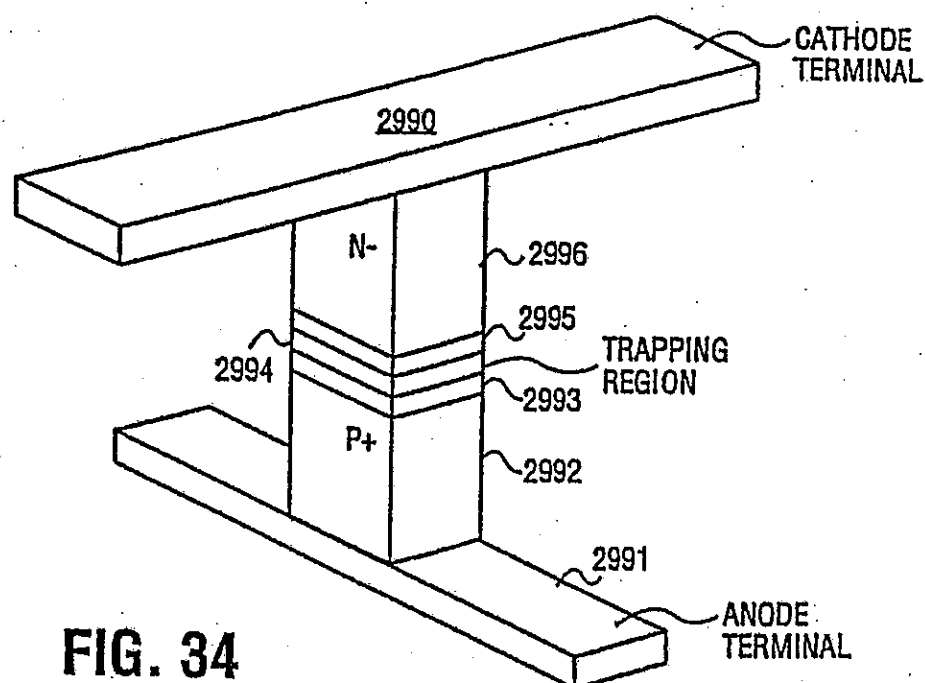


FIG. 34

24/85°

FIG. 35

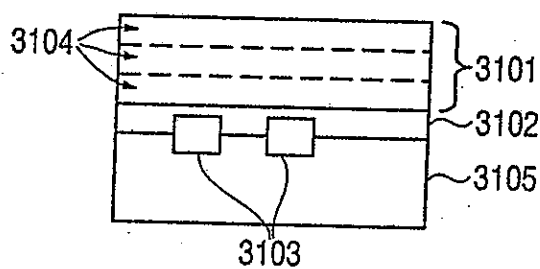
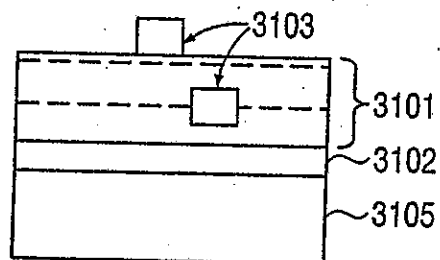


FIG. 36



25 / 85 °

FIG. 37

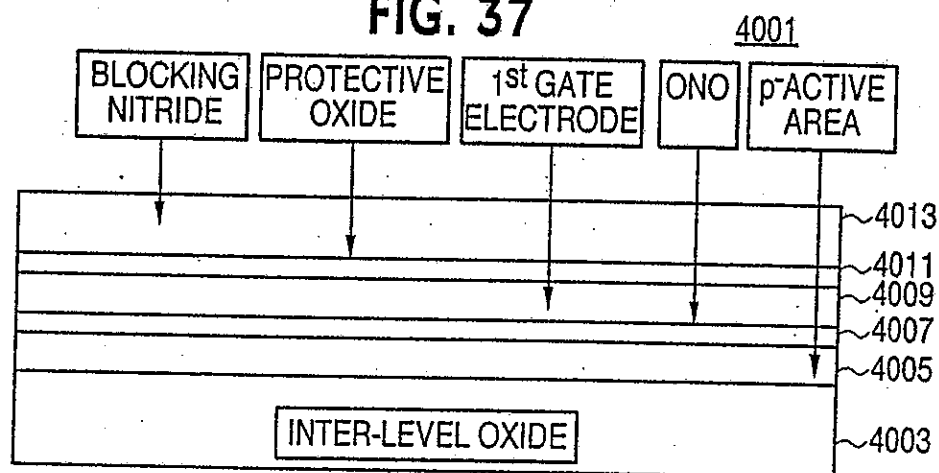
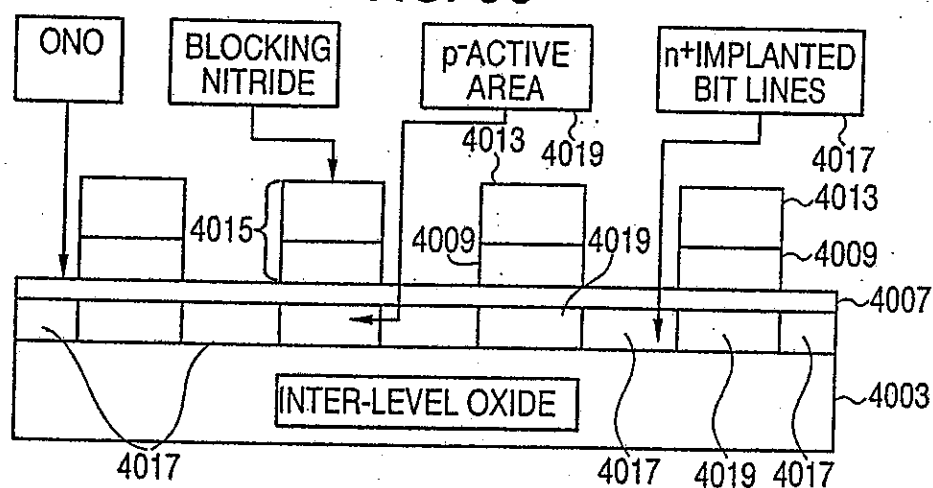


FIG. 38



This cross-sectional view illustrates a semiconductor device structure. A thick layer of **INTER-LEVEL OXIDE** (4003) forms the base. On top of this, a **1st GATE ELECTRODE** (4009) is formed, with **OXIDE SPACERS** (4021) positioned between them. **TiSi₂ IN BIT LINES** (4023) are formed on the surface. The structure includes various layers and regions labeled with reference numerals: 4007, 4023, 4017, 4009, 4021, 4023, 4003, 4019, and 4025. A bracket labeled 4025 groups the top layers on the right side.

[illegible]

A cross-sectional diagram of a semiconductor device. The base layer is labeled "INTER-LEVEL OXIDE" (4003). Above it are several layers and structures. A horizontal line represents a conductive layer (4009). Above this, there are vertical structures labeled "1st GATE ELECTRODE" (4009), "OXIDE SPACER" (4021), "OXIDE FILLING" (4027), and "TiSi₂ IN BIT LINES" (4023). Arrows point from labels 4021, 4027, and 4029 to specific regions. A bracket on the right side groups the top three layers as "4025".

FIG. 42

4043 2nd POLY. GATE

TiSi₂ IN WORDLINES

4035

n+ POLY IN WORD LINES 4037

4031

4037

4035

4033

4043

4007

4023

4017

4019

4009

4017

INTER-LEVEL OXIDE

4027

4025

4003

A

B

FIG. 43

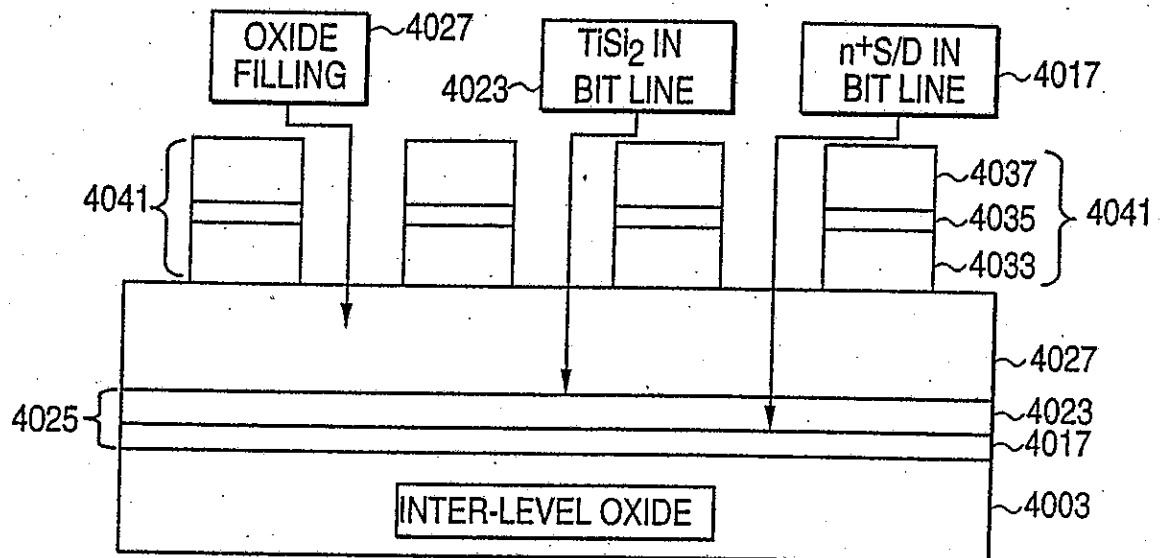
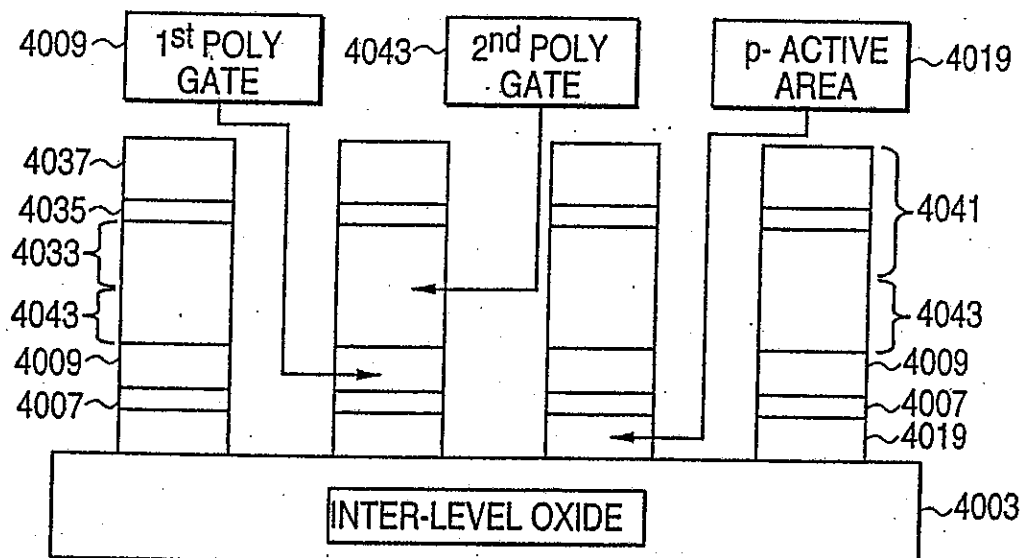


FIG. 44



29/85 °

FIG. 45

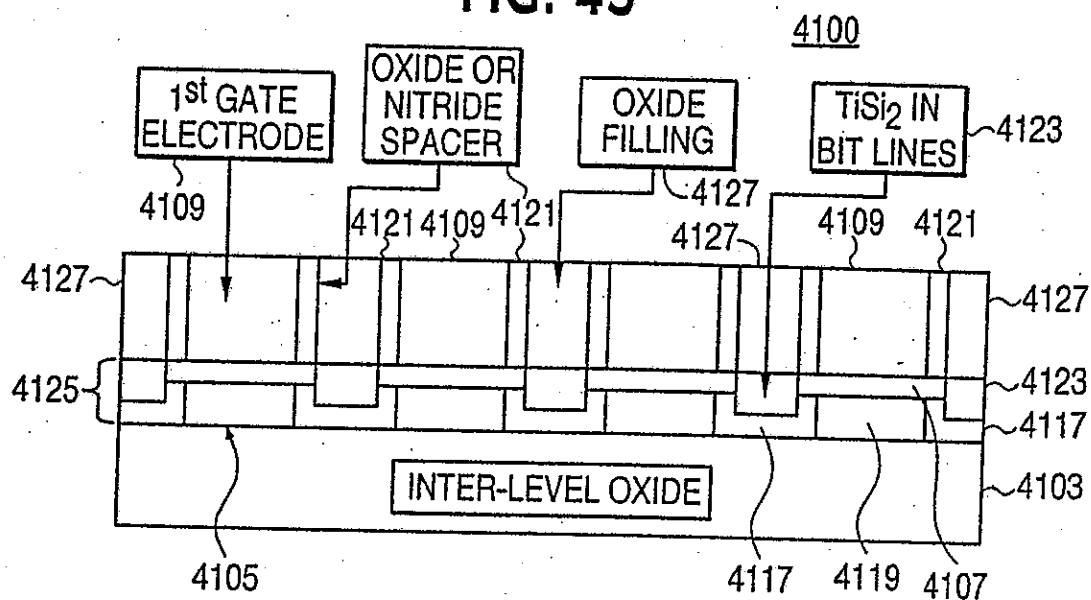
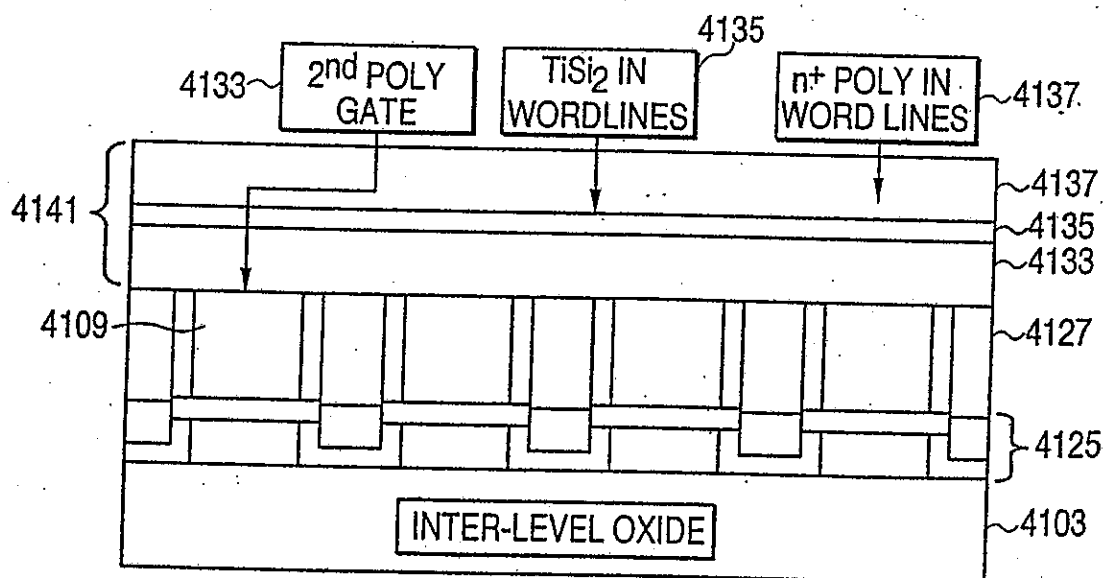
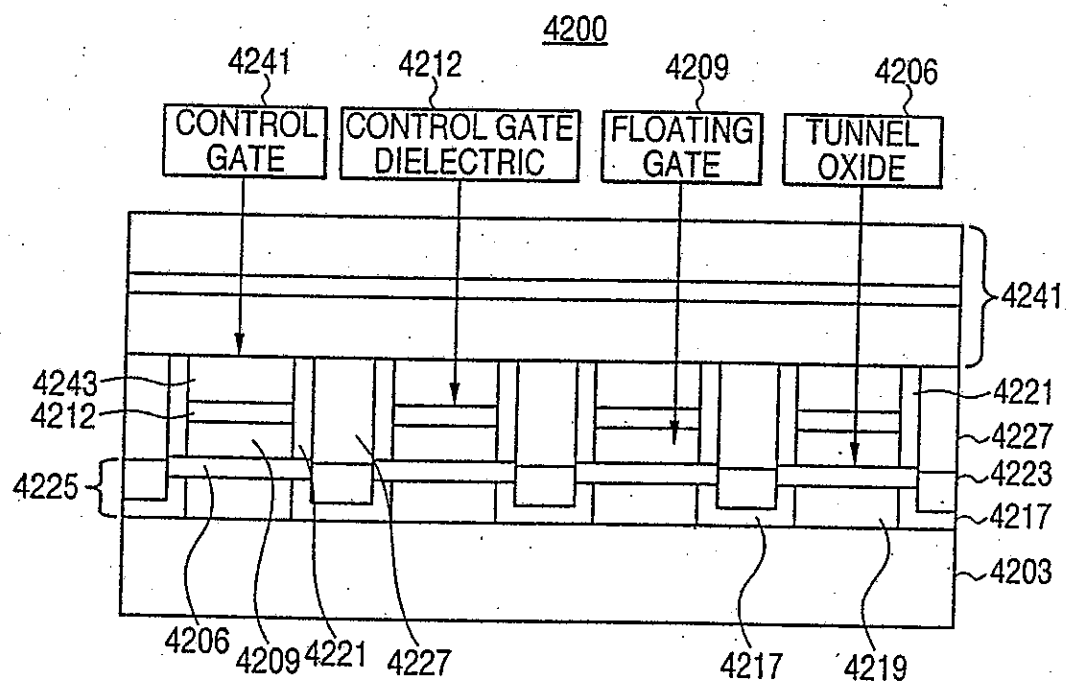


FIG. 46



30 / 85

FIG. 47



31/85 °

FIG. 48A

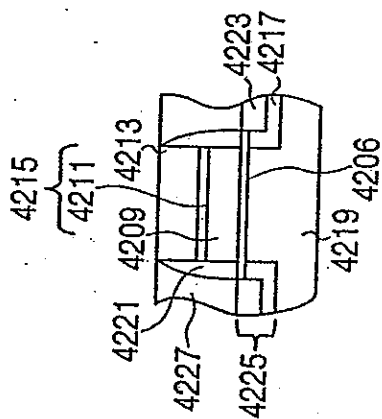


FIG. 48B

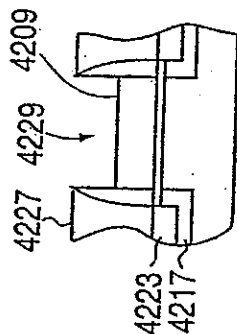


FIG. 48C

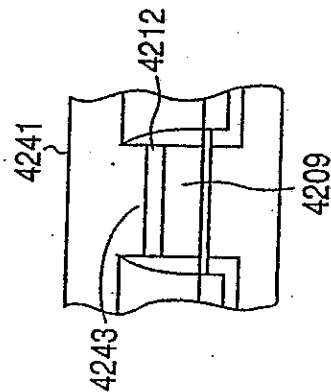


FIG. 49A

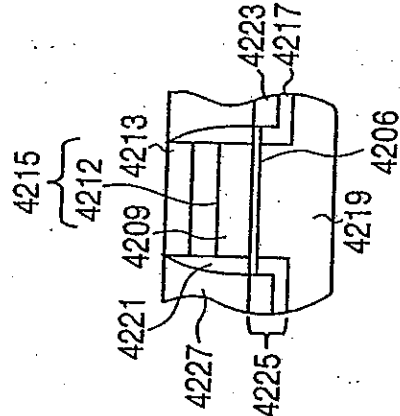


FIG. 49B

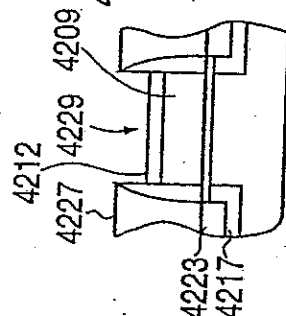
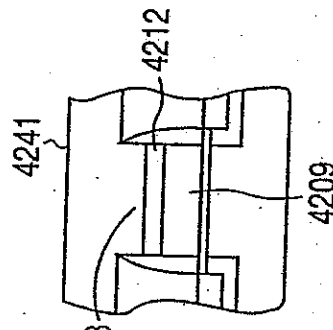
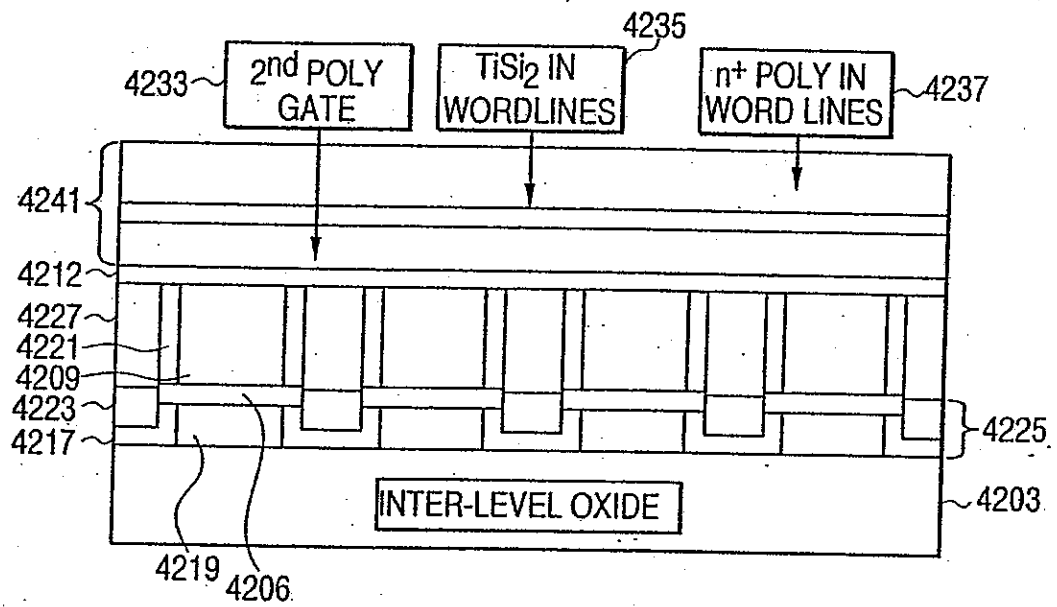


FIG. 49C



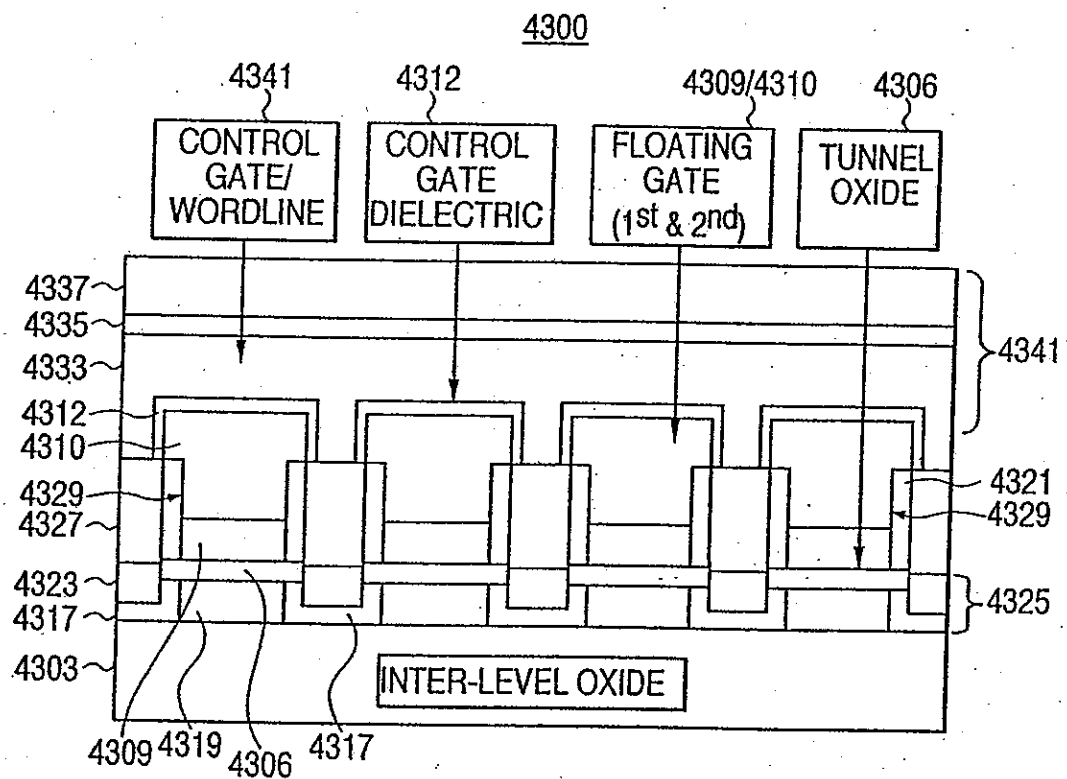
32 / 85 °

FIG. 50



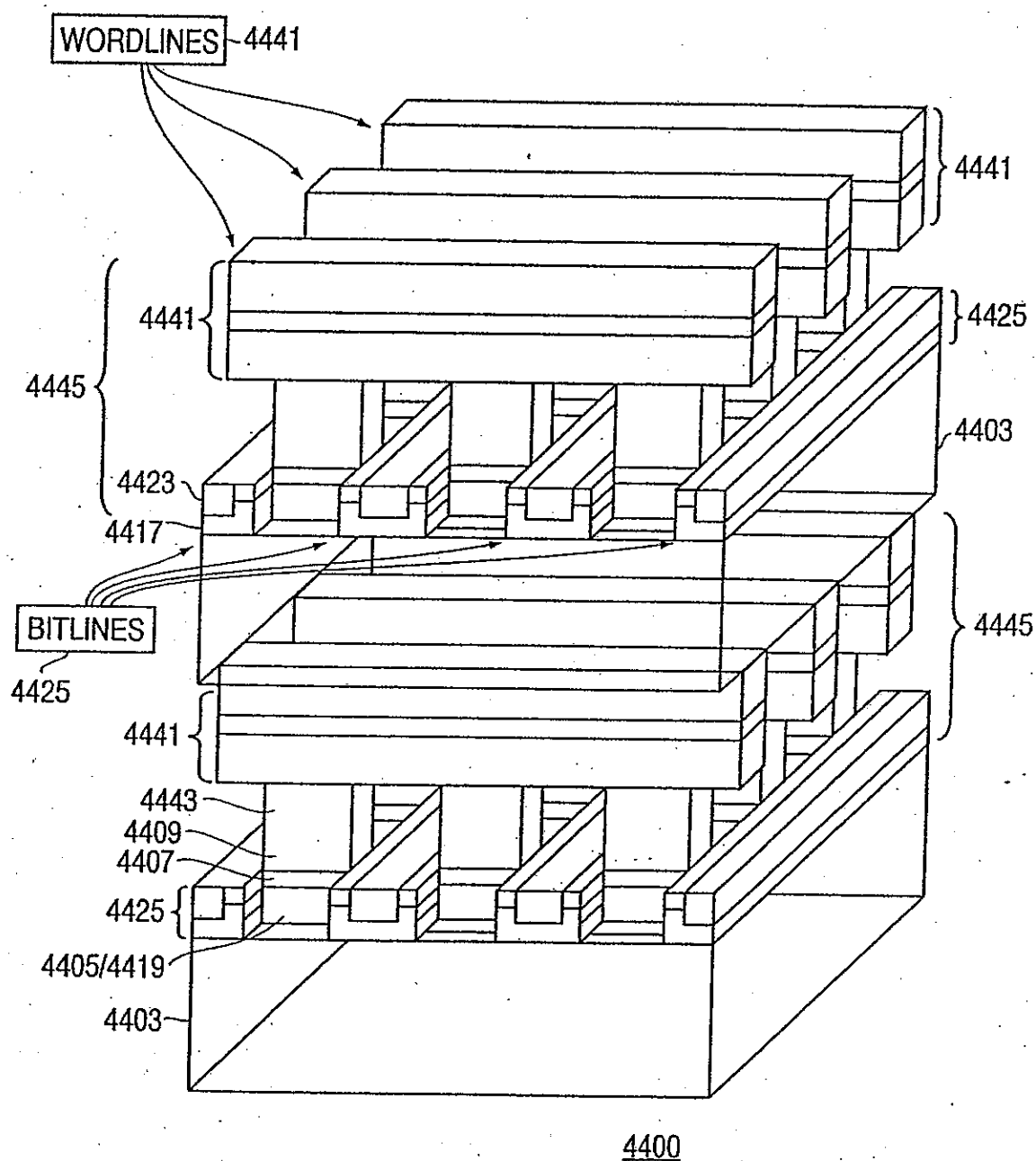
33 / 85 °

FIG. 51



34/85

FIG. 52



35 / 85 °

FIG. 53

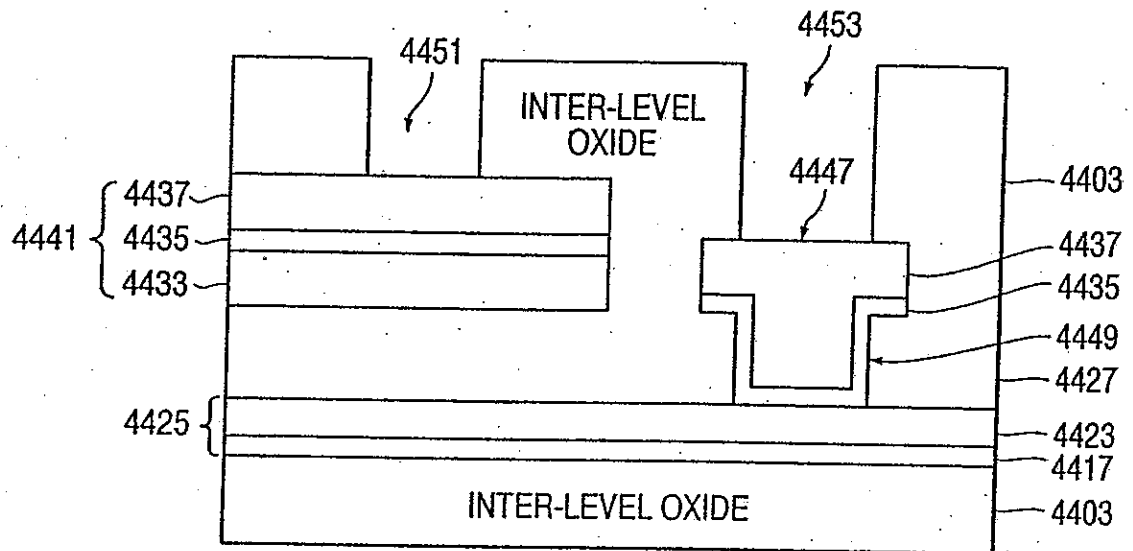
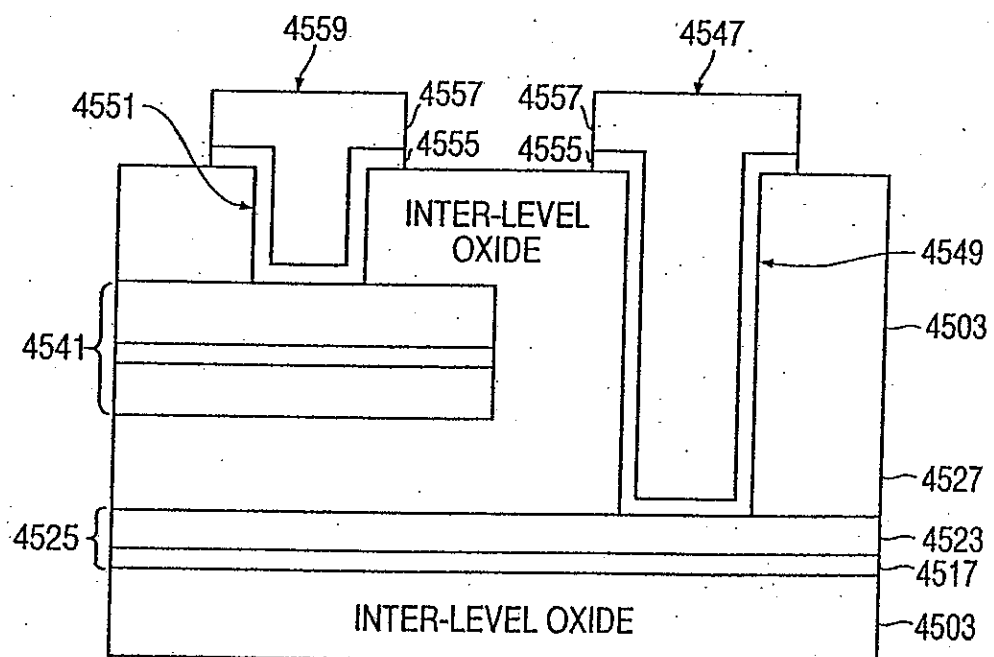


FIG. 54



36 / 85 °
FIG. 55

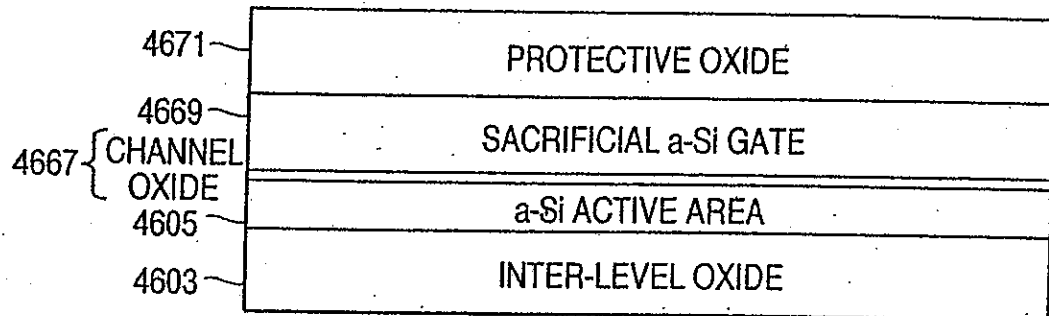


FIG. 56

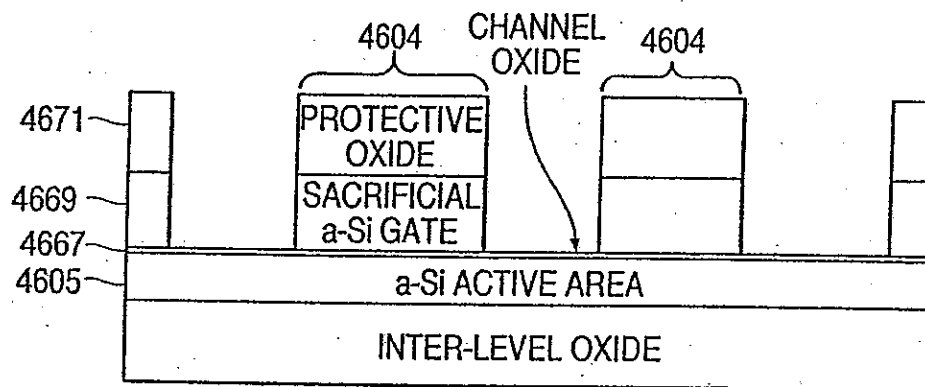
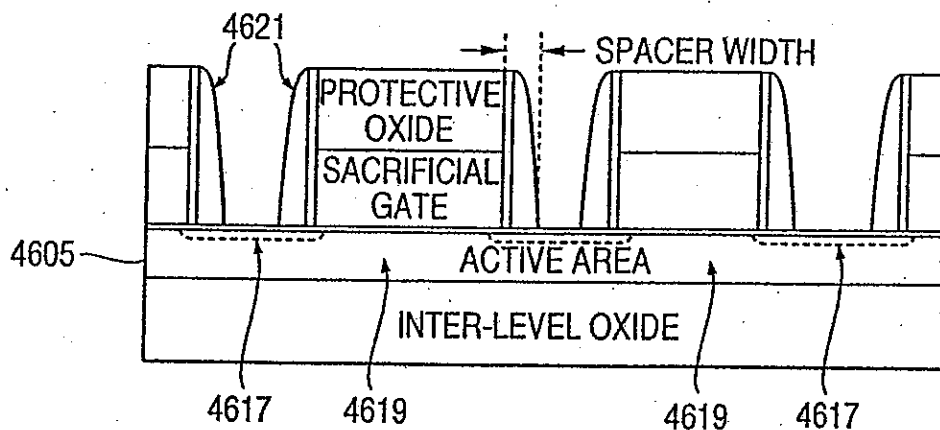


FIG. 57



37/85 °

FIG. 58

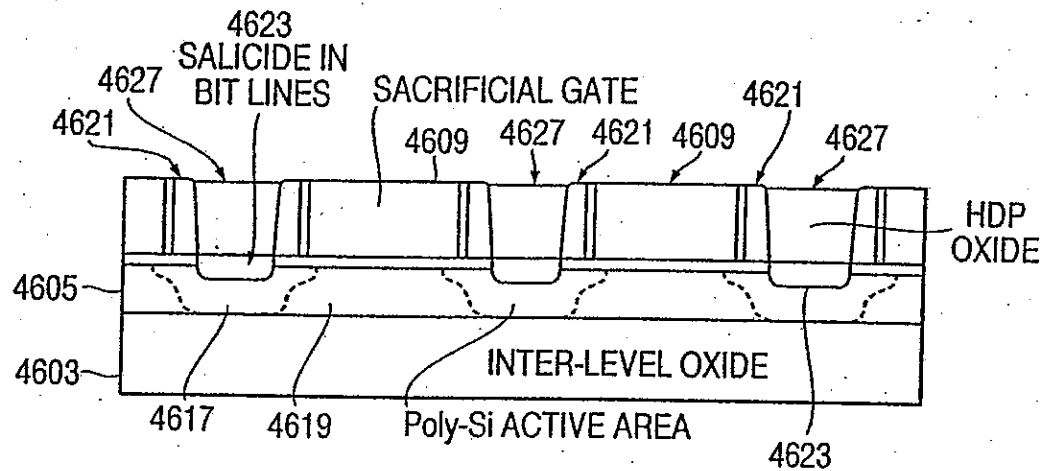
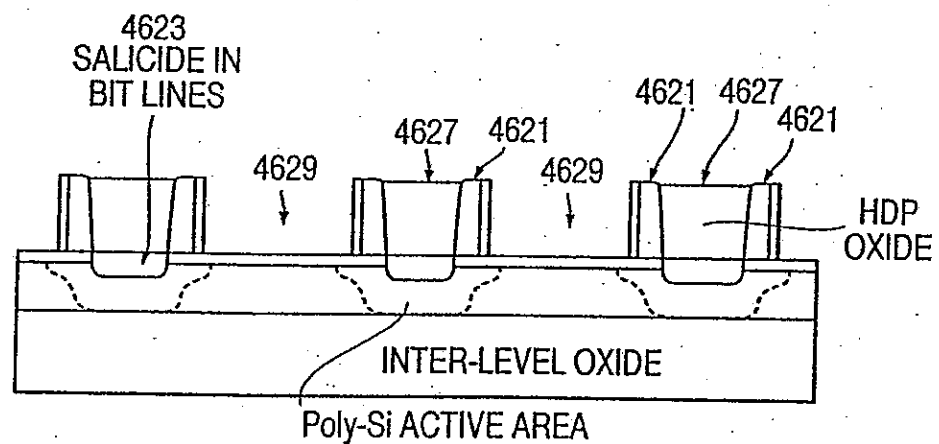


FIG. 59



38 / 85°

FIG. 60

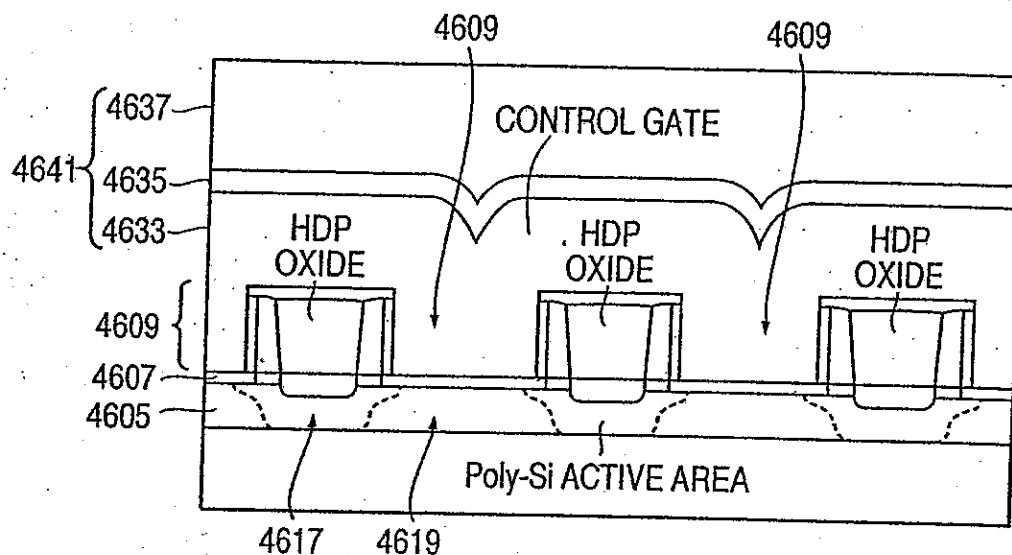
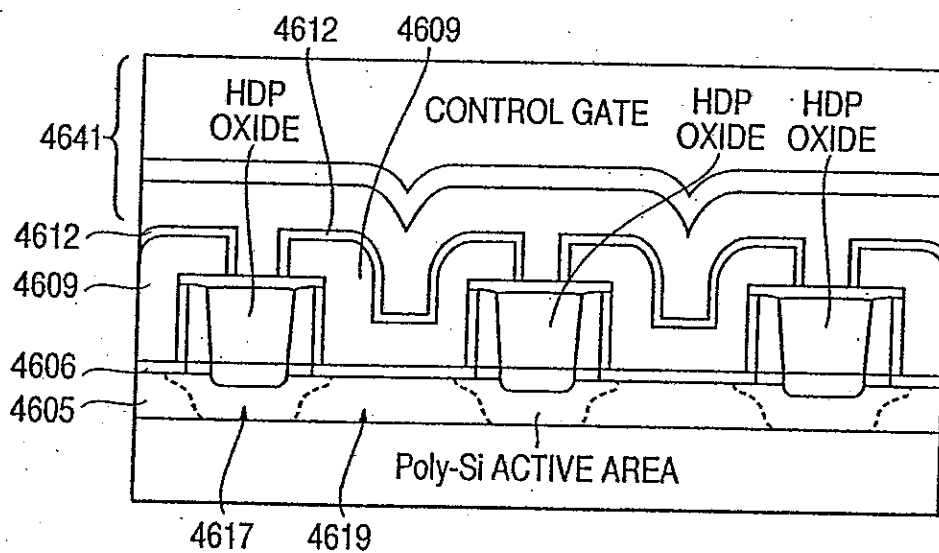
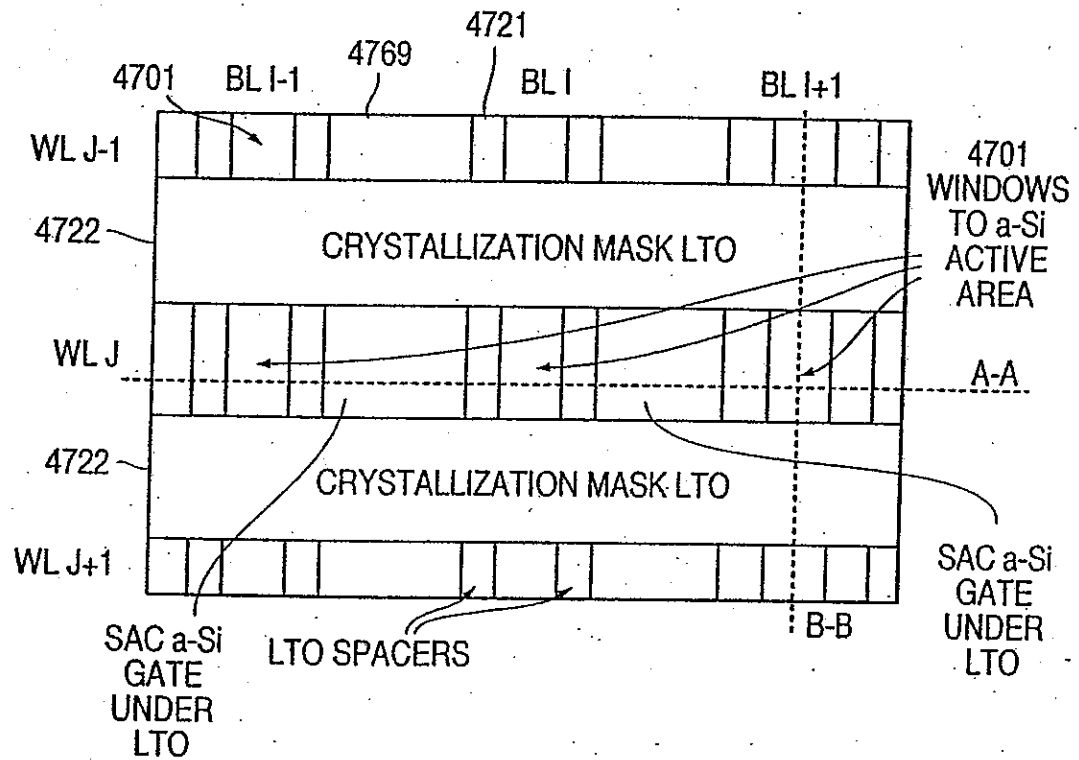


FIG. 61



39/85

FIG. 62



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FIG. 63

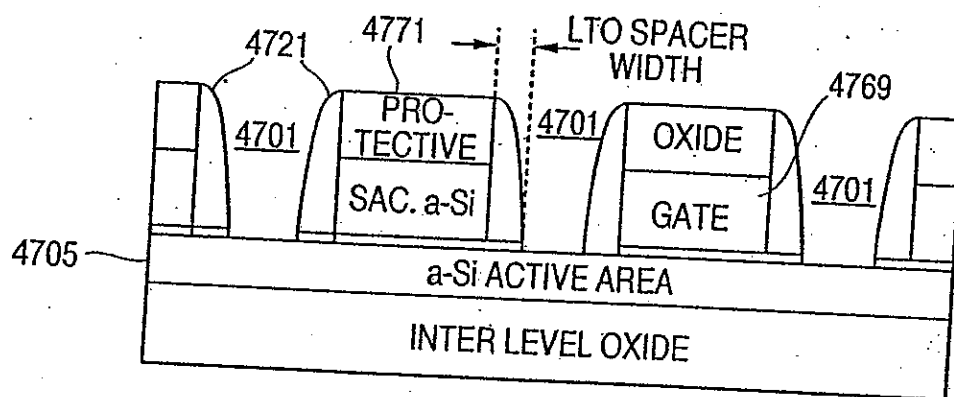
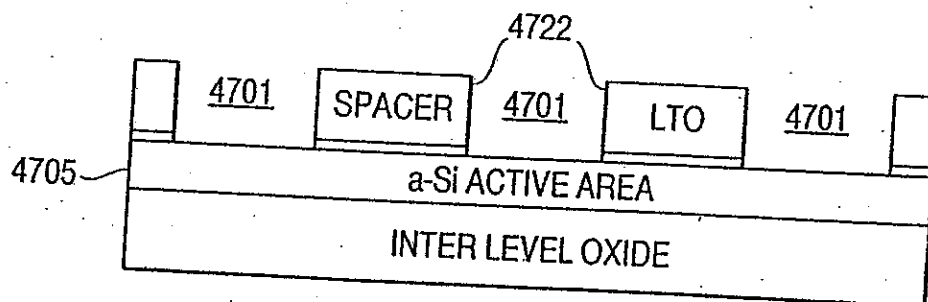
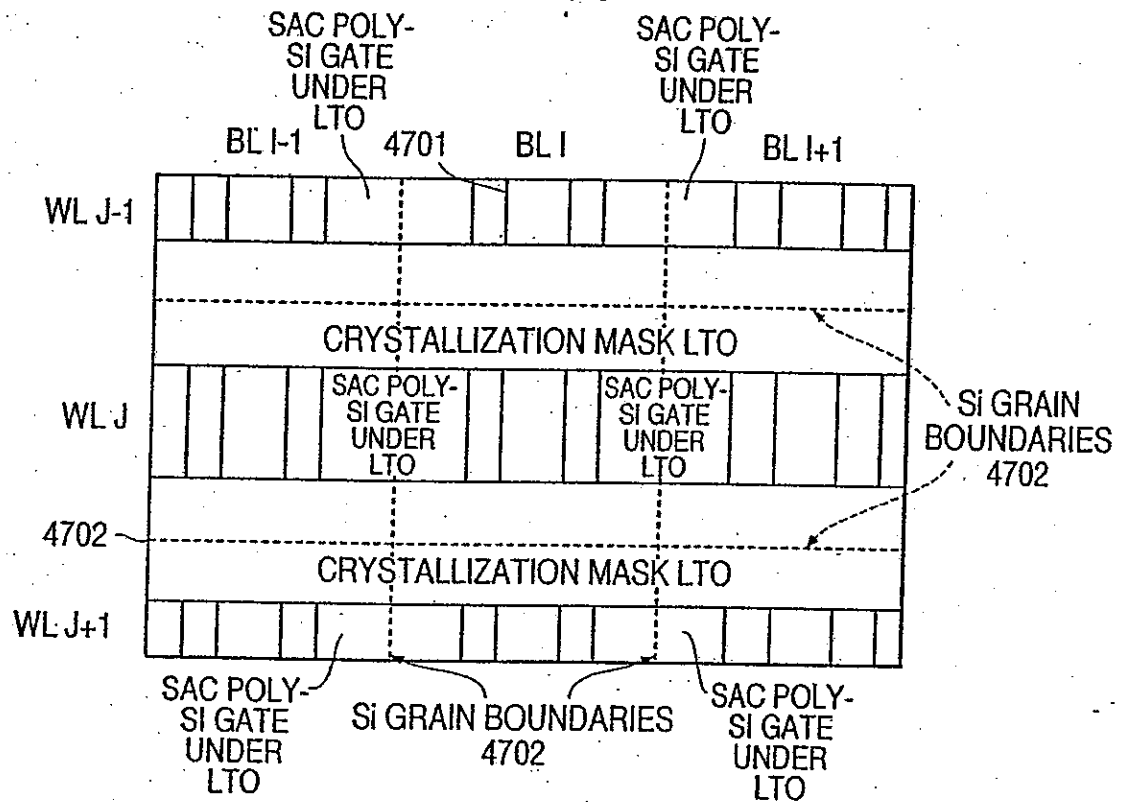


FIG. 64



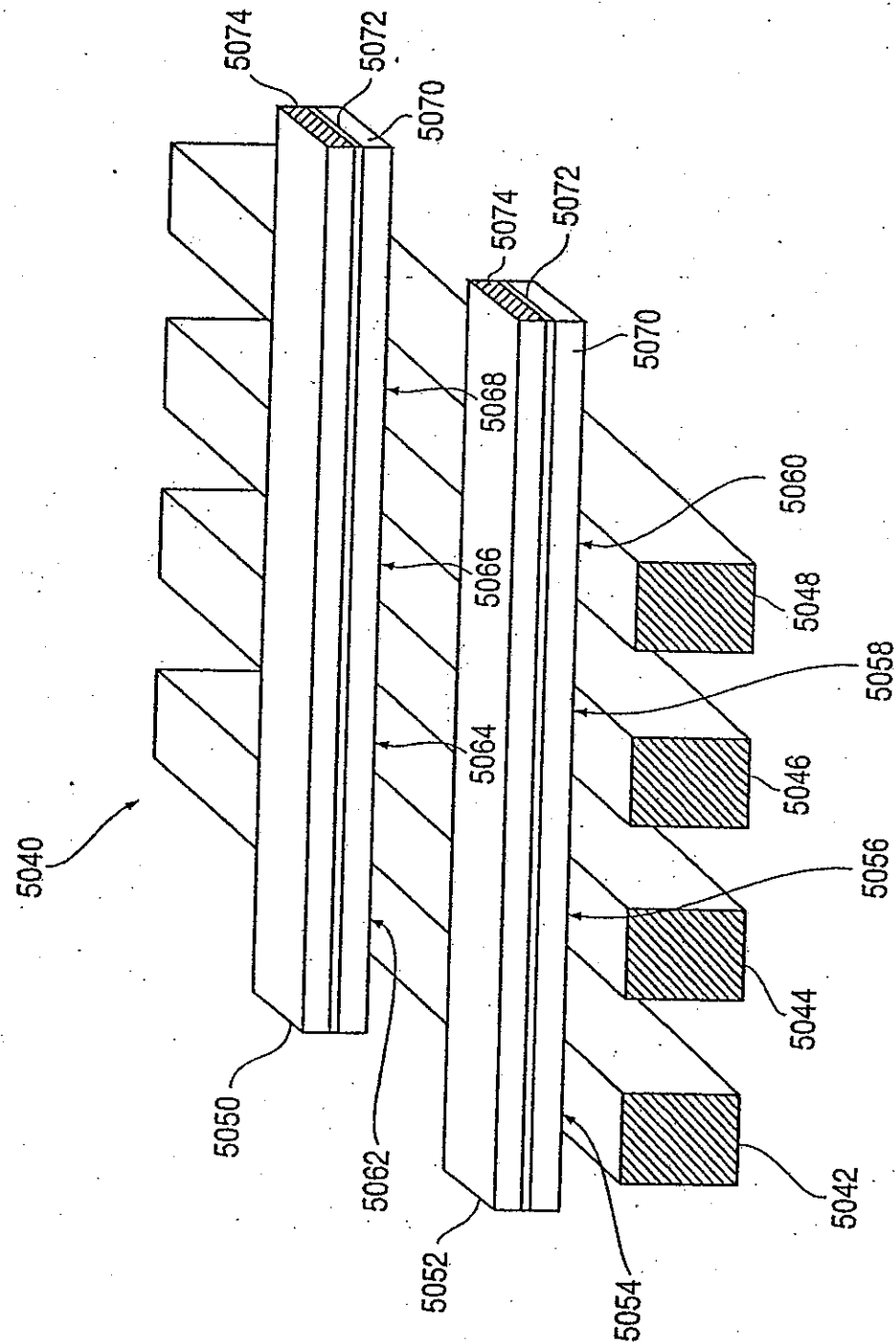
41 / 85°

FIG. 65



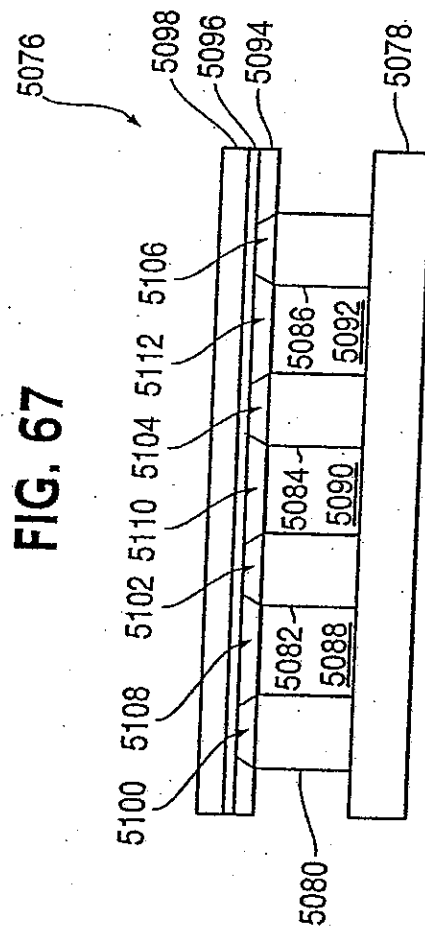
42 / 85°

FIG. 66



43/85°

FIG. 67



44 / 85_o

FIG. 68

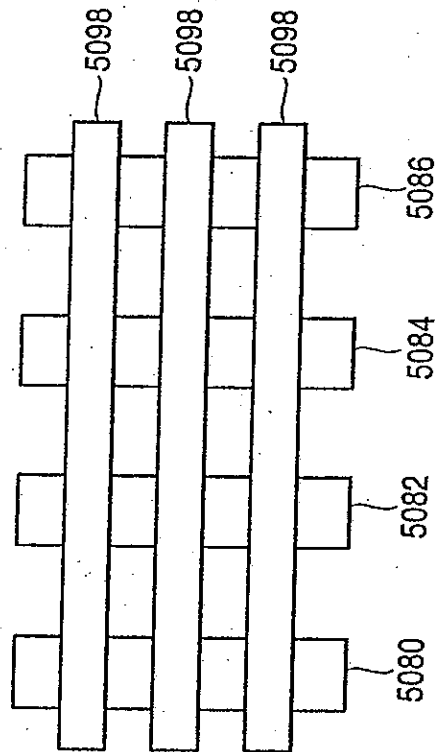


FIG. 69

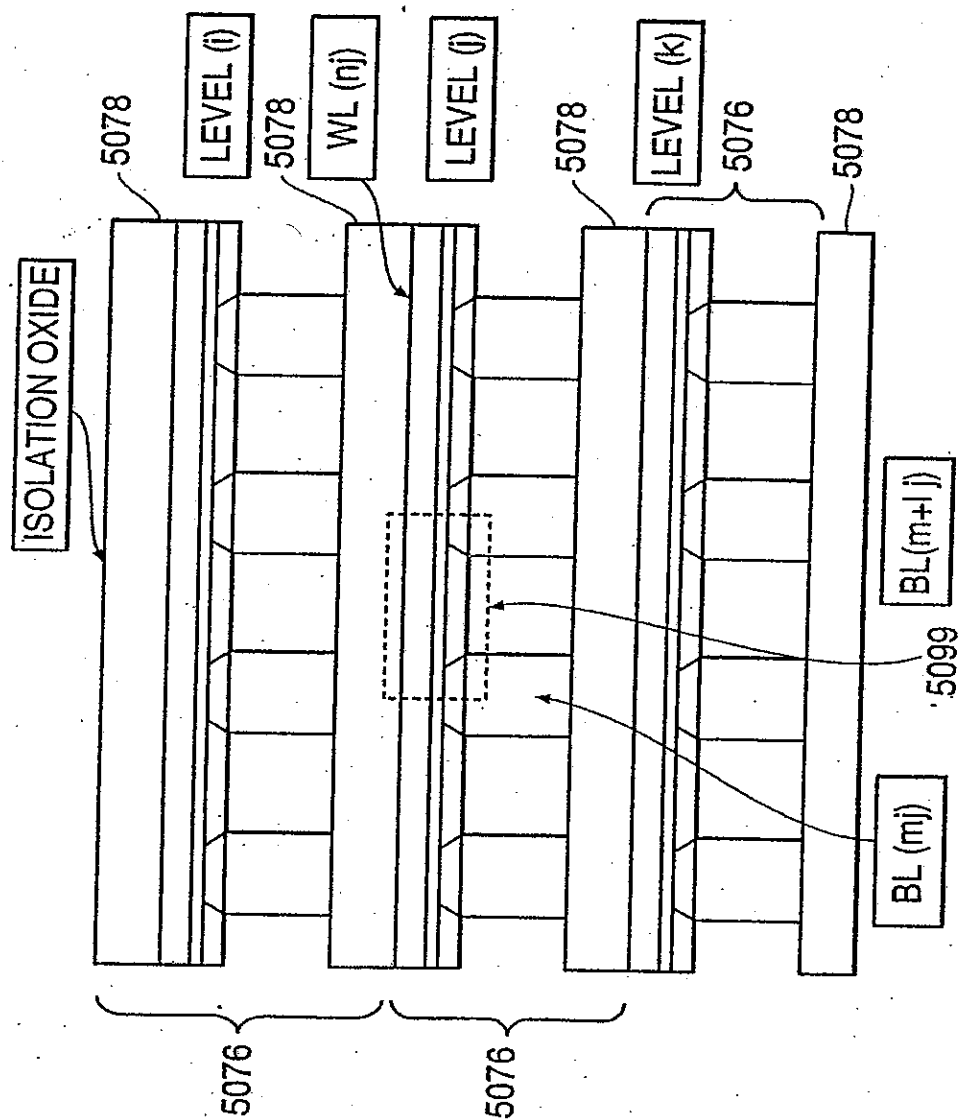
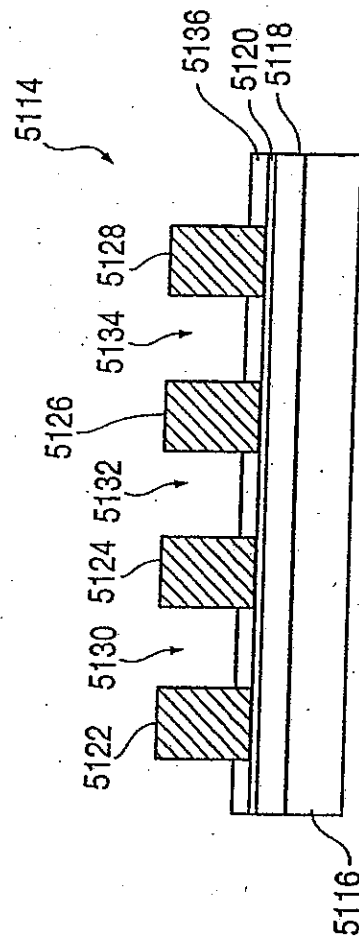


FIG. 70



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FIG. 71

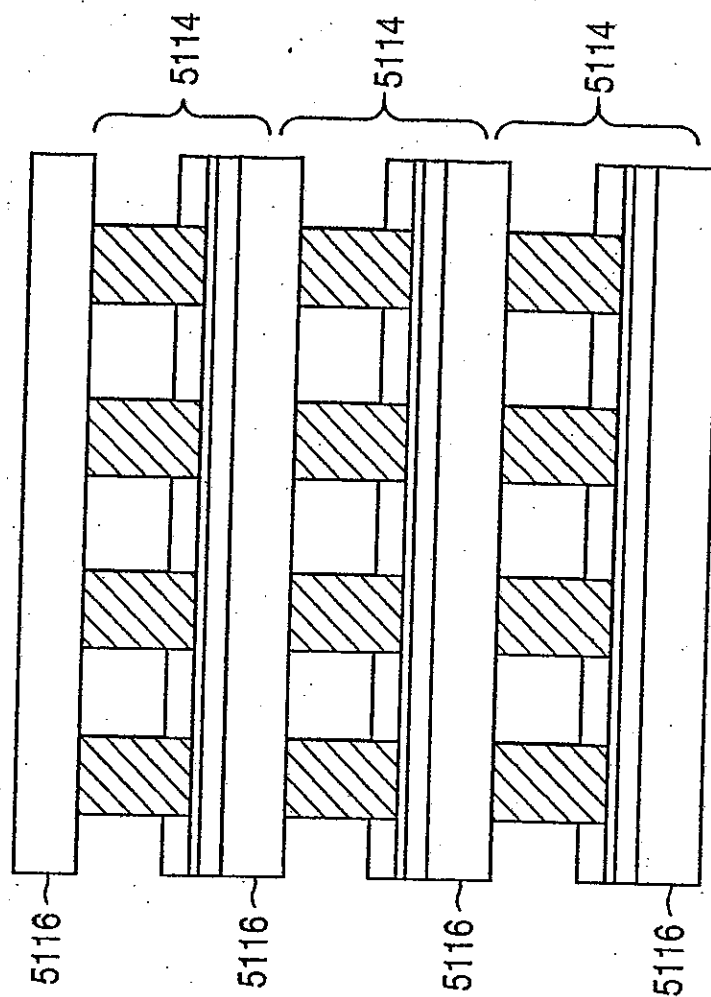
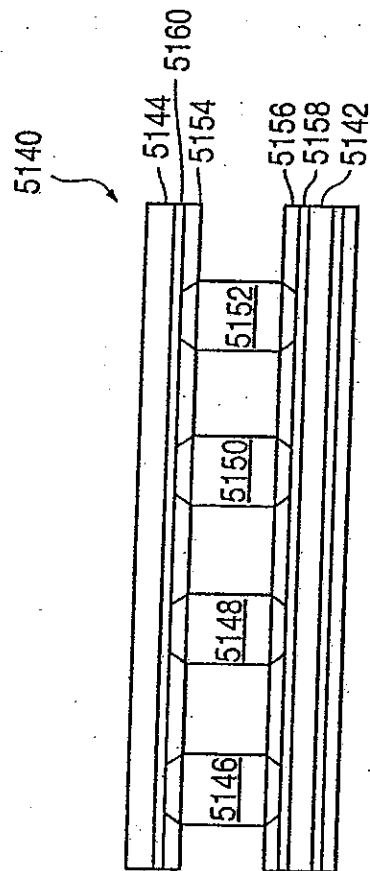


FIG. 72



49/85 °

FIG. 73

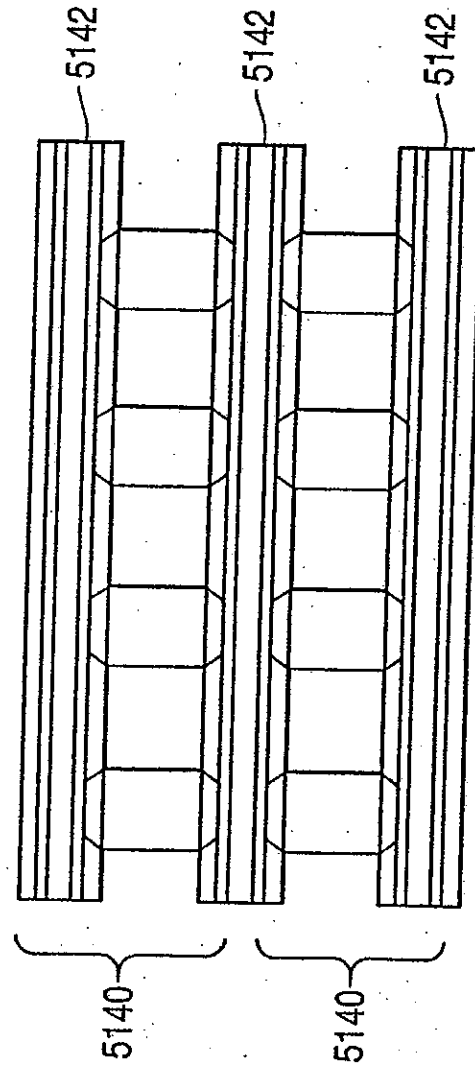
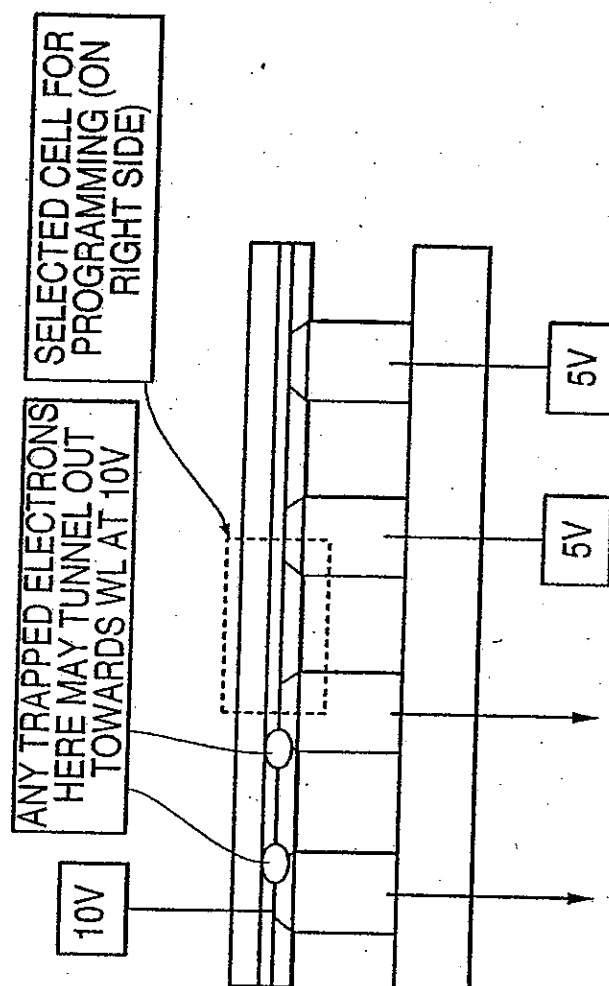
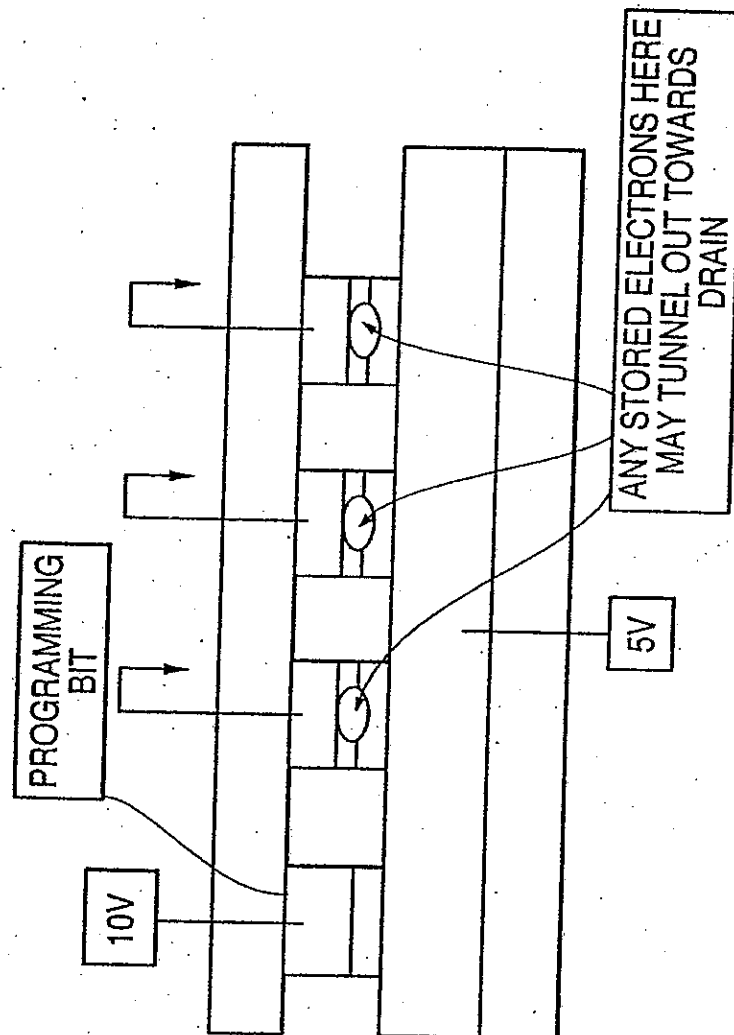


FIG. 74



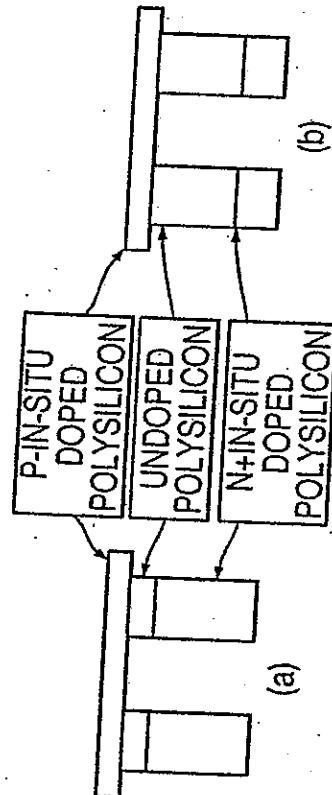
51/85 °

FIG. 75



52 / 85°

FIG. 76



53 / 85

FIG. 77

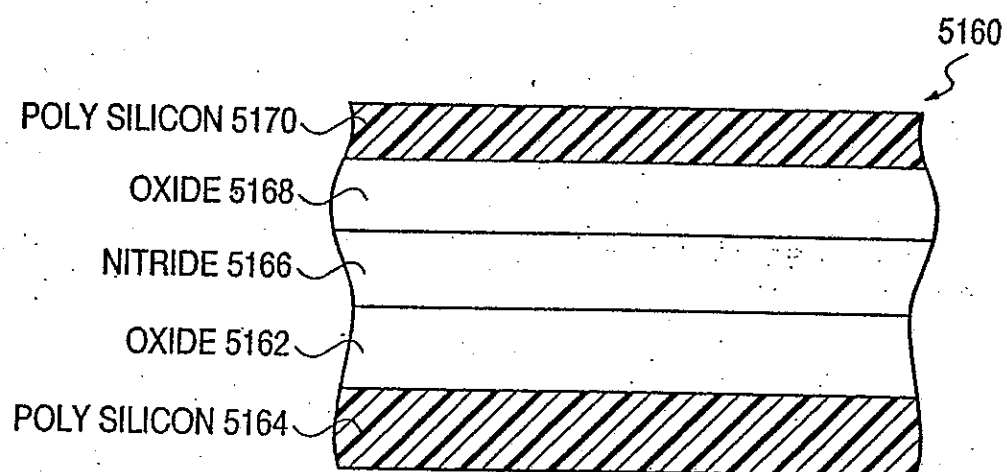
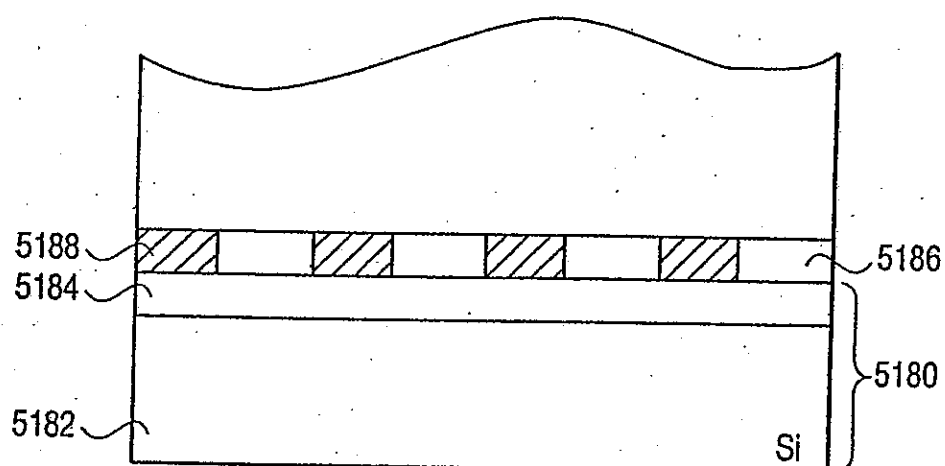


FIG. 80



54 / 85 °

FIG. 78

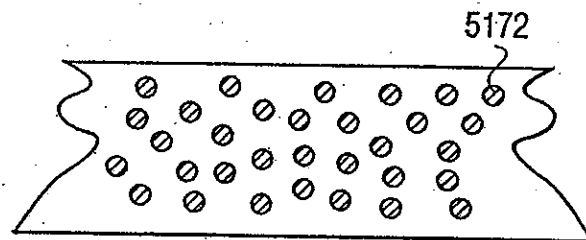
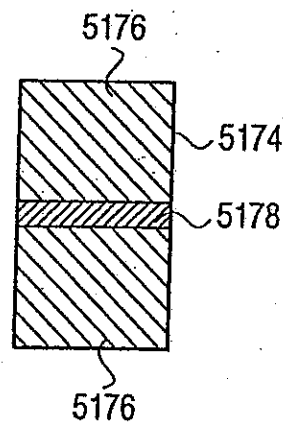


FIG. 79



55/85 °

FIG. 81A

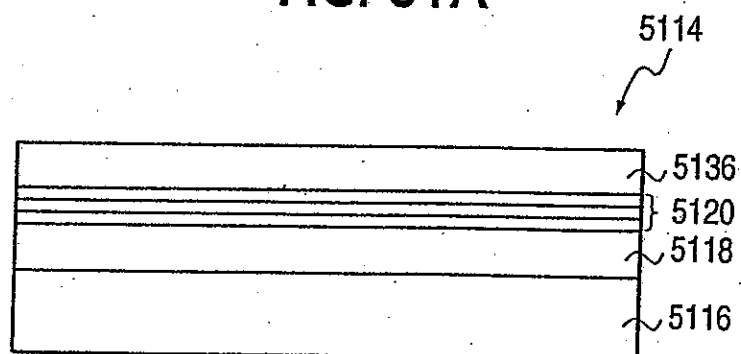


FIG. 81B

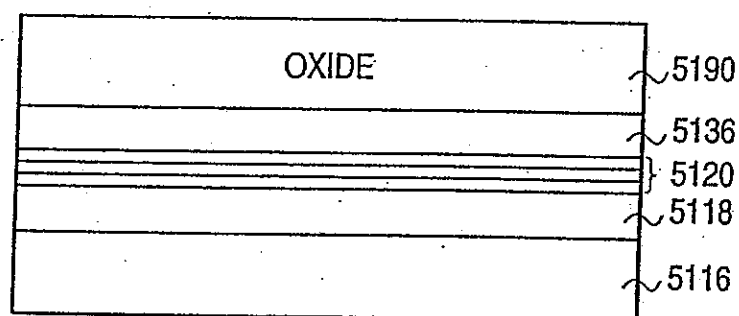
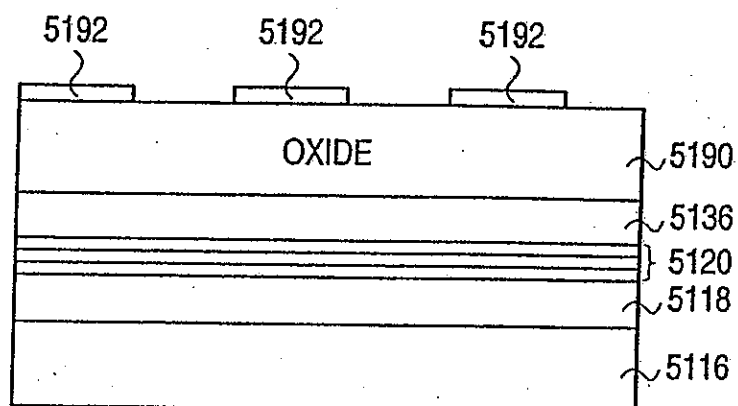


FIG. 81C



56/85 °

FIG. 81D

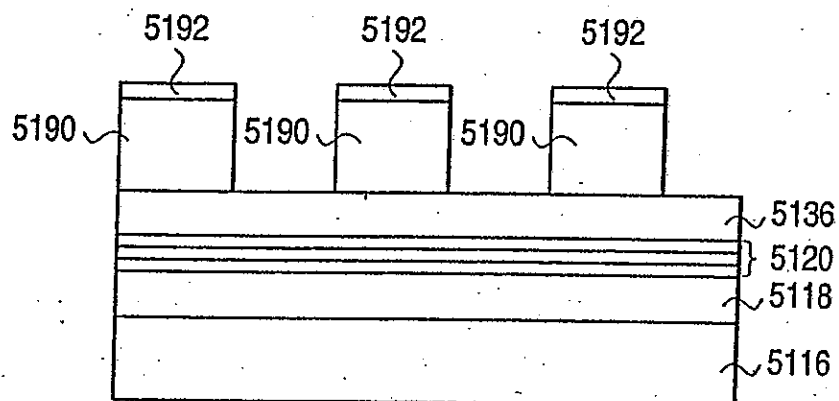


FIG. 81E

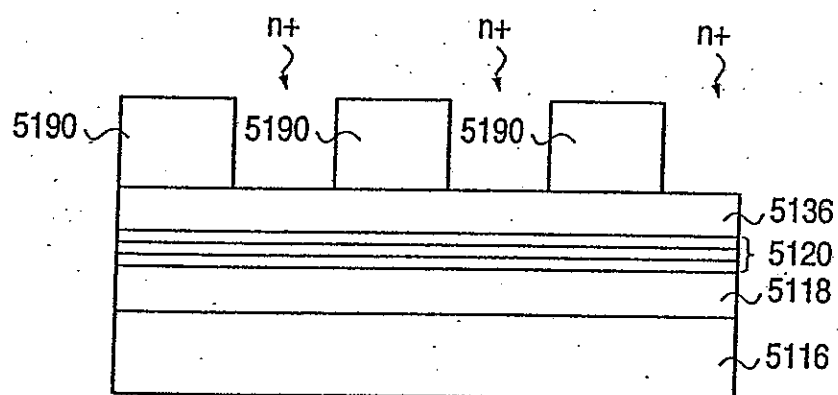
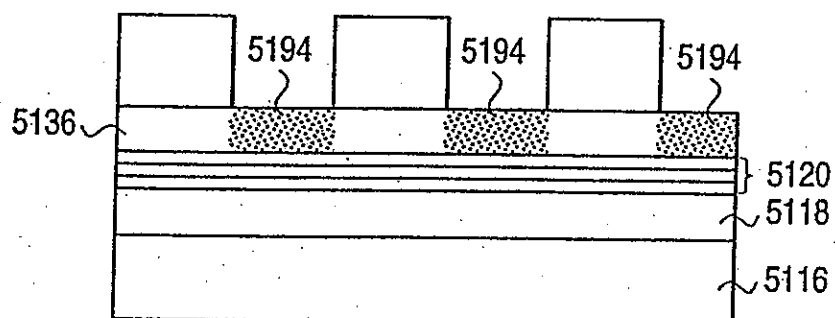


FIG. 81F



57/85 °

FIG. 81G

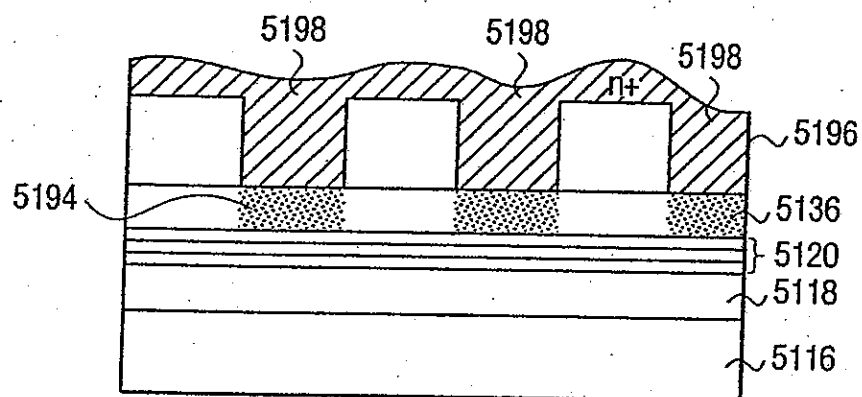
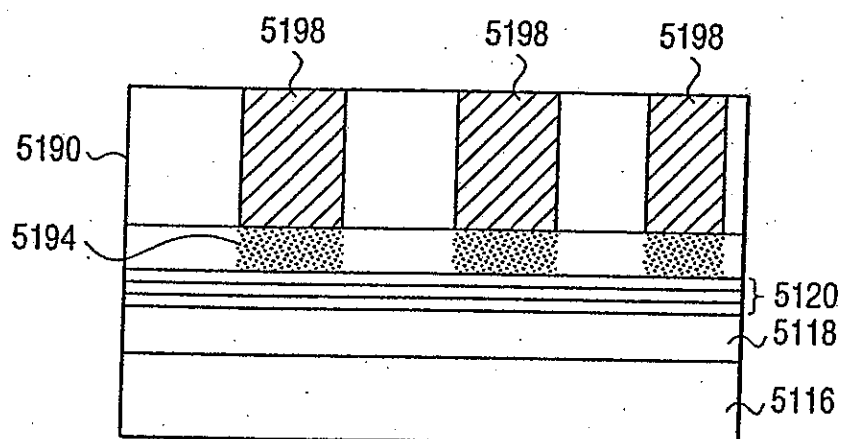


FIG. 81H



58/85 °

FIG. 82A

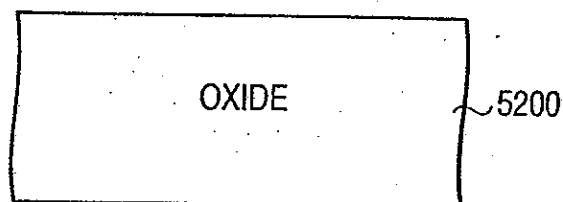


FIG. 82B

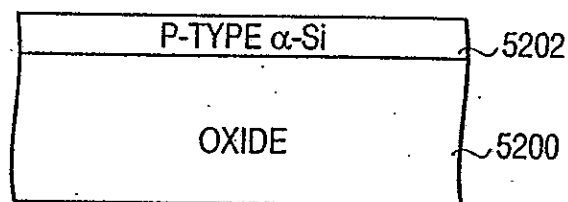
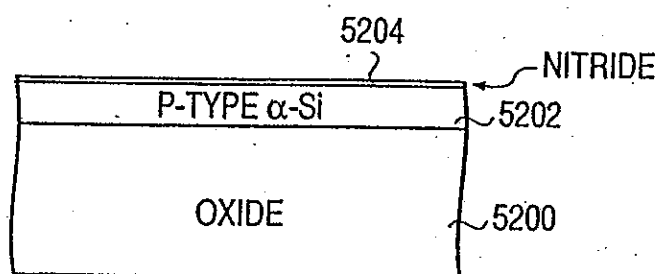


FIG. 82C



59/85 °

FIG. 82D

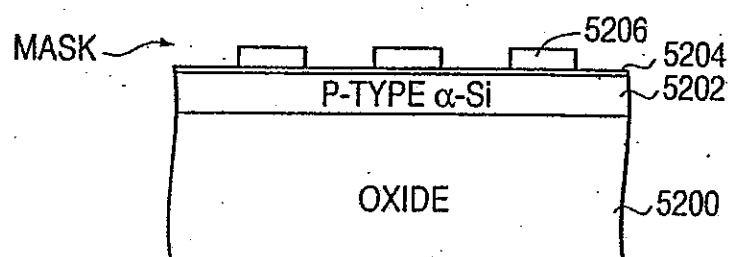


FIG. 82E

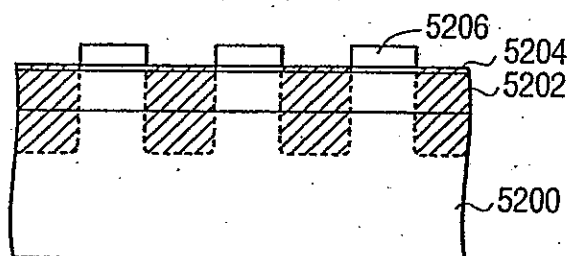
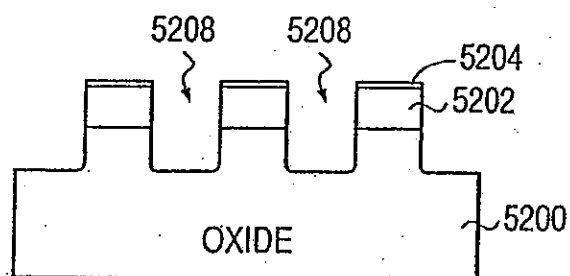


FIG. 82F



60 / 85°

FIG. 82G

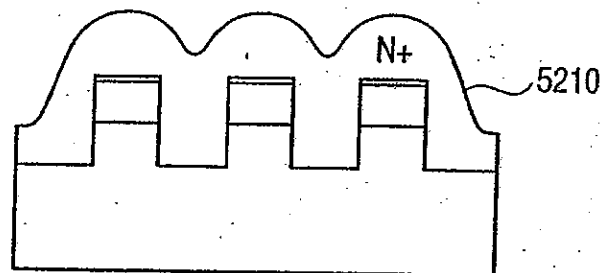


FIG. 82H

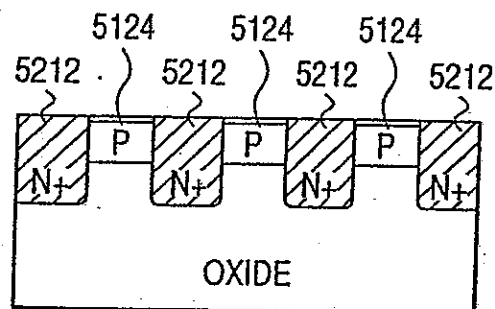
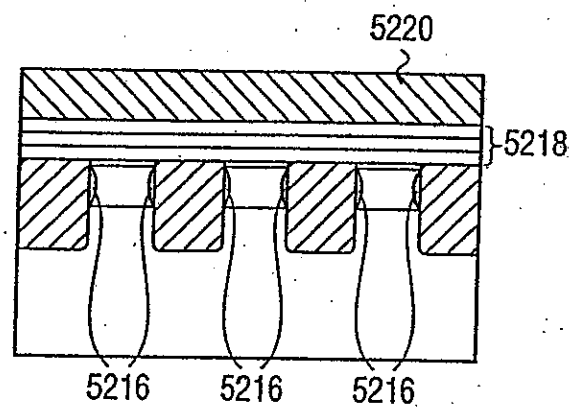


FIG. 82I



61/85 °

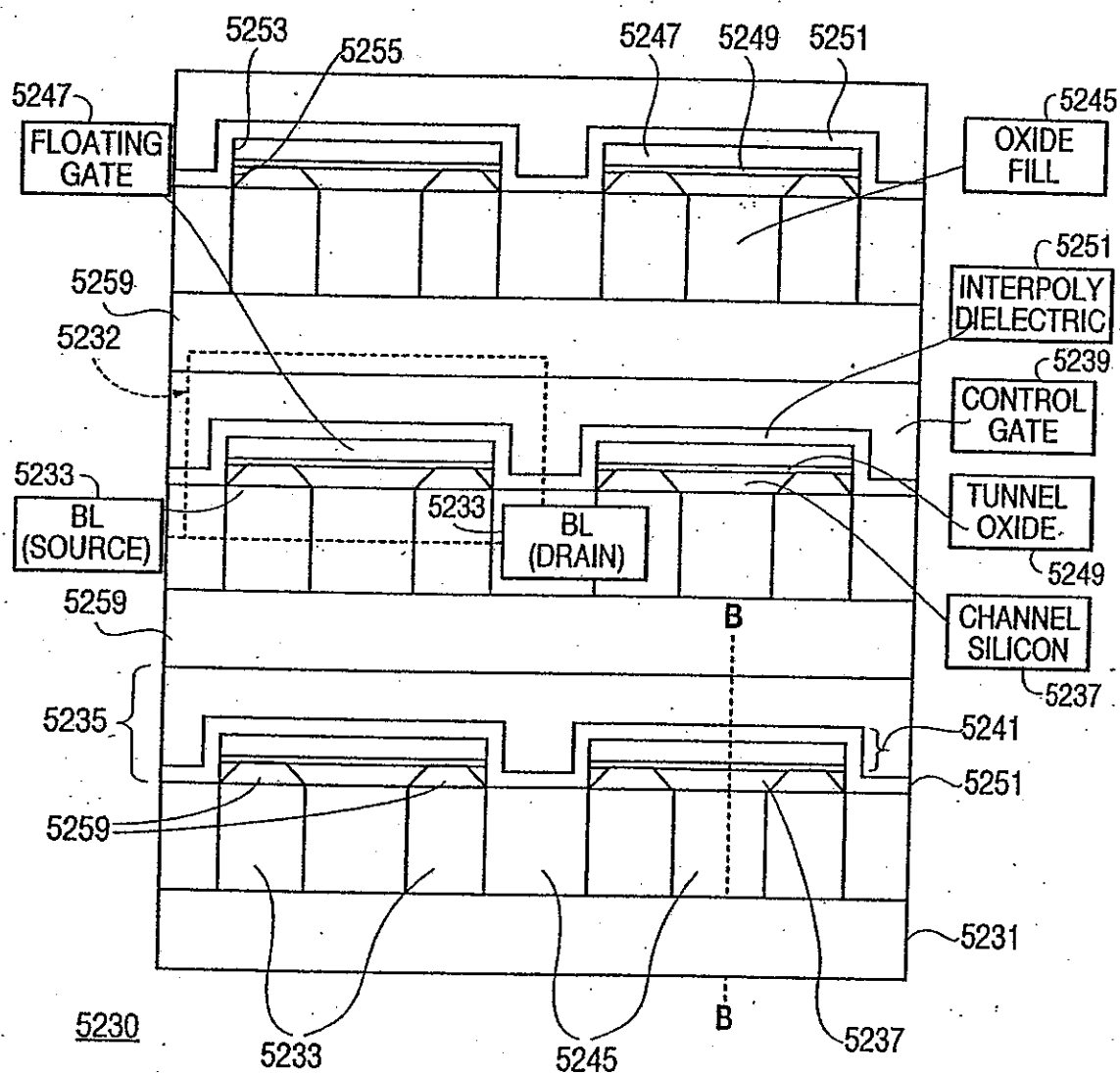
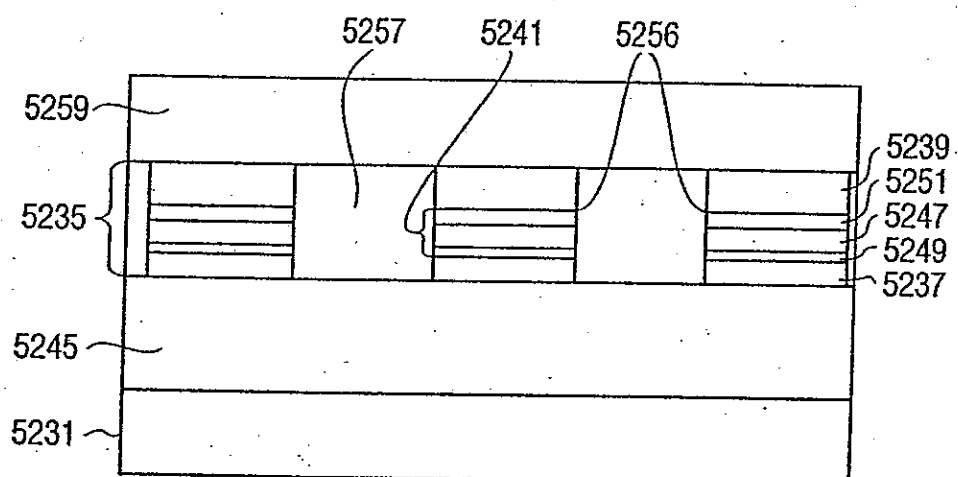
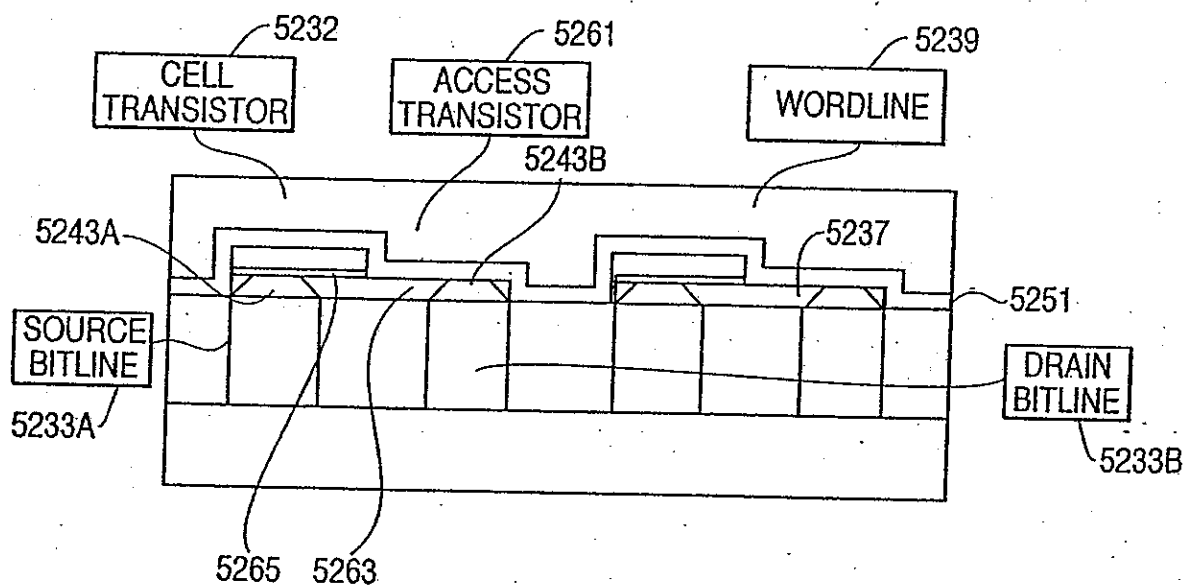
FIG. 83A

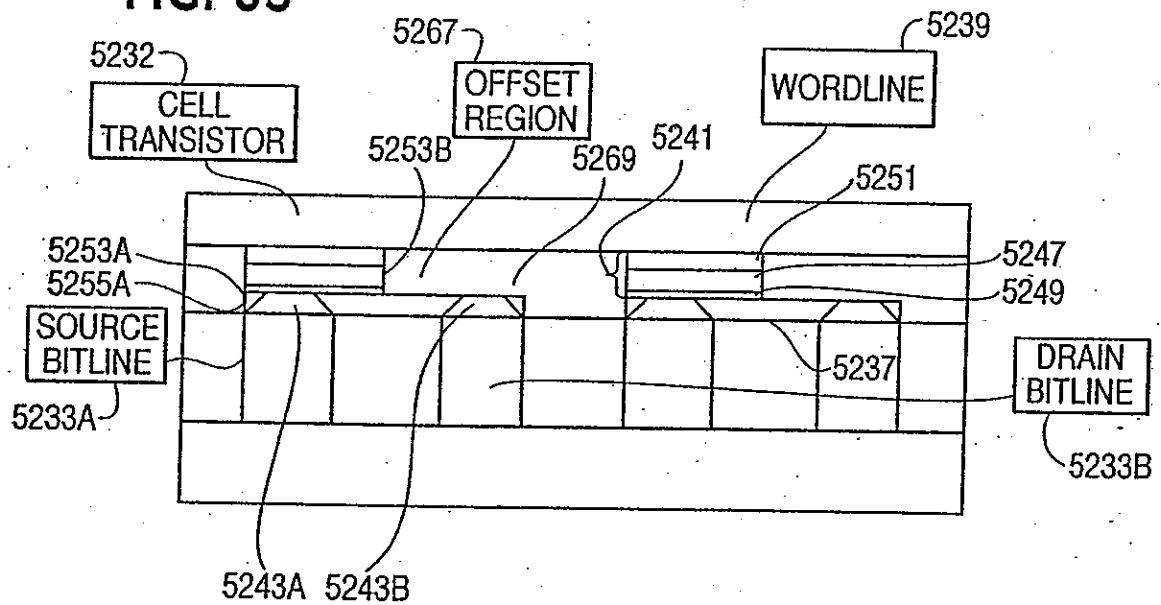
FIG. 83B

63 / 85 °

FIG. 84

64/85

FIG. 85



65 / 85 °

FIG. 86A

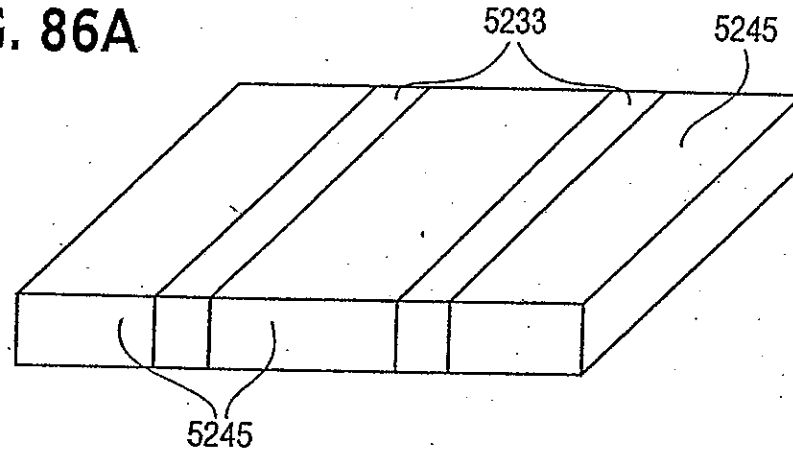


FIG. 86B

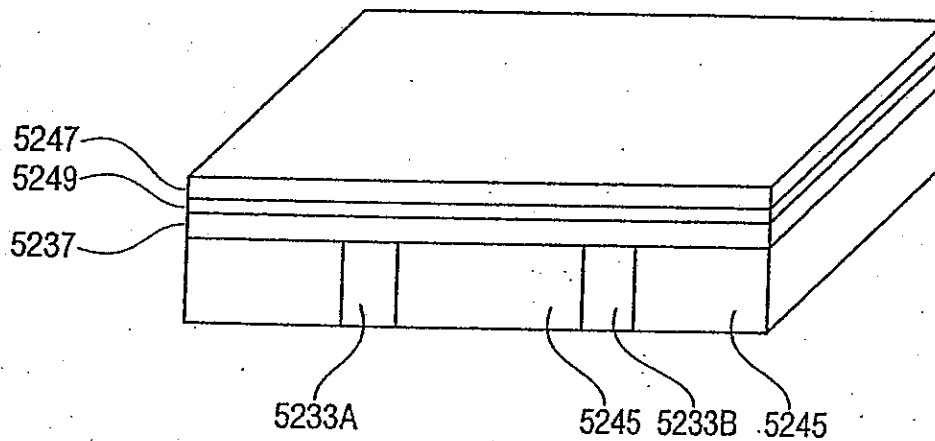
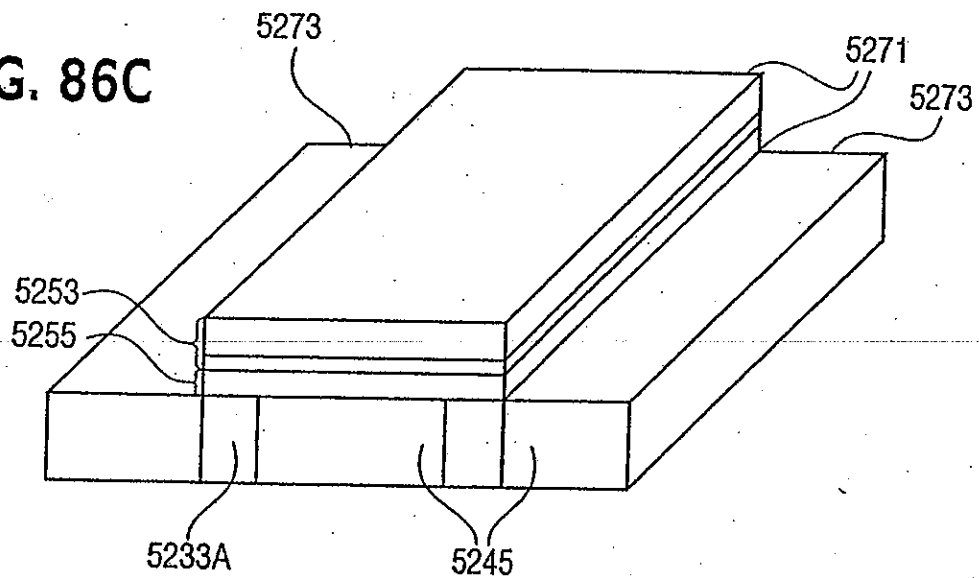
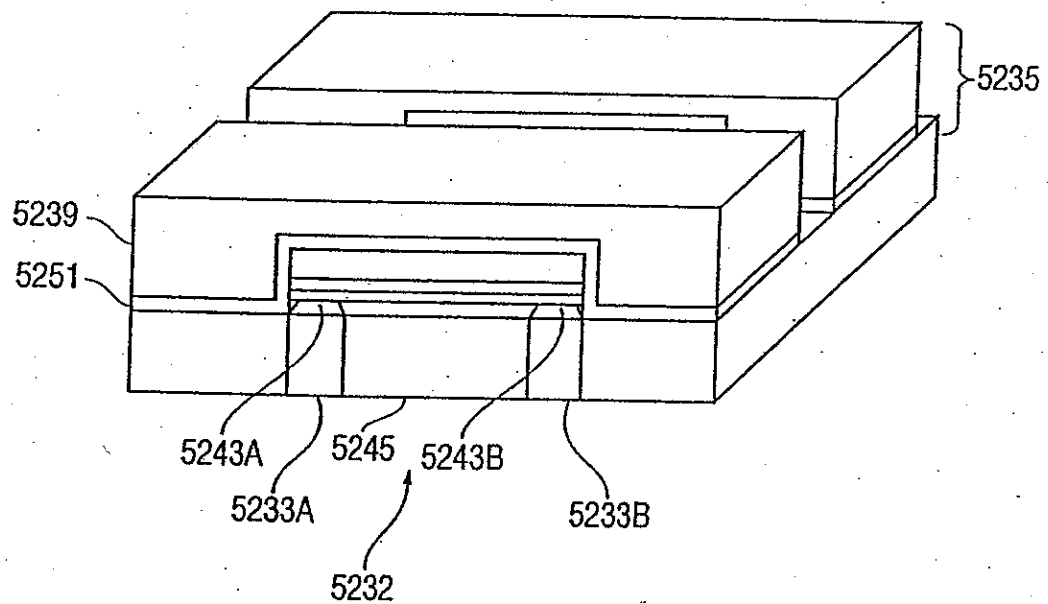


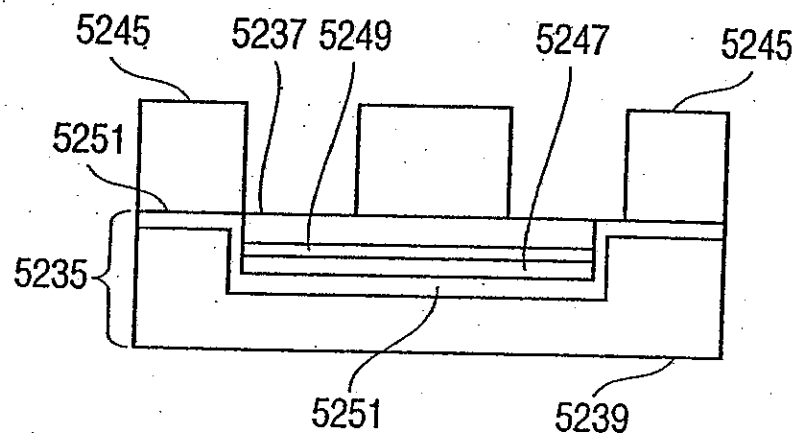
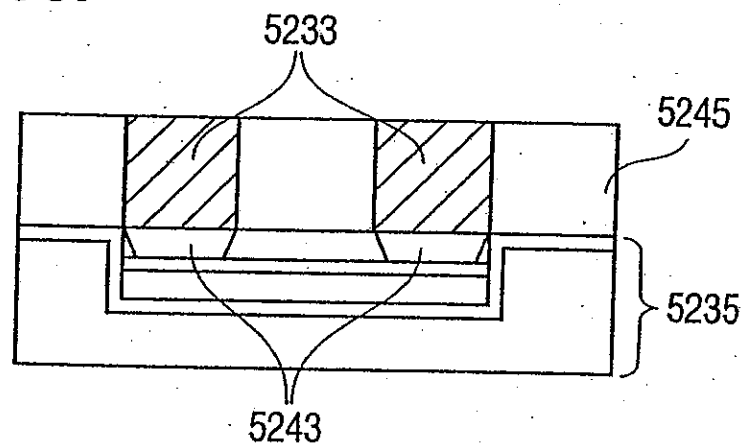
FIG. 86C



66 / 85°

FIG. 86D



67/85^o**FIG. 86E****FIG. 86F**

68 / 85^o

FIG. 86G

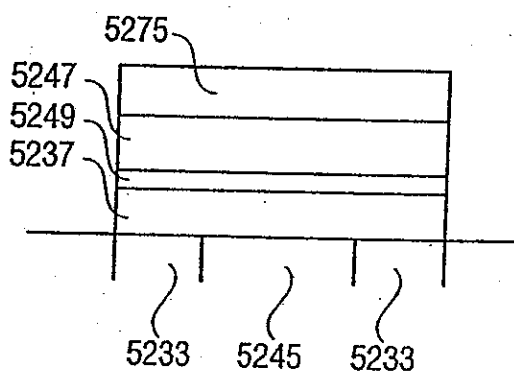


FIG. 86H

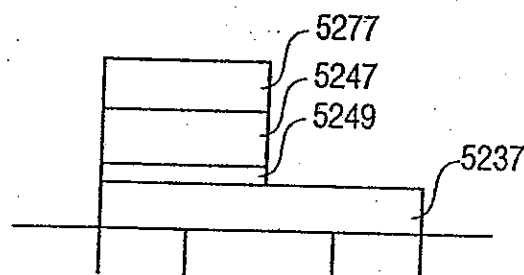


FIG. 86I

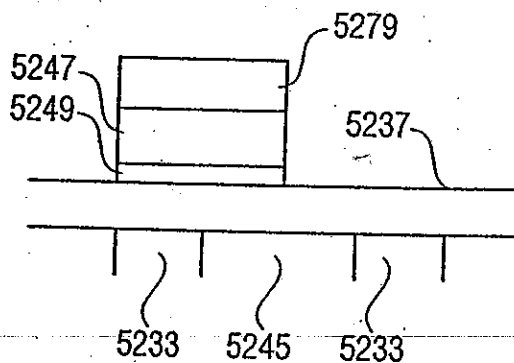
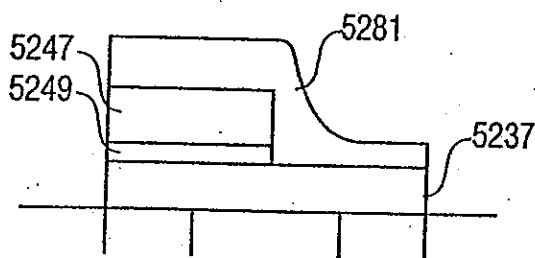
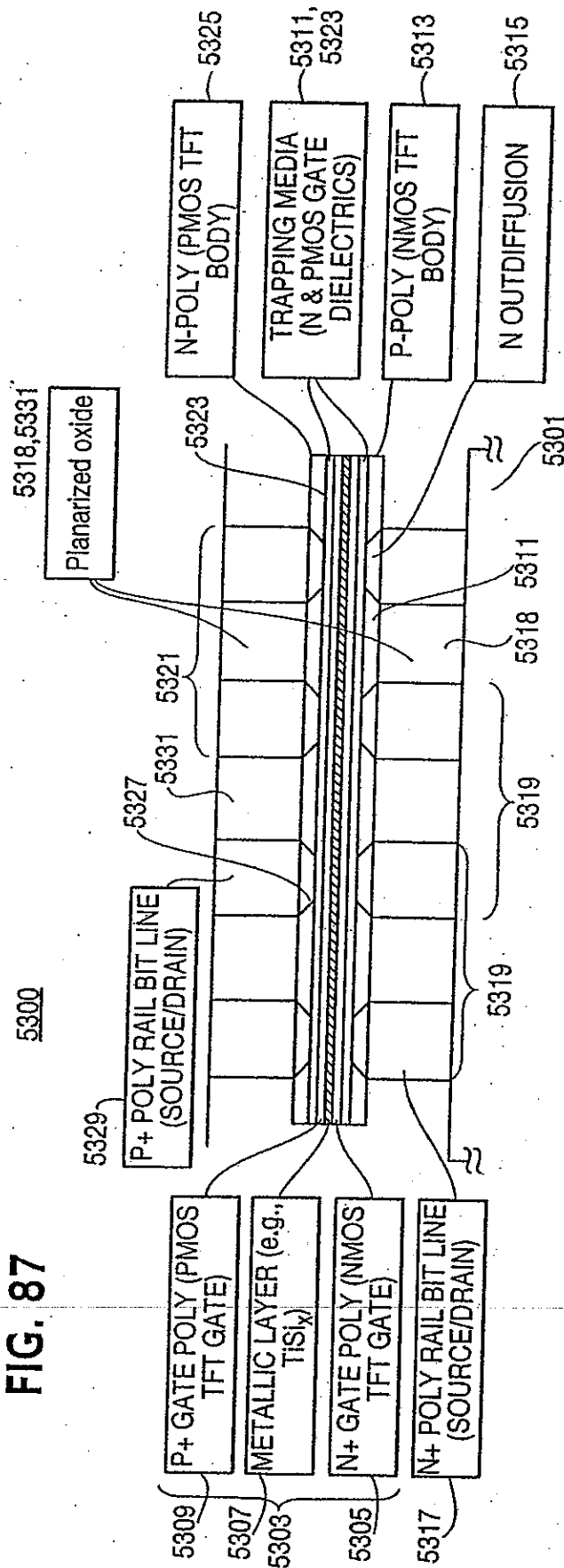


FIG. 86J



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FIG. 87



70 / 85 °

FIG. 88A

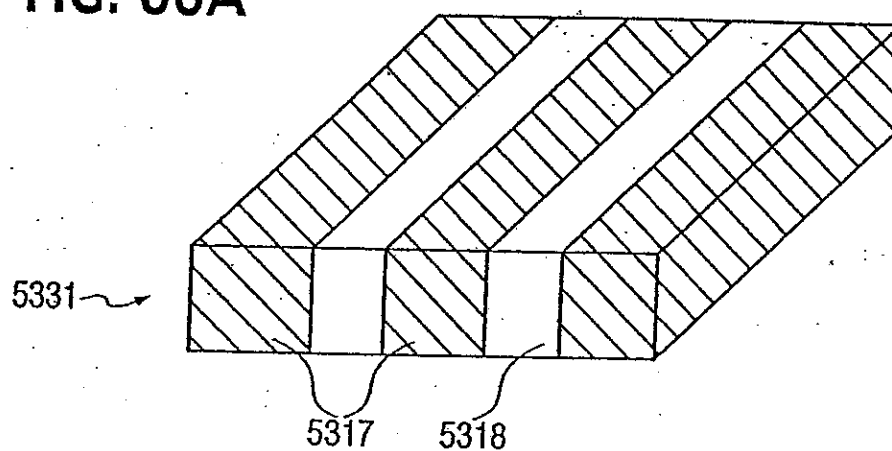
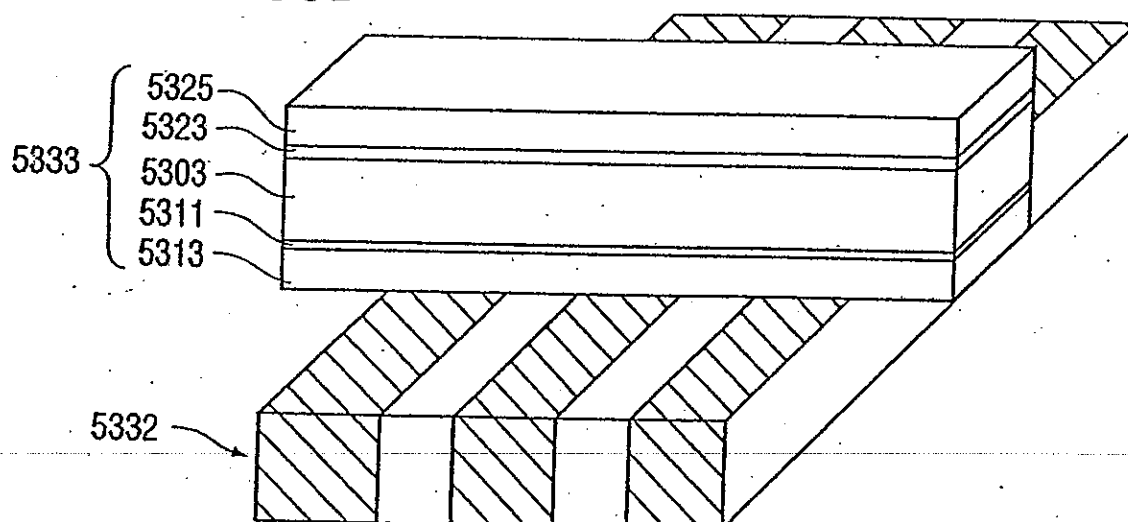
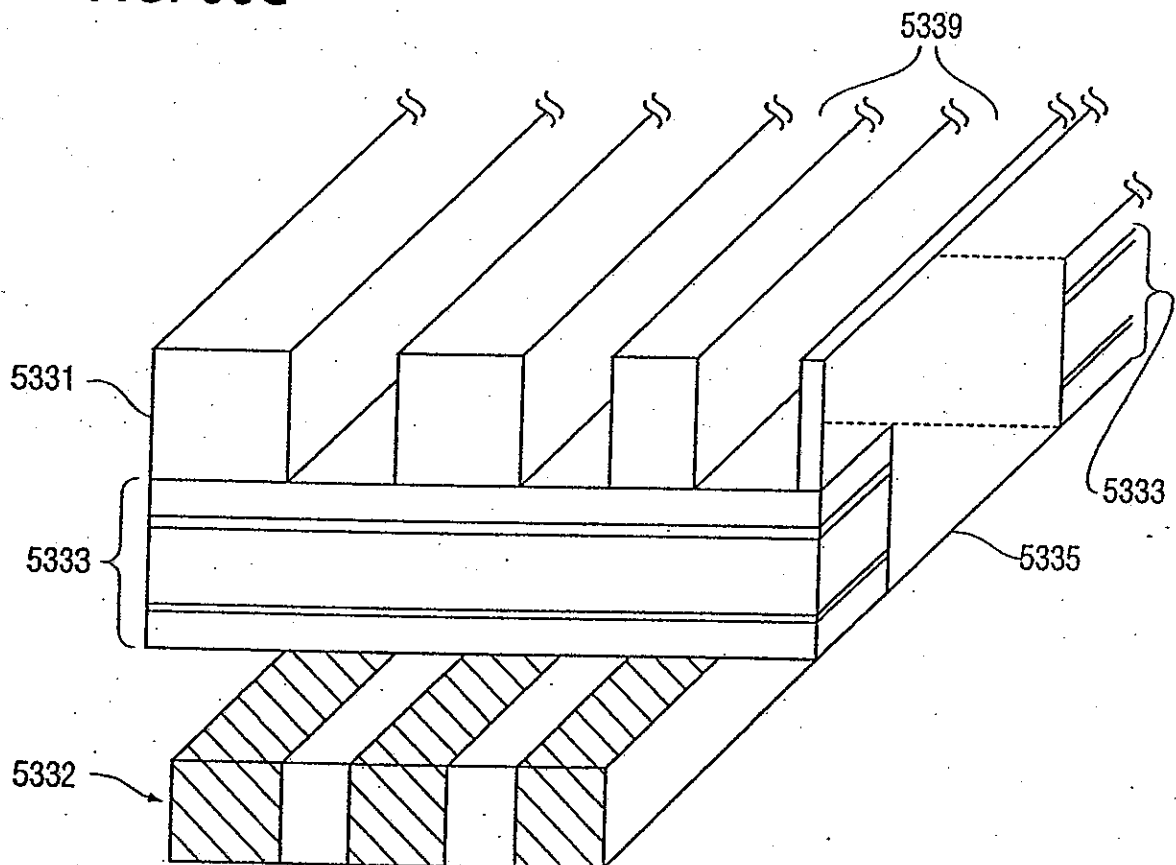


FIG. 88B



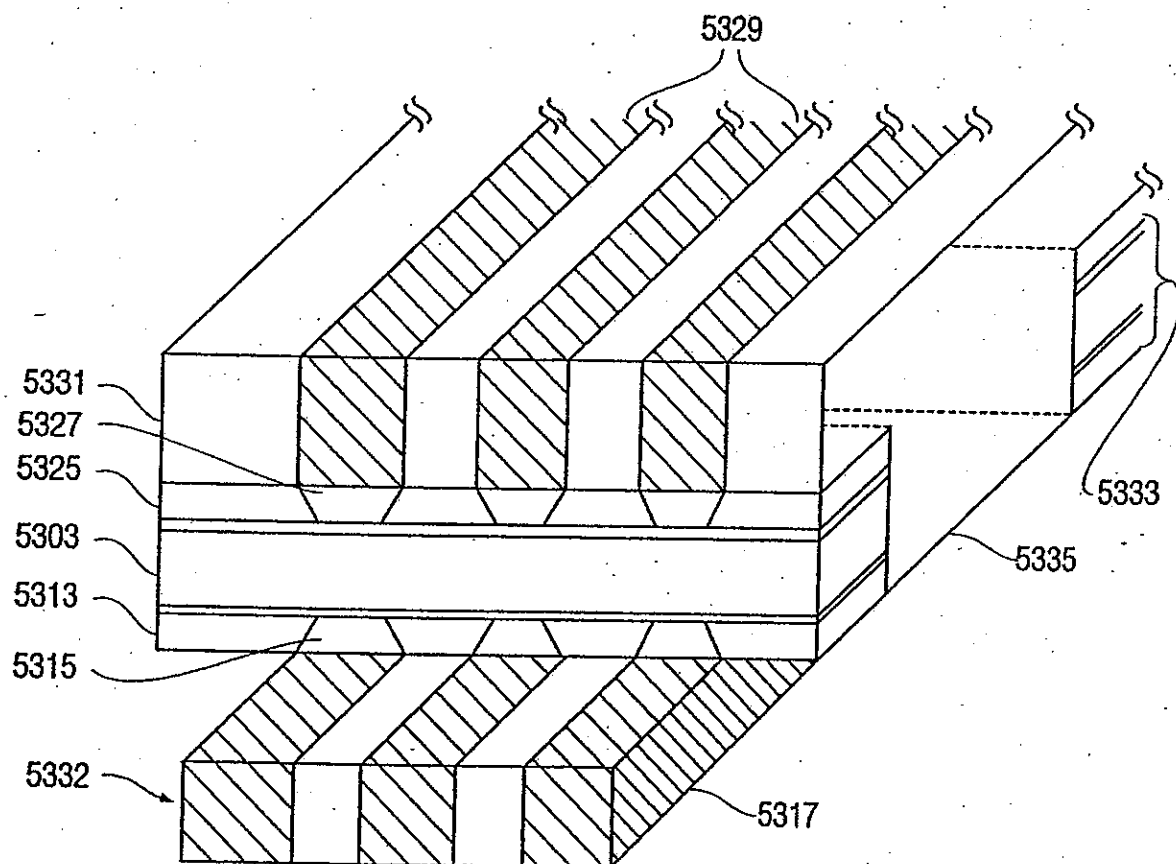
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FIG. 88C



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FIG. 88D



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FIG. 89

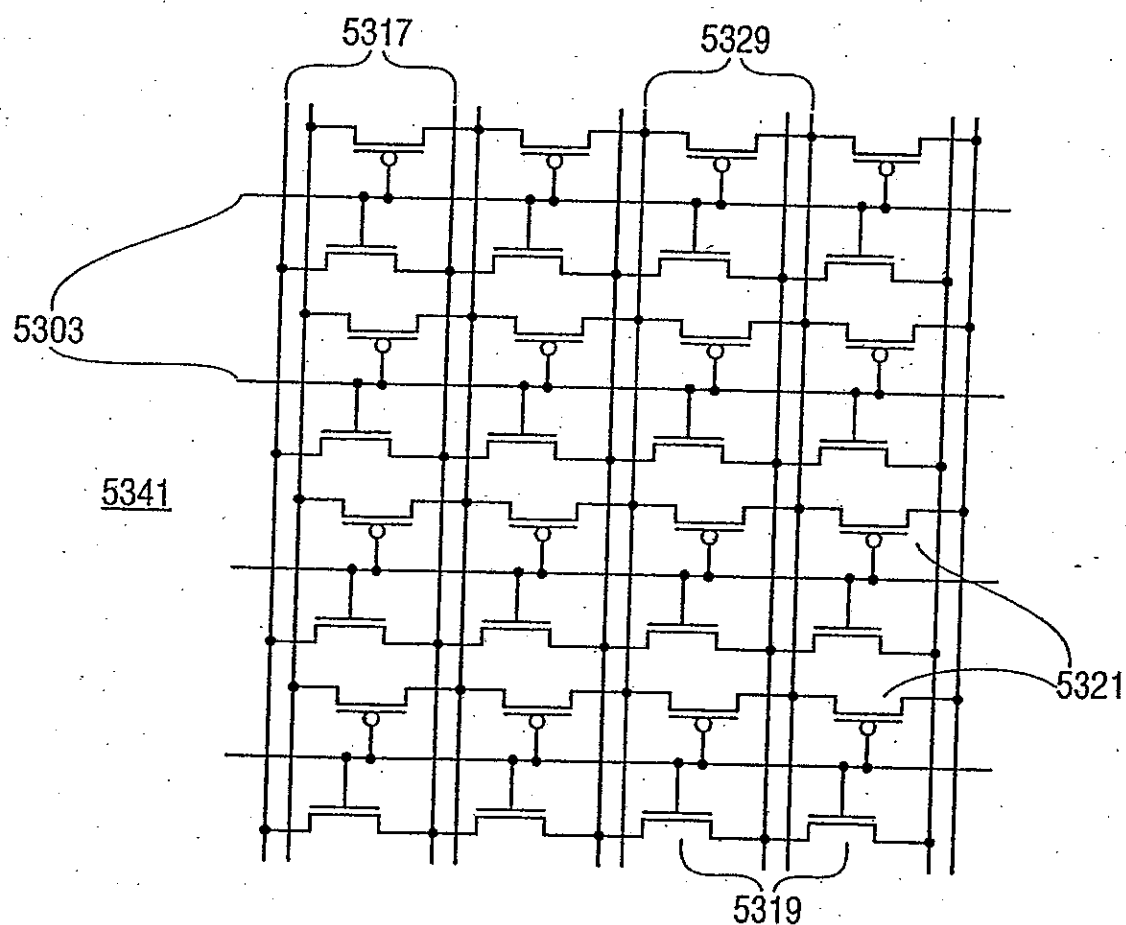
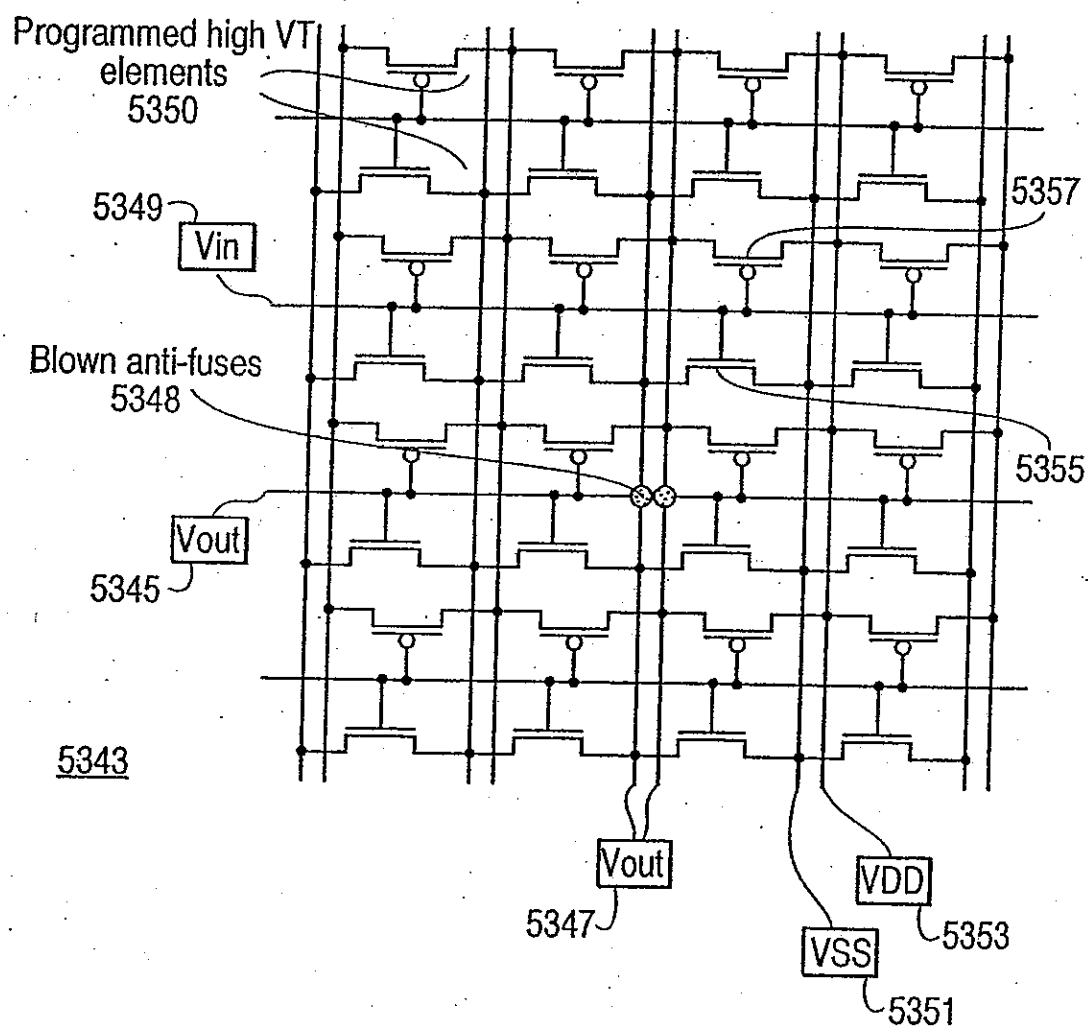
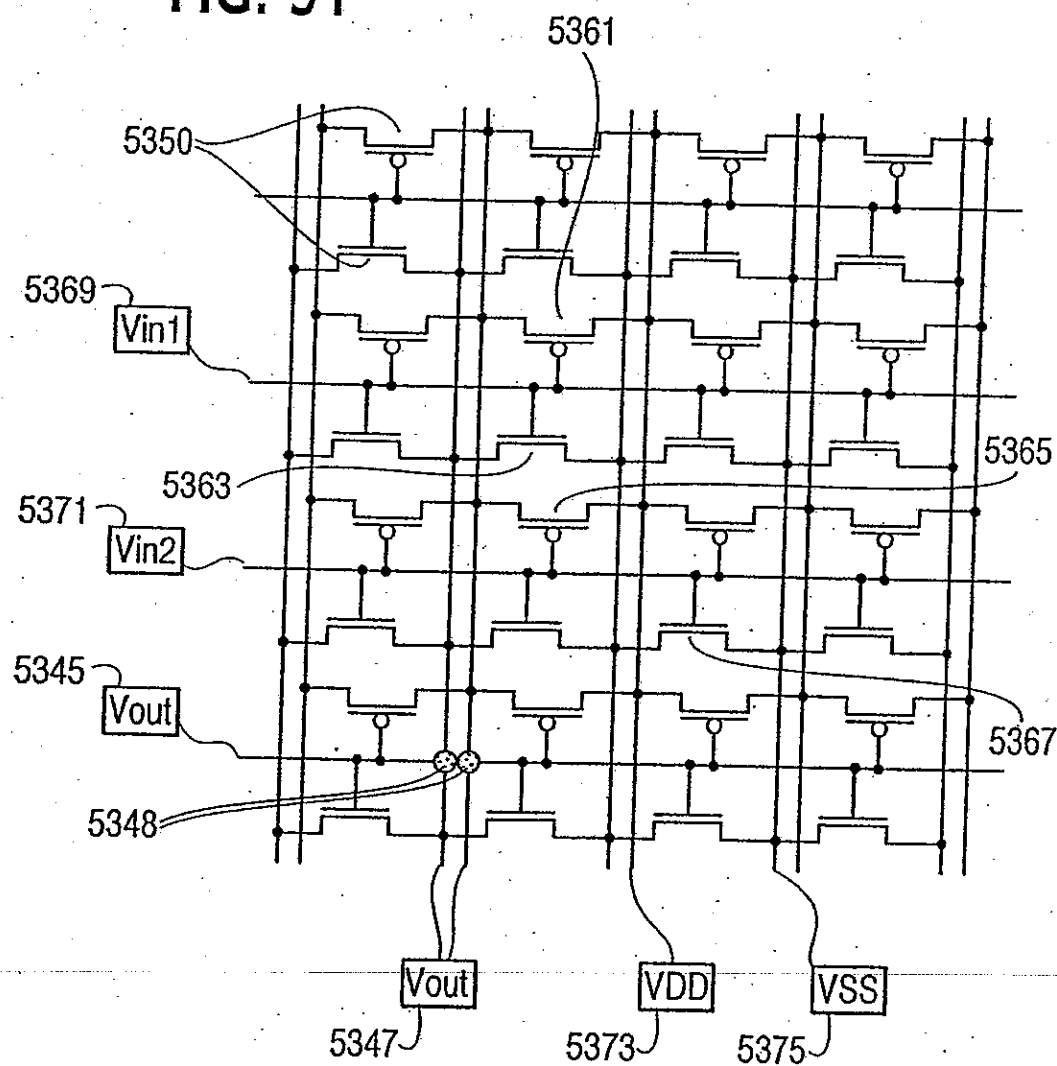


FIG. 90



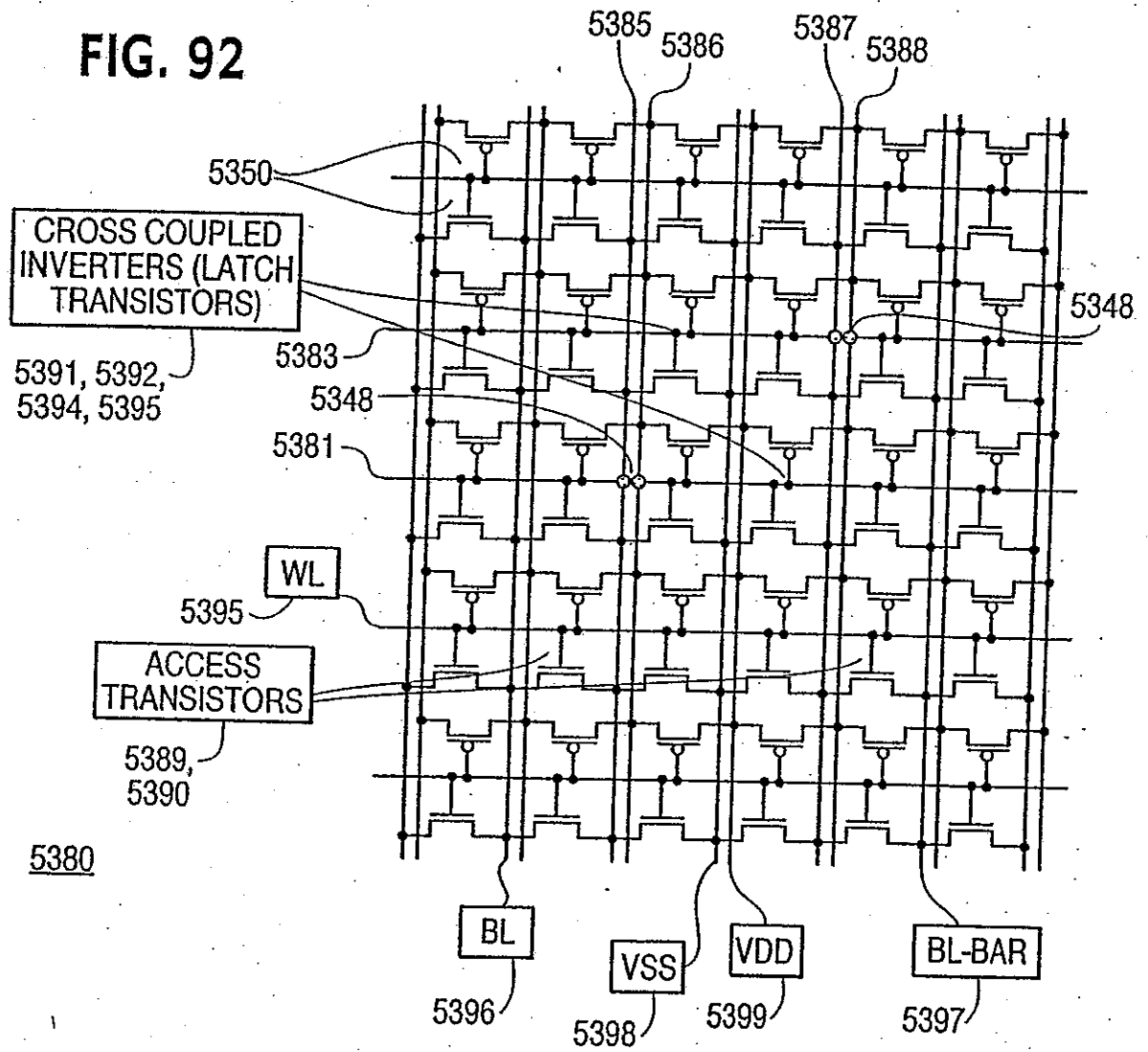
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FIG. 91

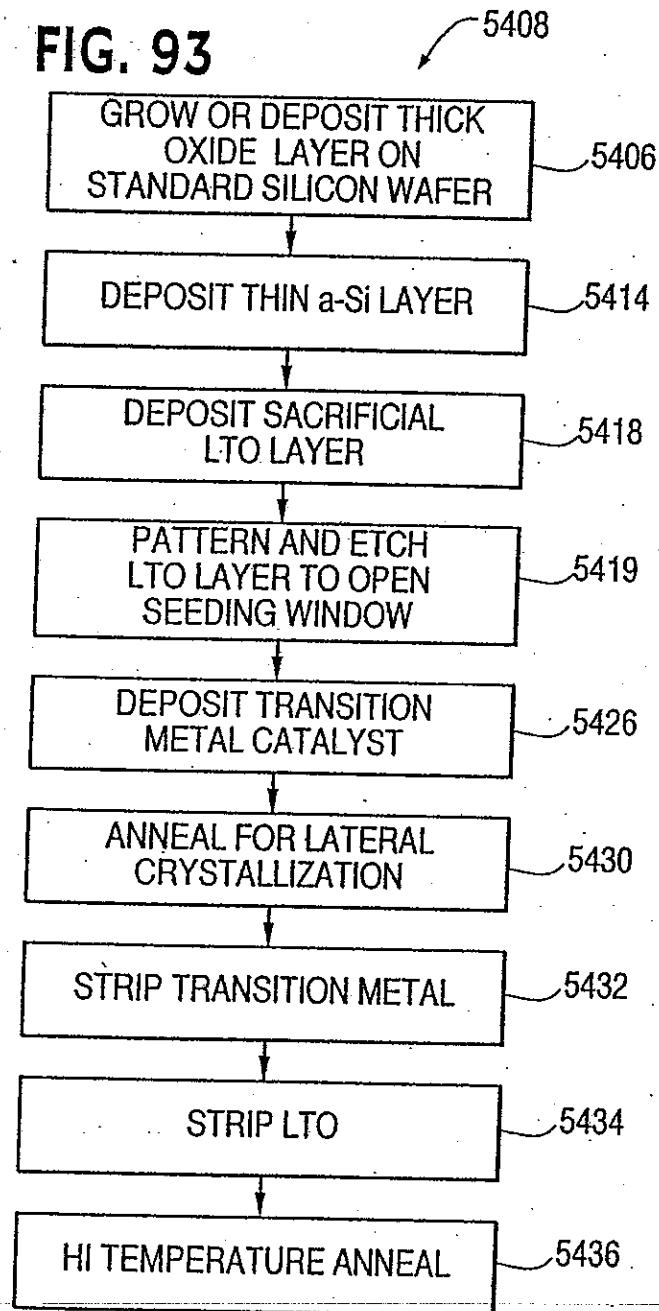


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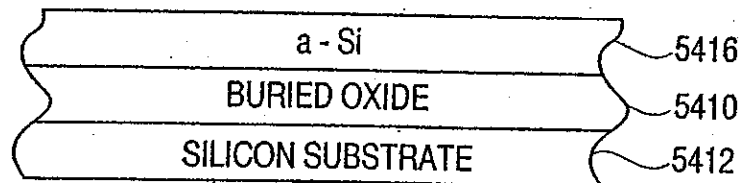
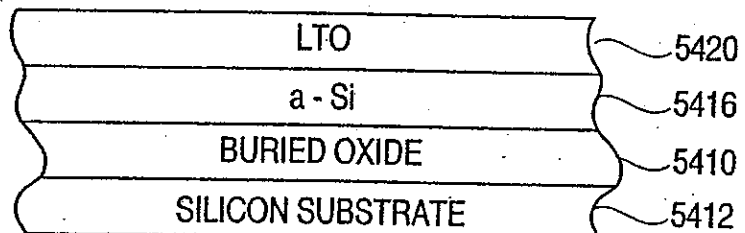
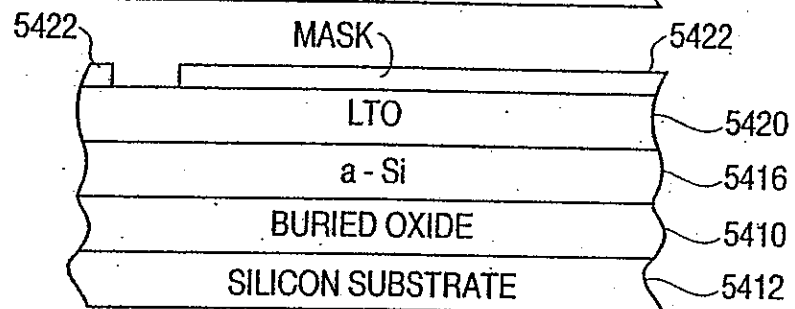
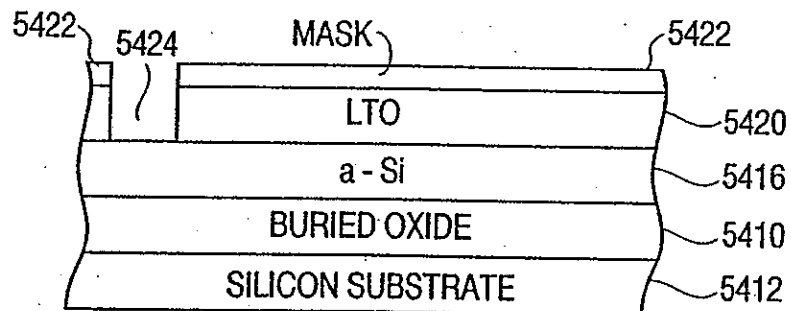
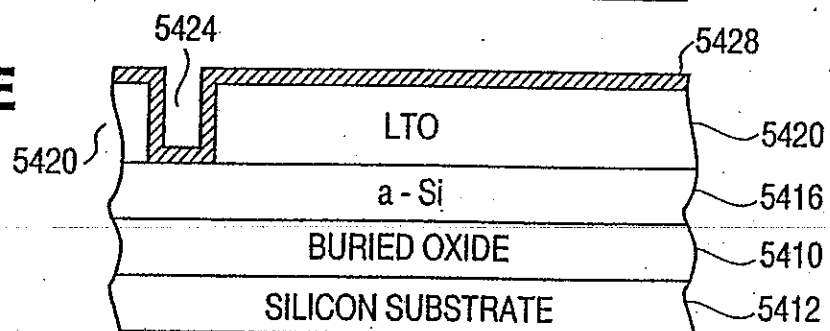
FIG. 92



77 / 85 °

FIG. 93

78/85 °

FIG. 94A**FIG. 94B****FIG. 94C****FIG. 94D****FIG. 94E**

79/85 °

FIG. 94F

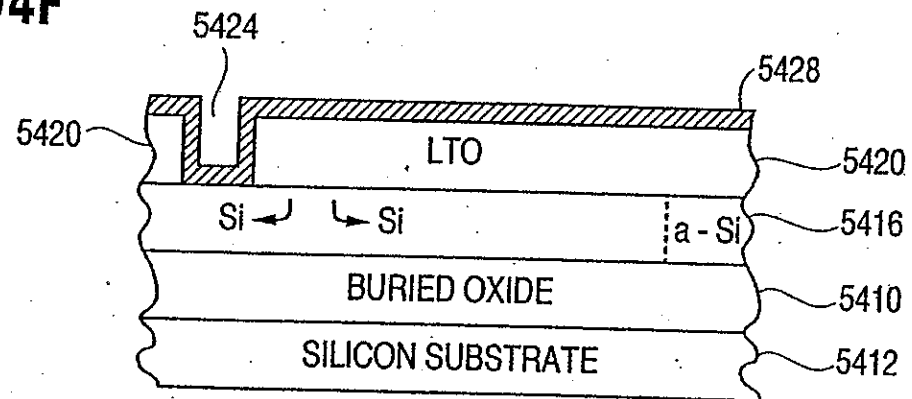


FIG. 94G

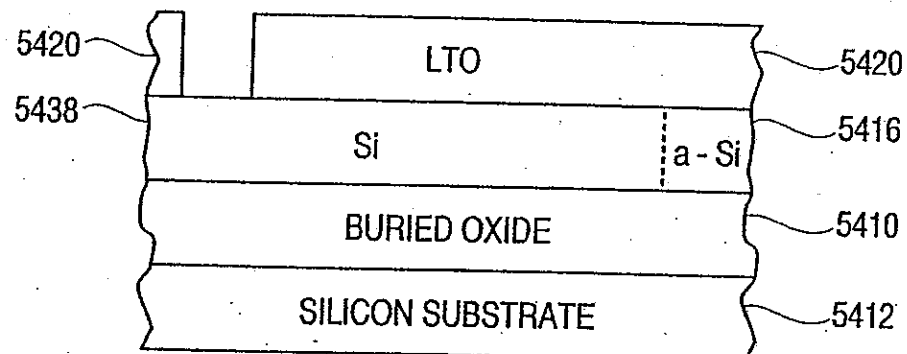
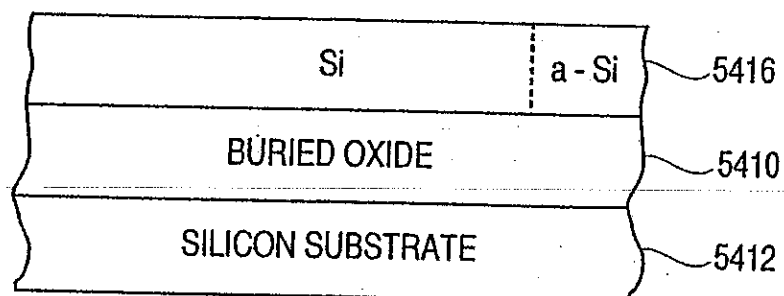
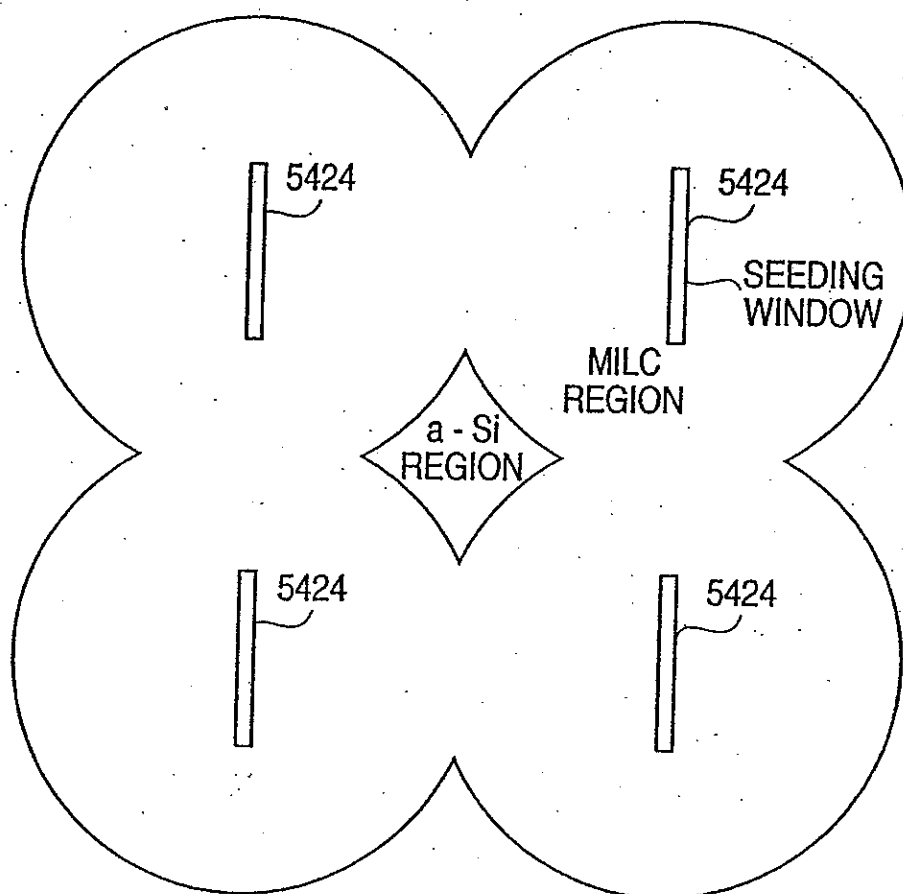


FIG. 94H

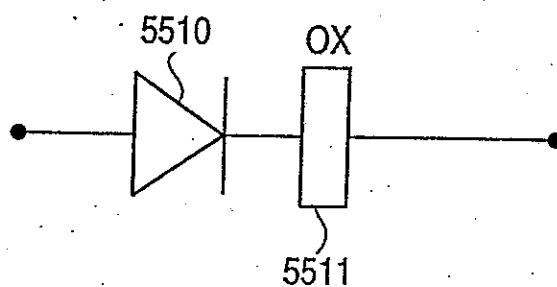
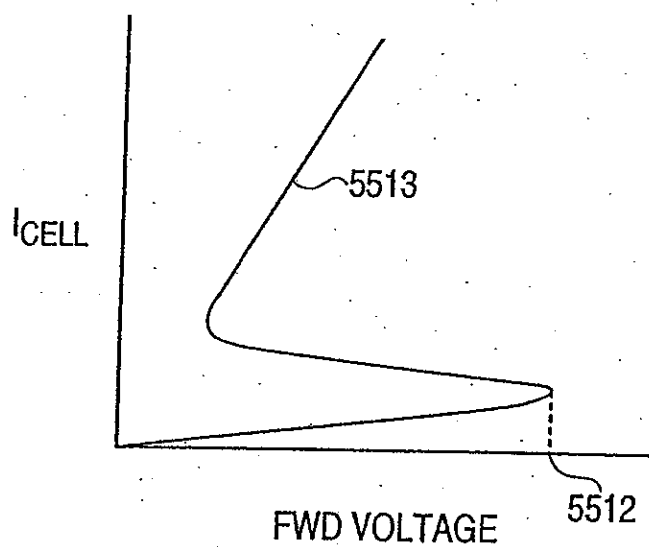


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FIG. 95

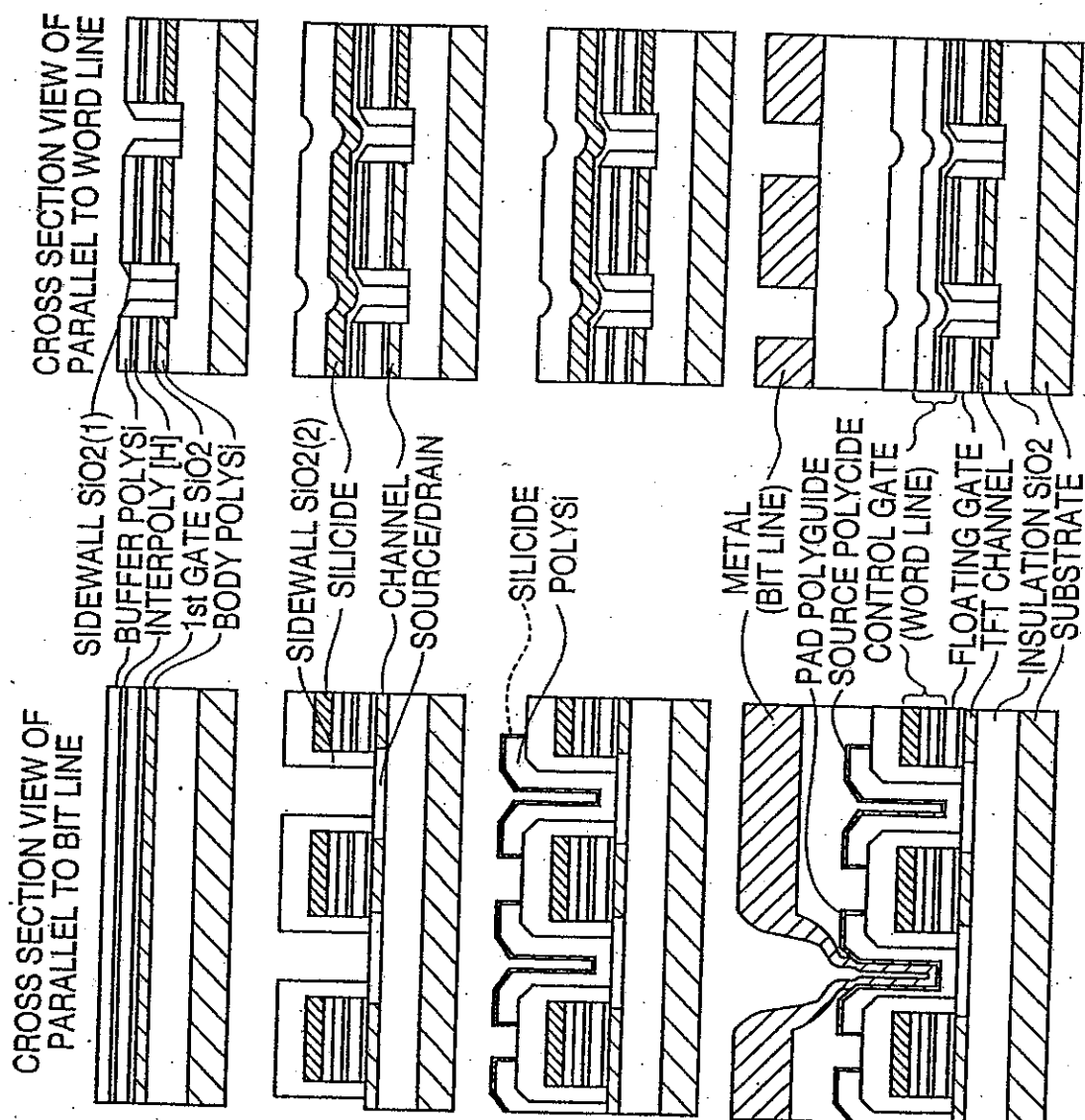


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FIG. 96
(PRIOR ART)**FIG. 97**
(PRIOR ART)

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FIG. 98
(PRIOR ART)



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FIG. 99
(PRIOR ART)

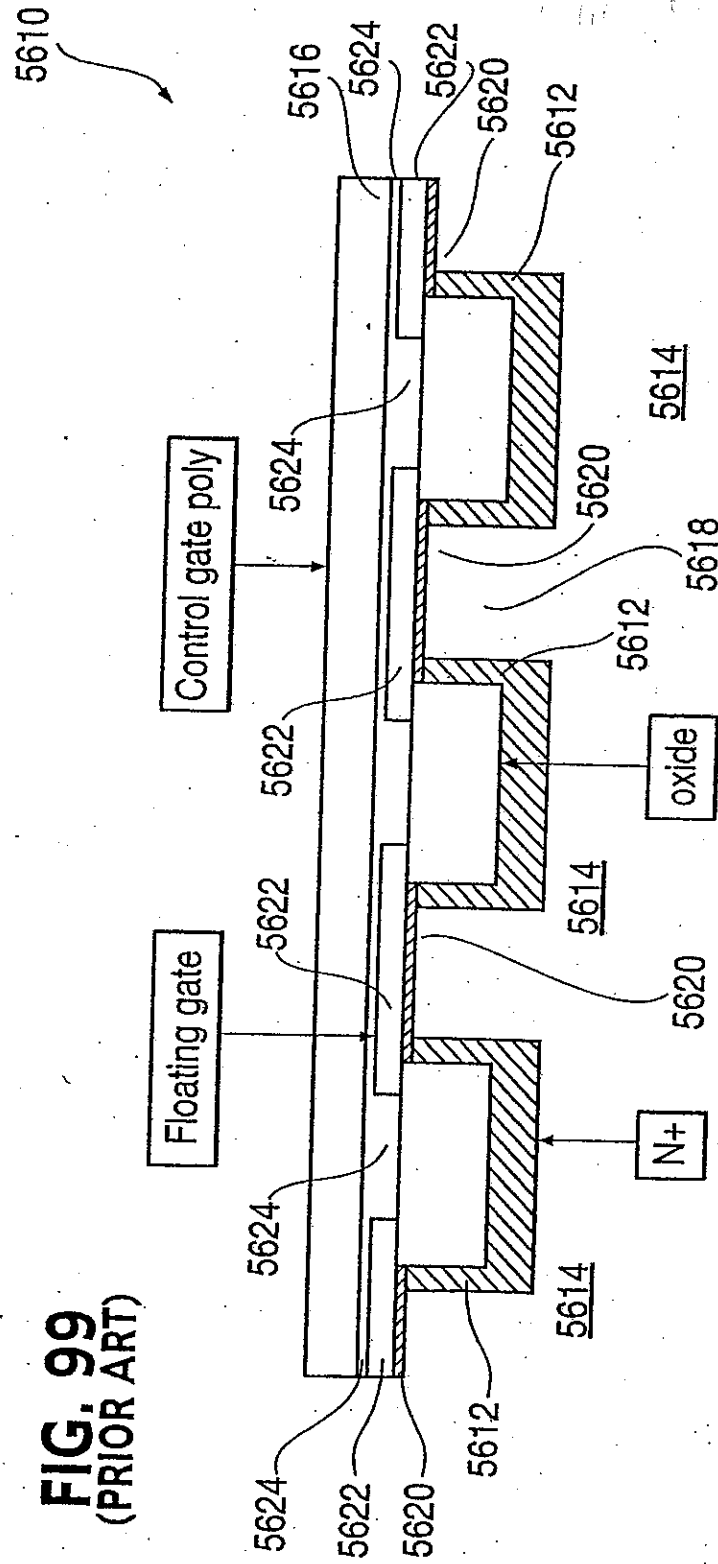
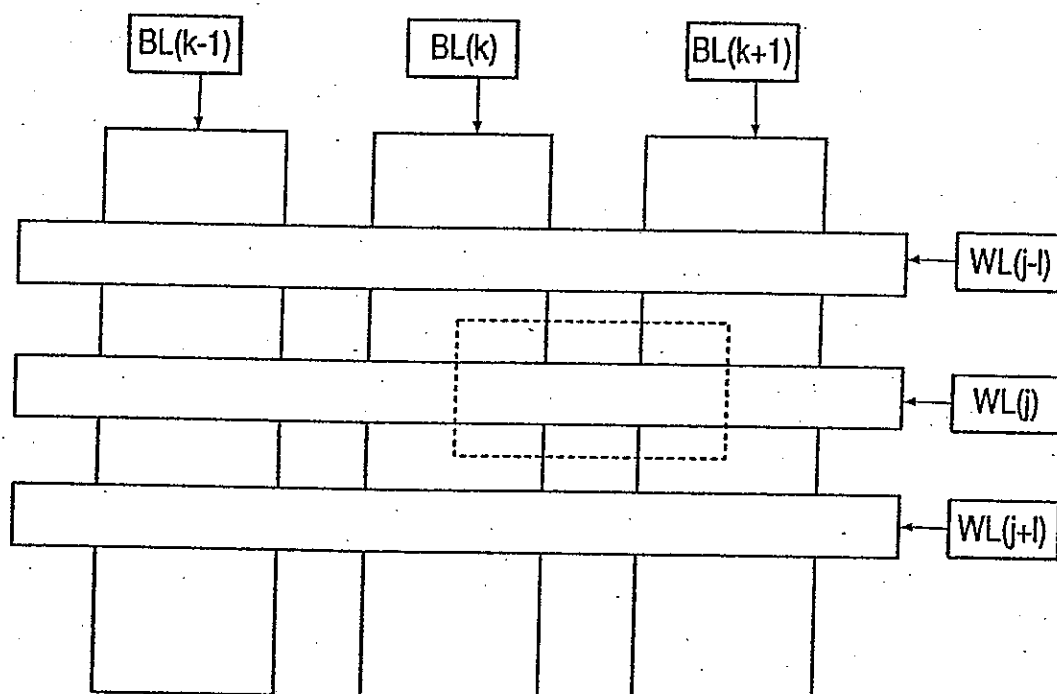


FIG. 100
(PRIOR ART)

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FIG. 101
(PRIOR ART)