

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
HAVING SYNCHRONOUS FUNCTION WITH
A PLURALITY OF EXTERNAL CLOCKS

Abstract of the Disclosure

The present invention is a method and apparatus for reducing the effects of transmission line impedance on the clock signal in a semiconductor device. In a departure from the prior art, the present invention includes multiple clock inputs, located near the device's
5 synchronous input/output ports, reducing the maximum distance that any single internal clock signal must travel and thereby reducing the amount of delay caused by the effects of transmission line impedance on the internal clock signals. The present invention also includes a read only memory ("ROM") to improve the speed of the device and to provide additional space
10 in the highly congested areas between the column decoder and address ports of the device. The ROM is programmed to decipher row address for information that would be beneficial in a redundant column access.

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