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(71) Applicant (for all designated States except US): **SIDENSE
CORP.** [CA/CA]; 349 Terry Fox Drive, Kanata, Ontario
K2K 2V6 (CA).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **KURJANOWICZ,
Wlodek** [CA/CA]; 56 Sherring Crescent, Ottawa, Ontario
K2K 2T1 (CA).

(74) Agents: **HUNG, Shin** et al.; Borden Ladner Gervais LLP,
World Exchange Plaza, 100 Queen Street, Suite 1100, Ot-
tawa, Ontario K1P 1J9 (CA).

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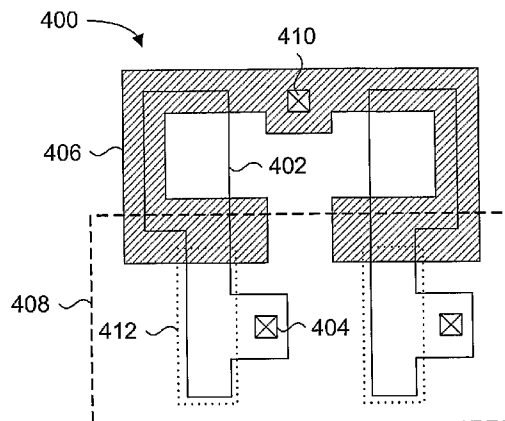
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(54) Title: SPLIT-CHANNEL ANTIFUSE ARRAY ARCHITECTURE



(57) Abstract: Generally, the present invention provides a variable thickness gate oxide anti-fuse transistor device that can be employed in a non-volatile, one-time-programmable (OTP) memory array application. The anti-fuse transistor can be fabricated with standard CMOS technology, and is configured as a standard transistor element having a source diffusion, gate oxide, polysilicon gate and optional drain diffusion. The variable gate oxide underneath the polysilicon gate consists of a thick gate oxide region and a thin gate oxide region, where the thin gate oxide region acts as a localized breakdown voltage zone. A conductive channel between the polysilicon gate and the channel region can be formed in the localized breakdown voltage zone during a programming operation. In a memory array application, a wordline read current applied to the polysilicon gate can be sensed through a bitline connected to the source diffusion, via the channel of the anti-fuse transistor. More specifically, the present invention provides an effective method for utilizing split channel MOS structures as an anti-fuse cell suitable for OTP memories.

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