DESCRIPTION

Title of Invention: PLASMA PROCESSING DEVICE, POWER SUPPLY SYSTEM, AND CONTROL METHOD

Technical Field

[0001] Example embodiments of the present disclosure relate to a plasma processing apparatus, a power supply system, and a control method.

Background Art

[0002] A plasma processing apparatus is used in plasma processing of a substrate. In the plasma processing apparatus, bias radio frequency power is used to attract ions from a plasma generated in a chamber to a substrate. Patent Literature 1 below discloses a plasma processing apparatus that modulates the power level and frequency of bias radio frequency power.

Citation List

Patent Literature

[0003] [Patent Literature 1] Japanese Unexamined Patent Publication No. 2009-246091

Summary of Invention

Technical Problem

[0004] The present disclosure provides a technique for identifying, at low cost, a degree of reflection of source radio frequency power in a waveform cycle of an electrical bias, and adjusting a source frequency of the source radio frequency power.

Solution to Problem

[0005] In one example embodiment, a plasma processing apparatus is disclosed. The plasma processing apparatus includes a chamber, a substrate support in the chamber, a radio frequency power supply, a bias supply, a sensor, a detector, an A/D converter, and a power supply controller. The radio frequency power supply is configured to supply source radio frequency power to generate a plasma from a gas in the chamber. The bias supply is configured to supply an electrical bias to the substrate support to attract ions from the plasma to a substrate on the substrate support. The sensor is configured to acquire a sensor signal reflecting a degree of reflection of the source radio frequency power. The detector is configured to detect an envelope signal of the sensor signal. The A/D converter is configured to perform A/D conversion on the envelope signal output from the detector. The power supply controller is configured to, in accordance with the degree of reflection in a waveform cycle of the electrical bias identified from a plurality of digital values generated by the A/D converter from the envelope signal in the waveform cycle, or in accordance with the degree of reflection in each of the plurality of phase periods that divide the waveform cycle, adjust a source frequency of the source radio frequency power for each of a plurality of phase periods to reduce the degree of reflection in a subsequent waveform cycle of the electrical bias. A sampling frequency of the A/D converter is not less than twice a product of a bias frequency, which is a reciprocal of a time length of the waveform cycle, and a number of the plurality of phase periods within the waveform cycle, and is not greater than a source frequency of the source radio frequency power.

Advantageous Effects of Invention

[0006] According to one example embodiment, a technique is provided for identifying, at low cost, a degree of reflection of source radio frequency power in a waveform cycle of an electrical bias, and adjusting a source frequency of the source radio frequency power.

Brief Description of Drawings

[0007] FIG. 1 illustrates an example configuration of a plasma processing system.

FIG. 2 illustrates an example configuration of the capacitively coupled plasma processing apparatus.

FIG. 3 is a diagram illustrating a plasma processing apparatus according to one example embodiment.

FIG. 4 is a diagram illustrating an example of a waveform of an electrical bias.

Each of FIG. 5(a) and FIG. 5(b) is a timing chart of an example of source radio frequency power and an electrical bias in a plasma processing apparatus according to one example embodiment.

FIG. 6 is a flowchart illustrating a control method according to one example embodiment.

FIG. 7 is a flowchart illustrating an example of a feedback process.

FIG. 8 is a flowchart illustrating an example of processing in operation ST9 illustrated in FIG. 7.

FIG. 9 is a flowchart illustrating another example of a feedback process.

FIG. 10 is a flowchart illustrating an example of processing in

operation ST9a illustrated in FIG. 9.

FIG. 11 is a timing chart of an example of source radio frequency power and an electrical bias in a plasma processing apparatus according to one example embodiment.

FIG. 12 is a timing chart related to a power supply system according to one example embodiment.

FIG. 13 is a timing chart related to a power supply system according to one example embodiment.

FIG. 14 is a flowchart illustrating a control method of a first example.

FIG. 15 is a diagram for explaining the control method of the first example illustrated in FIG. 14.

FIG. 16 is a flowchart illustrating a control method of a second example.

FIG. 17 is a diagram for explaining the control method of the second example illustrated in FIG. 16.

FIG. 18 is a diagram for explaining the control method of the second example illustrated in FIG. 16.

FIG. 19 is a diagram for explaining the control method of the second example illustrated in FIG. 16.

FIG. 20 is a diagram for explaining the control method of the second example illustrated in FIG. 16.

FIG. 21 is a flowchart illustrating a control method of a third example.

FIG. 22 is a diagram for explaining the control method of the third example illustrated in FIG. 21.

FIG. 23 is a block diagram of processing circuitry for performing computer-based operations described herein.

Description of Embodiments

[0008] Hereinafter, various example embodiments will be described in detail with reference to the drawings. In the drawings, the same or equivalent portions are denoted by the same reference signs.

[0009] FIG. 1 illustrates an example configuration of a plasma processing system. In an embodiment, the plasma processing system includes a plasma processing apparatus 1 and a controller 2. The plasma processing system is an example substrate processing system, and the plasma processing apparatus 1 is an example substrate processing apparatus. The plasma processing apparatus 1 includes a plasma processing chamber 10, a substrate support 11, and a plasma generator 12. The plasma processing chamber 10 has a plasma processing space. The plasma processing chamber 10 further has at least one gas inlet for supplying at least one process gas into the plasma processing space and at least one gas outlet for exhausting gases from the plasma processing space. The gas inlet is connected to a gas supply 20 described below and the gas outlet is connected to a gas exhaust system 40 described below. The substrate support 11 is disposed in the plasma processing space and has a substrate supporting surface for supporting a substrate.

[0010] The plasma generator 12 is configured to generate a plasma from the at least one process gas supplied into the plasma processing space. The plasma formed in the plasma processing space may be, for example, a capacitively coupled plasma (CCP), an inductively coupled plasma (ICP), an electron-cyclotron-resonance (ECR) plasma, a helicon wave

plasma (HWP), or a surface wave plasma (SWP). Various types of plasma generators may also be used, such as an alternating current (AC) plasma generator and a direct current (DC) plasma generator. In an embodiment, an AC signal (AC power) used in the AC plasma generator has a frequency in a range of 100 kHz to 10 GHz. Hence, examples of the AC signal include a radio frequency (RF) signal and a microwave signal. In an embodiment, the RF signal has a frequency in a range of 100 kHz to 150 MHz.

[0011] The controller 2 processes computer executable instructions causing the plasma processing apparatus 1 to perform various steps described in this disclosure. The controller 2 may be configured to control individual components of the plasma processing apparatus 1 such that these components execute the various steps. In an embodiment, the controller 2 may be partially or entirely incorporated into the plasma processing apparatus 1. The controller 2 may include a processor 2a1, a storage 2a2, and a communication interface 2a3. The controller 2 is implemented in, for example, a computer 2a. The processor 2a1 may be configured to read a program from the storage 2a2, and then perform various control operations by executing the read program. This program may be preliminarily stored in the storage 2a2 or retrieved via any medium, when needed. The retrieved program is stored in the storage 2a2, and then the processor 2a1 reads and executes the program from the storage 2a2. The medium may be any of various storage media which can be accessed by the computer 2a or may be a communication line connected to the communication interface 2a3. The processor 2a1 may be a central processing unit (CPU). The storage 2a2

may include a random access memory (RAM), a read only memory (ROM), a hard disk drive (HDD), a solid state drive (SSD), or any combination thereof. The communication interface 2a3 may communicate with the plasma processing apparatus 1 via a communication line, such as a local area network (LAN).

[0012] An example configuration of a capacitively coupled plasma processing apparatus, which is an example of the plasma processing apparatus 1, will now be described. FIG. 2 illustrates an example configuration of the capacitively coupled plasma processing apparatus.

[0013] The capacitively coupled plasma processing apparatus 1 includes a plasma processing chamber 10, a gas supply 20, an electric power source 30, and a gas exhaust system 40. The plasma processing apparatus 1 further includes a substrate support 11 and a gas introduction unit. The gas introduction unit is configured to introduce at least one process gas into the plasma processing chamber 10. The gas introduction unit includes a showerhead 13. The substrate support 11 is disposed in the plasma processing chamber 10. The showerhead 13 is disposed above the substrate support 11. In an embodiment, the showerhead 13 functions as at least part of the ceiling of the plasma processing chamber 10. The plasma processing chamber 10 has a plasma processing space 10s that is defined by the showerhead 13, a sidewall 10a of the plasma processing chamber 10, and the substrate support 11. The plasma processing chamber 10 is grounded. The showerhead 13 and the substrate support 11 are electrically insulated from the housing of the plasma processing chamber 10.

[0014] The substrate support 11 includes a body 111 and a ring assembly

112. The body 111 has a central region 111a for supporting a substrate W and an annular region 111b for supporting the ring assembly 112. An example of the substrate W is a wafer. The annular region 111b of the body 111 surrounds the central region 111a of the body 111 in plan view. The substrate W is disposed on the central region 111a of the body 111, and the ring assembly 112 is disposed on the annular region 111b of the body 111 so as to surround the substrate W on the central region 111a of the body 111. Thus, the central region 111a is also called a substrate supporting surface for supporting the substrate W, while the annular region 111b is also called a ring supporting surface for supporting the ring assembly 112.

[0015] In an embodiment, the body 111 includes a base 1110 and an electrostatic chuck 1111. The base 1110 includes a conductive member. The conductive member of the base 1110 can function as a lower electrode. The electrostatic chuck 1111 is disposed on the base 1110. The electrostatic chuck 1111 includes a ceramic member 1111a and an electrostatic electrode 1111b disposed in the ceramic member 1111a. The ceramic member 1111a has the central region 111a. In an embodiment, the ceramic member 1111a also has the annular region 111b. Any other member, such as an annular electrostatic chuck or an annular insulating member, surrounding the electrostatic chuck 1111 may have the annular region 111b. In this case, the ring assembly 112 may be disposed on either the annular electrostatic chuck or the annular insulating member, or on both the electrostatic chuck 1111 and the annular insulating member. At least one RF/DC electrode coupled to an RF source 31 and/or a DC source 32 described below may be disposed in

the ceramic member 1111a. In this case, the at least one RF/DC electrode functions as the lower electrode. If a bias RF signal and/or a DC signal described below are supplied to the at least one RF/DC electrode, the RF/DC electrode is also called a bias electrode. It is noted that the conductive member of the base 1110 and the at least one RF/DC electrode may function as a plurality of lower electrodes. The electrostatic electrode 1111b may also function as a lower electrode. The substrate support 11 accordingly includes at least one lower electrode.

[0016] The ring assembly 112 includes one or more annular members. In an embodiment, the annular members include one or more edge rings and at least one cover ring. The one or more edge rings are made of a conductive or insulating material, whereas the cover ring is made of an insulating material.

[0017] The substrate support 11 may also include a temperature adjusting module that is configured to adjust at least one of the electrostatic chuck 1111, the ring assembly 112, and the substrate to a target temperature. The temperature adjusting module may include a heater, a heat transfer medium, a flow passage 1110a, or any combination thereof. A heat transfer fluid, such as brine or gas, flows into the flow passage 1110a. In an embodiment, the flow passage 1110a is formed in the base 1110, and one or more heaters are disposed in the ceramic member 1111a of the electrostatic chuck 1111. The substrate support 11 may further include a heat transfer gas supply configured to supply a heat transfer gas to a gap between the rear surface of the substrate W and the central region 111a.

[0018] The showerhead 13 is configured to introduce at least one process gas from the gas supply 20 into the plasma processing space 10s. The showerhead 13 has at least one gas inlet 13a, at least one gas diffusing space 13b, and a plurality of gas feeding ports 13c. The process gas supplied to the gas inlet 13a passes through the gas diffusing space 13b and is then introduced into the plasma processing space 10s from the gas feeding ports 13c. The showerhead 13 further includes at least one upper electrode. The gas introduction unit may include one or more side gas injectors provided at one or more openings formed in the sidewall 10a, in addition to the showerhead 13.

[0019] The gas supply 20 may include at least one gas source 21 and at least one flow controller 22. In an embodiment, the gas supply 20 is configured to supply at least one process gas from the corresponding gas source 21 through the corresponding flow controller 22 to the showerhead 13. Each flow controller 22 may include, for example, a mass flow controller or a pressure-controlled flow controller. The gas supply 20 may include at least one flow modulation device that can modulate or pulse the flow of the at least one process gas.

[0020] The electric power source 30 includes an RF source 31 coupled to the plasma processing chamber 10 through at least one impedance matching circuit. The RF source 31 is configured to supply at least one RF signal (RF power) to at least one lower electrode and/or at least one upper electrode. A plasma is thereby formed from at least one process gas supplied into the plasma processing space 10s. Thus, the RF source 31 can function as at least part of the plasma generator 12. The bias RF signal supplied to the at least one lower electrode causes a bias potential

to occur in the substrate W, which potential then attracts ionic components in the plasma to the substrate W.

[0021] In an embodiment, the RF source 31 includes a first RF generator 31a and a second RF generator 31b. The first RF generator 31a is coupled to the at least one lower electrode and/or the at least one upper electrode through the at least one impedance matching circuit and is configured to generate a source RF signal (source RF power) for generating a plasma. In an embodiment, the source RF signal has a frequency in a range of 10 MHz to 150 MHz. In an embodiment, the first RF generator 31a may be configured to generate a plurality of source RF signals having different frequencies. The generated source RF signal(s) is supplied to the at least one lower electrode and/or the at least one upper electrode.

[0022] The second RF generator 31b is coupled to the at least one lower electrode through the at least one impedance matching circuit and is configured to generate a bias RF signal (bias RF power). The bias RF signal and the source RF signal may have the same frequency or different frequencies. In an embodiment, the bias RF signal has a frequency which is lower than that of the source RF signal. In an embodiment, the bias RF signal has a frequency in a range of 100 kHz to 60 MHz. In an embodiment, the second RF generator 31b may be configured to generate a plurality of bias RF signals having different frequencies. The generated bias RF signal(s) is supplied to the at least one lower electrode. In various embodiments, at least one of the source RF signal and the bias RF signal may be pulsed.

[0023] The electric power source 30 may also include a DC source 32

coupled to the plasma processing chamber 10. The DC source 32 includes a first DC generator 32a and a second DC generator 32b. In an embodiment, the first DC generator 32a is connected to the at least one lower electrode and is configured to generate a first DC signal. The generated first DC signal is applied to the at least one lower electrode. In an embodiment, the second DC generator 32b is connected to the at least one upper electrode and is configured to generate a second DC signal. The generated second DC signal is applied to the at least one upper electrode.

[0024] In various embodiments, the first and second DC signals may be pulsed. In this case, a sequence of voltage pulses is applied to the at least one lower electrode and/or the at least one upper electrode. The voltage pulses may have a rectangular, trapezoidal, or triangular pulse waveform, or a pulse waveform of a combination thereof. In an embodiment, a waveform generator for generating a sequence of voltage pulses from the DC signal is connected between the first DC generator 32a and the at least one lower electrode. The first DC generator 32a and the waveform generator thereby function as a voltage pulse generator. In the case that the second DC generator 32b and the waveform generator function as a voltage pulse generator, the voltage pulse generator is connected to the at least one upper electrode. The voltage pulses may have positive polarity or negative polarity. A sequence of voltage pulses may also include one or more positive voltage pulses and one or more negative voltage pulses in a cycle. The first and second DC generators 32a, 32b may be disposed in addition to the RF source 31, or the first DC generator 32a may be disposed in place of the second RF generator 31b.

[0025] The gas exhaust system 40 may be connected to, for example, a gas outlet 10e provided in the bottom of the plasma processing chamber 10. The gas exhaust system 40 may include a pressure regulation valve and a vacuum pump. The pressure regulation valve enables the pressure in the plasma processing space 10s to be adjusted. The vacuum pump may include a turbo-molecular pump, a dry pump, or a combination thereof.

[0026] Hereinafter, reference is made to FIG. 3. FIG. 3 is a diagram illustrating a plasma processing apparatus according to one example embodiment. As illustrated in FIG. 3, the plasma processing apparatus 1 includes a power supply system 30S. The power supply system 30S includes a radio frequency power supply 41, a bias supply 42, a sensor 45, a detector 51, and an A/D converter 52.

[0027] The radio frequency power supply 41 is the first RF generator 31a. The radio frequency power supply 41 is configured to generate a source RF signal, that is, source radio frequency power HF. The source radio frequency power HF has a source frequency f. That is, the source radio frequency power HF has a sinusoidal waveform of which a frequency is the source frequency f. The source frequency f may be a frequency in a range of 10 MHz to 150 MHz. The radio frequency power supply 41 is configured to be capable of adjusting the source frequency f between a minimum frequency f_{MIN} and a maximum frequency f_{MAX} thereof. In one example, the minimum frequency f_{MIN} is 36 MHz and the maximum frequency f_{MAX} is 44 MHz. The source frequency f is adjusted so as to reduce the degree of reflection of the source radio frequency power HF from a load of the radio frequency

power supply 41, as described below.

[0028] The radio frequency power supply 41 is electrically connected to a radio frequency electrode via a matcher 43 and is configured to supply the source radio frequency power HF to the radio frequency electrode. The radio frequency electrode may be disposed in the substrate support 11. The radio frequency electrode may be the conductive member of the base 1110 or at least one electrode disposed in the ceramic member 1111a. Alternatively, the radio frequency electrode may be an upper electrode. When the source radio frequency power HF is supplied to the radio frequency electrode, a plasma is generated from the gas in the chamber 10.

[0029] The matcher 43 has a variable impedance. The variable impedance of the matcher 43 is set so as to reduce the reflection of the source radio frequency power HF from the load. The matcher 43 can be controlled by, for example, the controller 2.

[0030] In one embodiment, the radio frequency power supply 41 may include a signal generator 41g, a D/A converter 41c, and an amplifier 41a. The signal generator 41g generates a radio frequency signal having the source frequency f. The signal generator 41g may be configured from a programmable processor, a programmable logic device such as an FPGA (Field-Programmable Gate Array), or a dedicated circuit such as an ASIC (Application Specific Integrated Circuit).

[0031] The output of the signal generator 41g is connected to the input of the D/A converter 41c. The D/A converter 41c converts the radio frequency signal from the signal generator 41g into an analog signal. The output of the D/A converter 41c is connected to the input of the

amplifier 41a. The amplifier 41a amplifies the analog signal from the D/A converter 41c to generate the source radio frequency power HF. The amplification factor of the amplifier 41a is specified to the radio frequency power supply 41 by the controller 2. The radio frequency power supply 41 need not include the D/A converter 41c. In this case, the output of the signal generator 41g is connected to the input of the amplifier 41a, and the amplifier 41a amplifies the radio frequency signal from the signal generator 41g to generate the source radio frequency power HF.

[0032] The bias supply 42 includes the second RF generator 31b or the first DC generator 32a. The bias supply 42 is electrically coupled to the substrate support 11. The bias supply 42 is electrically connected to a bias electrode in the substrate support 11 and is configured to supply an electrical bias EB to the bias electrode. The bias electrode may be the conductive member of the base 1110 or at least one electrode disposed in the ceramic member 1111a. The bias electrode may be common with the radio frequency electrode. When the electrical bias EB is supplied to the bias electrode, ions from the plasma are attracted to the substrate W.

[0033] Hereinafter, reference is made to FIG. 4 together with FIG. 3. FIG. 4 is a diagram illustrating an example of a waveform of an electrical bias. The bias supply 42 is configured to periodically apply an electrical bias EB having a waveform cycle CY to the bias electrode. That is, the electrical bias EB is applied to the bias electrode in each of a plurality of waveform cycles CY, which are repetitions of the waveform cycle CY. The waveform cycle CY is defined by a bias frequency. The bias frequency is, for example, a frequency of 50 kHz or more and 27

MHz or less. The time length of the waveform cycle CY is the reciprocal of the bias frequency. The bias frequency may be 13.56 MHz or less, or 400 kHz or less.

[0034] The electrical bias EB may be a bias RF signal, that is, bias radio frequency power LF having a bias frequency. That is, the electrical bias EB may have a sinusoidal waveform of which a frequency is the bias frequency. In this case, the bias supply 42 is electrically connected to the bias electrode via a matcher 44. The variable impedance of the matcher 44 is set so as to reduce reflection of the bias radio frequency power LF from the load.

[0035] Alternatively, the electrical bias EB may include a pulsed first DC signal, that is, a voltage pulse VP. The voltage pulse VP is applied to the bias electrode in the waveform cycle CY. The voltage pulse VP is periodically applied to the bias electrode at time intervals equal to the time length of the waveform cycle CY. The waveform of the voltage pulse VP may be a rectangular wave, a triangular wave, or any waveform. The polarity of the voltage of the voltage pulse VP is set so as to create a potential difference between the substrate W and the plasma and attract ions from the plasma to the substrate W. The voltage pulse VP is applied to the bias electrode such that the waveform cycle CY includes a period during which the potential of the substrate W is a negative potential. The voltage pulse VP applied to the bias electrode may have a negative potential, a positive potential, or a potential that varies between a positive potential and a negative potential. The voltage pulse VP may be a pulse of a negative voltage or a pulse of a negative DC voltage. When the electrical bias EB is the voltage pulse VP, the

plasma processing apparatus 1 need not include the matcher 44.

[0036] Hereinafter, reference is made to FIG. 5(a) and FIG. 5(b) together with FIGS. 3 and 4. Each of FIG. 5(a) and FIG. 5(b) is a timing chart of an example of source radio frequency power and an electrical bias in a plasma processing apparatus according to one example embodiment. In these figures, "ON" of the source radio frequency power HF indicates that the source radio frequency power HF is being supplied, and "OFF" of the source radio frequency power HF indicates that the supply of the source radio frequency power HF is stopped. Also, in FIG. 5(b), "HIGH" of the source radio frequency power HF indicates that the source radio frequency power HF having a power level higher than the power level indicated by "LOW" is being supplied. Also, in these figures, "ON" of the electrical bias EB indicates that the electrical bias EB is being supplied, and "OFF" of the electrical bias EB indicates that the supply of the electrical bias EB is stopped. In FIG. 5(b), "HIGH" of the electrical bias EB indicates that the electrical bias EB having a level higher than the level indicated by "LOW" is being supplied. When the electrical bias EB is the bias radio frequency power LF, the level of the electrical bias EB is the power level of the bias radio frequency power LF. When the electrical bias EB includes the voltage pulse VP, the electrical bias EB has a higher level as the energy of ions attracted to the substrate W becomes higher. When the electrical bias EB includes the voltage pulse VP, the level of the electrical bias EB may be the absolute value of the voltage level of the voltage pulse VP in the negative direction with respect to a reference voltage (for example, 0 V).

[0037] The radio frequency power supply 41 is configured to supply the

source radio frequency power HF in parallel with periodic supply of the electrical bias EB from the bias supply 42. As illustrated in FIG. 5(a), the electrical bias EB and the source radio frequency power HF may be supplied simultaneously and continuously from the start to the end of a process. That is, a continuous wave of the electrical bias EB and a continuous wave of the source radio frequency power HF may be supplied in parallel.

[0038] Alternatively, as illustrated in FIG. 5(b), pulses of the electrical bias EB and pulses of the source radio frequency power HF may be supplied in synchronization with each other. That is, in each of pulse periods PP_1, PP_2, PP_3, ... (that is, a plurality of pulse periods PP), a pulse of the electrical bias EB and a pulse of the source radio frequency power HF may be supplied simultaneously. Each of the plurality of pulse periods PP includes a plurality of waveform cycles CY. That is, in each of the plurality of pulse periods PP, the electrical bias EB is periodically supplied. The pulses of the electrical bias EB may be ON/OFF pulses that alternately take a supply state (ON state of FIG. 5(b)) and a stopped state (OFF state of FIG. 5(b)). Alternatively, the pulses of the electrical bias EB may be HIGH/LOW pulses that alternately take a high-level state (HIGH state of FIG. 5(b)) and a LOW-level state (LOW state of FIG. 5(b)). Also, the pulses of the source radio frequency power HF may be ON/OFF pulses that alternately take a supply state (ON state of FIG. 5(b)) and a stopped state (OFF state of FIG. 5(b)). Alternatively, the pulses of the source radio frequency power HF may be HIGH/LOW pulses that alternately take a high-level state (HIGH state of FIG. 5(b)) and a LOW-level state (LOW state of FIG. 5(b)). Also, the power level

of the source radio frequency power HF may be modulated during a period in which the source radio frequency power HF is ON. Also, the power level of the source radio frequency power HF may be modulated during a period in which the power level of the source radio frequency power HF is HIGH. Also, the power level of the source radio frequency power HF may be modulated during a period in which the power level of the source radio frequency power HF is LOW.

[0039] As illustrated in FIG. 3, the sensor 45 is configured to acquire a sensor signal SS reflecting a degree of reflection R_D of the source radio frequency power HF from a load. In one embodiment, the sensor 45 may include a directional coupler. In this case, the sensor signal SS is a voltage signal VS of a reflected wave of the source radio frequency power HF. The output of the sensor 45 is connected to the input of the detector 51.

[0040] The detector 51 is configured to detect an envelope signal ES of the sensor signal SS output from the sensor 45. The output of the detector 51 is connected to the input of the A/D converter 52. The A/D converter 52 is configured to perform A/D conversion on the envelope signal ES output from the detector 51.

[0041] The plasma processing apparatus 1 further includes a power supply controller. In the example illustrated in FIG. 3, the power supply controller may be the signal generator 41g. The power supply controller may be the controller 2, or may be another controller in the plasma processing apparatus 1 or the power supply system 30S.

[0042] The power supply controller adjusts the source frequency f for each of the plurality of phase periods PH so as to reduce the degree of

reflection R_D in a subsequent waveform cycle CY, in accordance with the degree of reflection R_D in the waveform cycle CY or the degree of reflection R_D in each of the plurality of phase periods PH (see FIG. 4) that divide the waveform cycle CY. The degree of reflection R_D is identified from a plurality of digital values V_D generated by the A/D converter 52 from the envelope signal ES in the waveform cycle CY. The degree of reflection R_D can be obtained in the power supply controller.

[0043] The degree of reflection R_D is a representative value of a plurality of evaluation values obtained from the plurality of digital values in the waveform cycle CY or in each phase period PH. The representative value may be an average value. For example, when a plurality of digital values V_D obtained from the envelope signal ES of the above-described voltage signal VS are used, each of the plurality of evaluation values is the power level of the reflected wave, and the average value of the power levels of the reflected wave is obtained as the degree of reflection R_D by the following equation (1).

[Math. 1]

$$R_D = \frac{1}{N_V}\sum_{j=1}^{N_V}\left(\frac{{V_{Dj}}^2}{Z_0}\right) * 10^{-\frac{C}{10}} * g \qquad \cdots (1)$$

In equation (1), V_{Dj} is the j-th digital value among the plurality of digital values V_D used in the calculation of equation (1). Also, Z_0 is a characteristic impedance, and is, for example, 50 Ω. Also, C is a coupling coefficient of the directional coupler and is predetermined. Also, g is a gain reflecting a characteristic of the detector 51 and is predetermined. NV is the number of the plurality of digital values V_D in the waveform cycle CY when the average value of the plurality of

evaluation values in the waveform cycle CY is obtained. Also, NV is the number of the plurality of digital values V_D in each phase period PH when the average value of the plurality of evaluation values in each phase period PH within the waveform cycle CY is obtained.

[0044] In the plasma processing apparatus 1, the sampling frequency of the A/D converter 52 is not less than twice the product of the bias frequency of the electrical bias EB and the number of the plurality of phase periods PH within the waveform cycle CY, and is not greater than the minimum frequency f_{MIN}. According to the A/D converter 52, two or more digital values V_D (that is, sampling values) are obtained from the envelope signal ES in each of the plurality of phase periods PH. Also, according to the plasma processing apparatus 1, the A/D converter 52 having a relatively small sampling frequency can be used. Therefore, according to the plasma processing apparatus 1, it is possible to identify, at low cost, the degree of reflection R_D in the waveform cycle CY or the degree of reflection R_D in each phase period PH, and to adjust the source frequency f for each phase period PH.

[0045] In one embodiment, the detector 51 may include an attenuator 511, a first filter 512, a detection circuit 513, a second filter 514, and an amplifier 515. The input of the attenuator 511 is connected to the sensor 45. The attenuator 511 is configured to generate a signal AS by attenuating the signal level of the sensor signal SS. The output of the attenuator 511 is connected to the input of the first filter 512.

[0046] The first filter 512 is a bandpass filter and is configured to generate a signal BPS (first signal) by performing filtering on the signal AS. The upper cutoff frequency of the first filter 512 may be greater

than or equal to the maximum frequency f_{MAX} and less than or equal to twice the minimum frequency f_{MIN}. The lower cutoff frequency of the first filter 512 may be less than or equal to the minimum frequency f_{MIN}. According to the first filter 512, harmonics having a frequency of twice or more the source frequency are substantially removed from the sensor signal SS. The output of the first filter 512 is connected to the input of the detection circuit 513. The output of the sensor 45 may be connected to the input of the first filter 512, the output of the first filter 512 may be connected to the input of the attenuator 511, and the output of the attenuator 511 may be connected to the input of the detection circuit 513.

[0047] The detection circuit 513 is configured to detect an envelope signal EAS (first envelope signal) of the signal BPS. The output of the detection circuit 513 is connected to the input of the second filter 514.

[0048] The second filter 514 is a low-pass filter and is configured to generate a signal LPS by performing filtering on the envelope signal EAS. The upper cutoff frequency of the second filter 514 has a value between the product of the bias frequency of the electrical bias EB and the number of the plurality of phase periods PH within the waveform cycle CY and the upper cutoff frequency of the first filter 512. The upper cutoff frequency of the second filter 514 may be less than or equal to the minimum frequency f_{MIN}. According to the second filter 514, high-frequency components are removed without removing the necessary signal components in each of the plurality of phase periods PH. The output of the second filter 514 is connected to the amplifier 515.

[0049] The amplifier 515 is configured to generate the above-described

envelope signal ES (that is, second envelope signal) by amplifying the signal LPS. The output of the amplifier 515 is connected to the input of the A/D converter 52. The A/D converter 52 performs A/D conversion on the envelope signal ES output from the amplifier 515. The above-described plurality of digital values V_D are thereby obtained.

[0050] Hereinafter, a control method according to one example embodiment will be described with reference to FIG. 6. FIG. 6 is a flowchart illustrating the control method according to one example embodiment. The control method illustrated in FIG. 6 (hereinafter referred to as "method MT") is performed in the plasma processing apparatus 1. In each operation of the method MT, each component of the plasma processing apparatus 1 can be controlled by the controller 2 and the power supply controller.

[0051] The method MT may include operation STp. In operation STp, the substrate W is prepared in the chamber 10. The substrate W is placed on the substrate support 11 and held by the electrostatic chuck 1111.

[0052] In operation STa, the source radio frequency power HF is supplied from the radio frequency power supply 41 to the radio frequency electrode to generate a plasma from the gas in the chamber 10. In operation STb, the electrical bias EB is supplied from the bias supply 42 to the substrate support 11 (or the bias electrode) to attract ions from the plasma to the substrate W on the substrate support 11.

[0053] In operation STc, the sensor signal SS is acquired by the sensor 45. In operation STd, the envelope signal ES is detected by the detector 51. In operation STe, A/D conversion is performed on the envelope signal ES by the A/D converter 52. In operation STf, the degree of

reflection R_D in the waveform cycle CY or the degree of reflection R_D in each phase period PH is identified from the plurality of digital values V_D generated by the A/D converter 52 from the envelope signal ES in the waveform cycle CY.

[0054] In operation STJ, it is determined whether a stop condition is satisfied. The determination in operation STJ can be performed by the power supply controller. In operation STJ, the stop condition is satisfied, for example, when a termination instruction has been issued from the controller 2. When it is determined in operation STJ that the stop condition is not satisfied, operation STg is performed. In operation STg, the source frequency f for each of the plurality of phase periods PH is adjusted by the power supply controller so as to reduce the degree of reflection in a subsequent waveform cycle CY, in accordance with the degree of reflection R_D identified in operation STf. After operation STg, processing from operation STa is performed again. In operation STa, the source radio frequency power HF having the source frequency f determined in operation STg for each of the plurality of phase periods PH is supplied. On the other hand, when it is determined in operation STJ that the stop condition is satisfied, the method MT ends.

[0055] Hereinafter, several embodiments related to the adjustment of the source frequency f in the method MT will be described. Also, the adjustment of the source frequency f by the power supply controller will be described together.

[0056] In one embodiment, the power supply controller performs the adjustment of the source frequency f by a feedback process. The feedback process is applied to a plurality of designated phase periods DP

within the waveform cycle CY.

[0057] In a feedback process according to a first embodiment, the plurality of designated phase periods DP within the waveform cycle CY may be all of the phase periods PH within the waveform cycle CY. That is, in the feedback process according to the first embodiment, the number of the plurality of designated phase periods DP within the waveform cycle CY is M, and M is N, which is the number of the plurality of phase periods PH within the waveform cycle CY.

[0058] In a feedback process according to a second embodiment, the plurality of designated phase periods DP within the waveform cycle CY may be some selected phase periods PH that are a subset of all the phase periods PH within the waveform cycle CY. That is, in the feedback process according to the second embodiment, the number of the plurality of designated phase periods DP within the waveform cycle CY is M, and M is less than N, which is the number of the plurality of phase periods PH within the waveform cycle CY. In the feedback process according to the second embodiment, the power supply controller determines the source frequency f for each of the phase periods other than the plurality of designated phase periods DP among the plurality of phase periods PH within the waveform cycle CY by interpolation using the source frequency f for the plurality of designated phase periods DP. The interpolation may be linear interpolation using the source frequency f for each of two adjacent designated phase periods DP. The interpolation may be interpolation by another method.

[0059] In the feedback process, the power supply controller determines the source frequency f[i, m] for the m-th designated phase period DP_m

within the i-th waveform cycle CY_i in a series CYS of waveform cycles CY, from the change in the source frequency of the m-th designated phase period DP_m within several preceding waveform cycles CY in the series CYS and the degree of reflection of the source radio frequency power, so as to suppress the degree of reflection. The waveform cycles CY preceding the waveform cycle CY_i in the series CYS may include waveform cycles CY_{i-Ifb} and $CY_{i-2\times Ifb}$. Here, "Ifb" is an integer of 1 or more.

[0060] The feedback process includes a first feedback process and/or a second feedback process. The first feedback process is applied when the source radio frequency power HF and the electrical bias EB are supplied simultaneously and continuously as illustrated in FIG. 5(a). In the first feedback process, the series CYS includes a plurality of waveform cycles CY that repeat continuously.

[0061] The second feedback process is applied when pulses of the source radio frequency power HF and pulses of the electrical bias EB synchronized with each other are supplied as illustrated in FIG. 5(b). In the second feedback process, the series CYS is composed of waveform cycles CY of the same order in each of the plurality of pulse periods PP, that is, the k-th waveform cycle CY_k in each of the plurality of pulse periods PP.

[0062] In the case of the example illustrated in FIG. 5(b), the second feedback process may be applied to all waveform cycles CY in each of the plurality of pulse periods PP. Alternatively, the second feedback process may be applied to each of the 1st through K_1-th waveform cycles CY within each of the plurality of pulse periods PP, and the first

feedback process may be applied to each of the (K_1+1)-th through last waveform cycles CY within each of the plurality of pulse periods PP. Here, K_1 is an integer of 1 or more. Alternatively, the second feedback process may be applied to each of the 1st through K_1-th waveform cycles CY within each of the plurality of pulse periods PP, and in each of the (K_1+1)-th through last waveform cycles CY within each of the plurality of pulse periods PP, the source frequency of each designated phase period of the K_1-th waveform cycle CY may be used for the same designated phase period.

[0063] Hereinafter, an example of the feedback process applied to each series CYS will be described with reference to FIGS. 7 and 8. FIG. 7 is a flowchart illustrating an example of the feedback process. FIG. 8 is a flowchart illustrating an example of processing in operation ST9 illustrated in FIG. 7. The example of the feedback process described below is an example in which the above-described "Ifb" is 1. However, as described above, "Ifb" may be an integer greater than 1.

[0064] As illustrated in FIG. 7, the feedback process may include operations ST1 through ST9. Operations ST1 through ST9 are performed for the plurality of designated phase periods DP within each waveform cycle CY in the series CYS.

[0065] In operation ST1, the power supply controller sets i to 1. "i" represents the order of the waveform cycle CY within the series CYS.

[0066] In subsequent operation ST2, the source frequency f and a shift value Δf for each of the plurality of designated phase periods DP of the i-th waveform cycle CY in the series CYS are set. Specifically, in operation ST2, the power supply controller sets the source frequency f[i,

m] and the shift value $\Delta f[i, m]$. In operation ST2, the source frequency $f[i, m]$ and the shift value $\Delta f[i, m]$, that is, the source frequency $f[1, m]$ and the shift value $\Delta f[1, m]$, are set to respective pre-set values. In the case of the feedback process according to the second embodiment, in operation ST2, the source frequency f for phase periods other than the plurality of designated phase periods DP is set by interpolation as described above.

[0067] Subsequent operation ST3 corresponds to operation STa of the method MT. In operation ST3, the power supply controller supplies the source radio frequency power HF having the source frequency f set in operation ST2 for each of the plurality of phase periods PH within the waveform cycle CY from the radio frequency power supply 41. That is, in operation ST3, the power supply controller supplies the source radio frequency power HF having the source frequency $f[i, m]$ in the designated phase period DP_m within the waveform cycle CY_i in the series CYS from the radio frequency power supply 41. Also, the electrical bias is supplied in operation STb described above, and the degree of reflection R_D is obtained in operations STc through STf described above.

[0068] Operations ST4, ST5, and ST6 correspond to operation STg of the method MT. The processing including operations ST4, ST5, and ST6 is performed for each of the plurality of designated phase periods DP within the i-th waveform cycle CY in the series CYS.

[0069] In operation ST4, the power supply controller determines whether the degree of reflection R_D of the source radio frequency power HF in the designated phase period DP_m within the waveform cycle CY_i

in the series CYS, that is, the degree of reflection $R_D[i, m]$, is large enough to satisfy a frequency change condition. In operation ST4, the frequency change condition is satisfied when the degree of reflection $R_D[i, m]$ of the source radio frequency power HF in the designated phase period DP_m within the waveform cycle CY_i in the series CYS is greater than a threshold value. In operation ST4, the frequency change condition may be satisfied when $R_D[i, m]$ is greater than a first threshold value $R_{th1}[m]$. The first threshold values R_{th1} for each of the plurality of designated phase periods DP may be the same as each other or may be different from each other.

[0070] When it is determined in operation ST4 that the frequency change condition is satisfied, the power supply controller sets the source frequency $f[i+1, m]$ for the designated phase period DP_m within the subsequent waveform cycle CY_{i+1} in the series CYS in operation ST5 by the following equation.

$$f[i+1, m] = f[i, m] + \Delta f[i, m]$$

[0071] On the other hand, when it is determined in operation ST4 that the frequency change condition is not satisfied, the power supply controller sets the source frequency $f[i+1, m]$ in operation ST6 by the following equation.

$$f[i+1, m] = f[i, m]$$

[0072] In the case of the feedback process according to the second embodiment, before the processing proceeds to the next operation ST7, the source frequency f for phase periods other than the plurality of designated phase periods DP is set by interpolation as described above.

[0073] Next, operations ST7 through ST9 are performed. Operations

ST7 through ST9 are repeated until it is determined in operation STJ of the method MT that the stop condition is satisfied. In operation ST7, the power supply controller increments i by 1.

[0074] Operations ST8 through ST9 are performed for each of the plurality of designated phase periods DP of the i-th waveform cycle CY in the series CYS. Operation ST8 corresponds to operation STa of the method MT. In operation ST8, the power supply controller supplies the source radio frequency power HF having the source frequency f set immediately before for each of the plurality of phase periods PH within the waveform cycle CY from the radio frequency power supply 41. That is, in operation ST8, the power supply controller supplies the source radio frequency power HF having the source frequency f[i, m] in the designated phase period DP_m within the waveform cycle CY_i in the series CYS from the radio frequency power supply 41. Also, the electrical bias is supplied in operation STb described above, and the degree of reflection R_D is obtained in operations STc through STf described above.

[0075] In subsequent operation ST9, the power supply controller determines the source frequency f[i+1, m] for the designated phase period DP_m within the subsequent waveform cycle CY_{i+1} in the series CYS in accordance with the degree of reflection $R_D[i, m]$.

[0076] As illustrated in FIG. 8, operation ST9 starts with operation ST901. In operation ST901, the power supply controller determines whether the degree of reflection $R_D[i, m]$ is in an increasing trend. In operation ST901, the degree of reflection $R_D[i, m]$ may be determined to be in an increasing trend when $R_D[i, m] > R_D[i-1, m]$ is satisfied.

Alternatively, the degree of reflection $R_D[i, m]$ may be determined to be in an increasing trend when the degree of reflection in the m-th designated phase period DP_m has been in an increasing trend over two or more waveform cycles CY up to the i-th waveform cycle CY_i in the series CYS.

[0077] When it is determined in operation ST901 that the degree of reflection $R_D[i, m]$ is not in an increasing trend, the power supply controller maintains the sign of the shift value $\Delta f[i, m]$ in operation ST902. That is, the power supply controller sets the shift value $\Delta f[i, m]$ in operation ST902 by the following equation.

$$\Delta f[i, m] = \Delta f[i-1, m]$$

[0078] On the other hand, when it is determined in operation ST901 that the degree of reflection $R_D[i, m]$ is in an increasing trend, the power supply controller changes the sign of the shift value $\Delta f[i, m]$ in operation ST903. That is, the power supply controller sets the shift value $\Delta f[i, m]$ in operation ST903 by the following equation.

$$\Delta f[i, m] = -\Delta f[i-1, m]$$

[0079] In subsequent operation ST904, the power supply controller determines whether the degree of reflection $R_D[i, m]$ of the source radio frequency power HF in the designated phase period DP_m within the waveform cycle CY_i in the series CYS is large enough to satisfy the frequency change condition. In operation ST904, the frequency change condition is satisfied when the degree of reflection $R_D[i, m]$ of the source radio frequency power HF in the designated phase period DP_m within the waveform cycle CY_i in the series CYS is greater than a threshold value.

[0080] In one embodiment, when it is determined as a result of a

comparison between the degree of reflection at the designated phase period DP_m in any waveform cycle within the series CYS and the first threshold value $R_{th1}[m]$ that the degree of reflection is small, the frequency change condition need not be satisfied in operation ST904 until it is determined in subsequent operation ST904 as a result of a comparison between the degree of reflection at the designated phase period DP_m and a second threshold value $R_{th2}[m]$ that the degree of reflection is large. The second threshold value $R_{th2}[m]$ is greater than or equal to the first threshold value $R_{th1}[m]$. The second threshold value $R_{th2}[m]$ may be greater than the first threshold value $R_{th1}[m]$. The second threshold values $R_{th2}[m]$ for each of the plurality of designated phase periods DP may be the same as each other or may be different from each other.

[0081] Specifically, when it is determined that the degree of reflection at the designated phase period DP_m in any waveform cycle within the series CYS is less than or equal to the first threshold value $R_{th1}[m]$, the second threshold value $R_{th2}[m]$ may be used as the threshold value to be compared with the degree of reflection at the designated phase period DP_m in subsequent operation ST904. Then, when it is determined that the degree of reflection at the designated phase period DP_m in any waveform cycle within the series CYS is greater than the second threshold value $R_{th2}[m]$, the first threshold value $R_{th1}[m]$ may be used as the threshold value to be compared with the degree of reflection at the designated phase period DP_m in subsequent operation ST904.

[0082] When it is determined in operation ST904 that the frequency change condition is satisfied, the power supply controller sets the source

frequency f[i+1, m] for the designated phase period DP_m within the subsequent waveform cycle CY_{i+1} in the series CYS in operation ST905 by the following equation.

$$f[i+1, m] = f[i, m] + \Delta f[i, m]$$

[0083] On the other hand, when the frequency change condition is not satisfied in operation ST904, the power supply controller sets the source frequency f[i+1, m] in operation ST906 by the following equation.

$$f[i+1, m] = f[i, m]$$

[0084] In the case of the feedback process according to the second embodiment, before the processing proceeds to the next operation, the source frequency f for phase periods other than the plurality of designated phase periods DP is set by interpolation as described above.

[0085] According to the feedback process, by adjusting the source frequency f[i+1, m] in accordance with the degree of reflection $R_D[i, m]$, reflection of the source radio frequency power HF is suppressed. Also, as described above, by using the first threshold value R_{th1} and the second threshold value R_{th2} in the determination of the frequency change condition, excessive changes in the source frequency are suppressed. Furthermore, when the method MT is repeated, high reproducibility of the temporal change in the source frequency can be achieved. Also, according to the feedback process of the second embodiment, the source frequency for each of the phase periods other than the plurality of designated phase periods DP among the plurality of phase periods PH is determined by interpolation based on the source frequency for the plurality of designated phase periods DP. Therefore, according to the feedback process of the second embodiment, large fluctuations in the

source frequency within the waveform cycle CY are suppressed.

[0086] Hereinafter, another example of the feedback process will be described with reference to FIGS. 9 and 10. FIG. 9 is a flowchart illustrating another example of the feedback process. FIG. 10 is a flowchart illustrating an example of processing in operation ST9a illustrated in FIG. 9. Hereinafter, the feedback process illustrated in FIGS. 9 and 10 will be described from the perspective of differences from the feedback process illustrated in FIGS. 7 and 8. In the processing illustrated in FIGS. 9 and 10, the power supply controller sets the shift value $\Delta f[i, m]$ to a value corresponding to the magnitude of the degree of reflection $R_D[i, m]$.

[0087] Specifically, as illustrated in FIG. 9, the power supply controller sets the source frequency $f[i, m]$ and a coefficient $\alpha[i, m]$ in operation ST2a between operation ST1 and operation ST3. In operation ST2a, the source frequency $f[i, m]$ and the coefficient $\alpha[i, m]$, that is, the source frequency $f[1, m]$ and the coefficient $\alpha[1, m]$, are set to respective pre-set values.

[0088] When it is determined in operation ST4 that the frequency change condition is satisfied, the power supply controller sets the shift value $\Delta f[i, m]$ in operation ST5a between operation ST4 and operation ST5 by the following equation.

$$\Delta f[i, m] = \alpha[i, m] * (R_D[i, m] - R_{th1}[m])$$

[0089] Then, in operation ST9a subsequent to operation ST8, the power supply controller determines the source frequency $f[i+1, m]$ for the designated phase period DP_m within the subsequent waveform cycle CY_{i+1} in the series CYS in accordance with the degree of reflection $R_D[i,$

m].

[0090] As illustrated in FIG. 10, operation ST9a starts with operation ST901. When it is determined in operation ST901 that the degree of reflection $R_D[i, m]$ is not in an increasing trend, the power supply controller maintains the sign of the coefficient $\alpha[i, m]$ in operation ST902a. That is, the power supply controller sets the coefficient $\alpha[i, m]$ in operation ST902a by the following equation.

$$\alpha[i, m] = \alpha[i-1, m]$$

[0091] On the other hand, when it is determined in operation ST901 that the degree of reflection $R_D[i, m]$ is in an increasing trend, the power supply controller changes the sign of the coefficient $\alpha[i, m]$ in operation ST903a. That is, the power supply controller sets the coefficient $\alpha[i, m]$ in operation ST903a by the following equation.

$$\alpha[i, m] = -\alpha[i-1, m]$$

[0092] As illustrated in FIG. 10, when it is determined in operation ST904 that the frequency change condition is satisfied, the power supply controller sets the shift value $\Delta f[i, m]$ in operation ST905a between operation ST904 and operation ST905 by the following equation.

$$\Delta f[i, m] = \alpha[i, m] * (R_D[i, m] - R_{th1}[m])$$

[0093] Hereinafter, reference is made to FIG. 11. FIG. 11 is a timing chart of an example of source radio frequency power and an electrical bias in a plasma processing apparatus according to one example embodiment. FIG. 11 illustrates an example in which pulses of the electrical bias EB and pulses of the source radio frequency power HF are supplied in synchronization with each other, similarly to FIG. 5(b). In FIG. 11, among all pulse periods, the pulse period PP_k is illustrated. As

illustrated in FIG. 11, each pulse period PP may include a first feedback period $P_F[1]$ and a second feedback period $P_F[2]$. The first feedback period $P_F[1]$ is a period from the start point of the pulse period PP to a point between the start point and the end point of the pulse period PP. The second feedback period $P_F[2]$ is a period that follows the first feedback period $P_F[1]$ and continues until the end point of the pulse period PP. Each of the first feedback period $P_F[1]$ and the second feedback period $P_F[2]$ may include a plurality of waveform cycles CY.

[0094] The power supply controller may perform the above-described second feedback process to determine the source frequency f for each of the plurality of designated phase periods DP within each of the plurality of waveform cycles CY in the first feedback period $P_F[1]$.

[0095] In the case of the feedback process according to the second embodiment, the power supply controller may set the source frequency f for each phase period between the last designated phase period within the j-th waveform cycle CY in the first feedback period $P_F[1]$ and the first designated phase period DP_1 within the (j+1)-th waveform cycle CY in the first feedback period $P_F[1]$ to a value obtained by interpolation (for example, linear interpolation) using the source frequency f for the last designated phase period and the source frequency f for the first designated phase period DP_1. In the case of the feedback process according to the second embodiment, the number of designated phase periods in each of the plurality of waveform cycles CY in the first feedback period $P_F[1]$ may be different. Also, in the case of the feedback process according to the second embodiment, in each of the plurality of waveform cycles CY in the first feedback period $P_F[1]$, the temporal

positions of the plurality of designated phase periods may be different.

[0096] Also, as described above, during the period between a period in which a pulse of the source radio frequency power HF is supplied and a period in which the next pulse of the source radio frequency power HF is supplied, the source radio frequency power HF having a power level lower than the power level of the pulse may be supplied. Hereinafter, the period during which the source radio frequency power HF having a power level lower than the power level of the pulse of the source radio frequency power HF is supplied is referred to as a LOW period. The source frequency f used in the LOW period may be constant or may be predetermined.

[0097] In the case of the feedback process according to the second embodiment, the first phase period PH_1 within the first waveform cycle CY in the first feedback period $P_F[1]$ may be the first designated phase period DP_1 among the plurality of designated phase periods DP. Alternatively, in the case of the feedback process according to the second embodiment, the first phase period PH_1 within the first waveform cycle CY in the first feedback period $P_F[1]$ may not be the first designated phase period DP_1 among the plurality of designated phase periods DP. In the latter case, the power supply controller may set the source frequency f for each phase period between the last time point in the LOW period and the first designated phase period DP_1 in the first feedback period $P_F[1]$ to a value obtained by interpolation (for example, linear interpolation) using the source frequency f in the LOW period and the source frequency f for the first designated phase period DP_1 in the first feedback period $P_F[1]$.

[0098] Also, the power supply controller may perform the above-described first feedback process to determine the source frequency f for each of the plurality of designated phase periods DP within each of the plurality of waveform cycles CY in the second feedback period $P_F[2]$. Also, in the case of the feedback process according to the second embodiment, the power supply controller may determine the source frequency f for each phase period other than the plurality of designated phase periods DP within each of the plurality of waveform cycles CY in the second feedback period $P_F[2]$ by interpolation using the source frequency f for the plurality of designated phase periods DP. Alternatively, the power supply controller may use, as the source frequency for each of the plurality of phase periods PH within each of the plurality of waveform cycles CY in the second feedback period $P_F[2]$, the source frequency for each of the plurality of phase periods PH within the last waveform cycle CY in the immediately preceding first feedback period $P_F[1]$.

[0099] Hereinafter, the plurality of designated phase periods DP within the waveform cycle CY in the feedback process according to the second embodiment will be described with reference to FIGS. 12 and 13. Each of FIGS. 12 and 13 is a timing chart related to a power supply system according to one example embodiment. As illustrated in FIG. 12, the number M of the plurality of designated phase periods DP within the waveform cycle CY is less than N, which is the number of the plurality of phase periods PH within the waveform cycle CY. The number M of the plurality of designated phase periods DP within the waveform cycle CY is 11 in the example of FIG. 12, but the number M is not limited to

11.

[0100] The intervals between the plurality of designated phase periods DP within the waveform cycle CY may be set such that the intervals in a section within the waveform cycle CY where the change in the potential of the substrate W is large are smaller than the intervals in a section within the waveform cycle CY where the change in the potential of the substrate W is small.

[0101] The phase of each of the plurality of designated phase periods DP in the waveform cycle CY may be predetermined. As illustrated in FIG. 13, when the electrical bias EB includes the voltage pulse VP, the waveform cycle CY may include a first period P_1, a second period P_2, and a third period P_3. The voltage pulse VP is in an OFF state in the first period P_1. The second period P_2 follows the first period P_1. The voltage pulse VP is in an ON state in the second period P_2. The third period P_3 follows the second period P_2. The voltage pulse VP is in an OFF state in the third period P_3.

[0102] In one embodiment, the plurality of designated phase periods DP may be predetermined such that the intervals thereof in the second period P_2 are smaller than the intervals thereof in each of the first period P_1 and the third period P_3. In this case, in the second period P_2 during which the potential of the substrate changes significantly, the source frequency f can be adjusted so as to more effectively suppress reflection of the source radio frequency power HF.

[0103] In one embodiment, the intervals of the plurality of designated phase periods DP in the third period P_3 may be the same as the intervals of the plurality of designated phase periods DP in the first period P_1, or

may be smaller than the intervals of the plurality of designated phase periods DP in the first period P_1. When the intervals of the plurality of designated phase periods DP in the third period P_3 are smaller than the intervals of the plurality of designated phase periods DP in the first period P_1, the source frequency f can be adjusted so as to more effectively suppress reflection of the source radio frequency power HF immediately after the voltage pulse VP switches from the ON state to the OFF state.

[0104] In one embodiment, the second period P_2 may include a first sub-period SP_1, a second sub-period SP_2, and a third sub-period SP_3. The first sub-period SP_1 is a period immediately after the first period P_1. In the first sub-period SP_1, the voltage level of the voltage pulse VP changes in the negative direction from a reference voltage level thereof (for example, 0 V) to a set voltage level. The second sub-period SP_2 follows the first sub-period SP_1. In the second sub-period SP_2, the voltage level of the voltage pulse VP is the set voltage level. The third sub-period SP_3 follows the second sub-period SP_2. In the third sub-period SP_3, the voltage level of the voltage pulse VP changes from the set voltage level to the reference voltage level. The intervals of the plurality of designated phase periods DP in each of the first sub-period SP_1, the second sub-period SP_2, and the third sub-period SP_3 may be the same as each other or may be different from each other.

[0105] In one embodiment, the plurality of designated phase periods DP may be determined in advance from the source frequency f for each of the plurality of phase periods PH within the waveform cycle CY obtained by performing the above-described feedback process for each

phase period PH in the series CYS of waveform cycles CY. Specifically, the plurality of designated phase periods DP may be selected in advance from the plurality of phase periods PH so as to exclude a phase period PH_n when the absolute value of the difference between the source frequency f[n] of the n-th phase period PH_n within the waveform cycle CY and the source frequency f[n-u] of the (n-u)-th phase period PH_{n-u} within the waveform cycle CY and the absolute value of the difference between the source frequency f[n] and the source frequency f[n+u] of the (n+u)-th phase period PH_{n+u} within the waveform cycle CY are each greater than a predetermined value, and both the source frequency f[n-u] and the source frequency f[n+u] are greater than or less than the source frequency f[n].

[0106] Also, the plurality of designated phase periods DP may be determined by calculation by the power supply controller. In one embodiment, the power supply controller acquires, in a preparation period, a series of source frequencies f for the plurality of phase periods PH within the waveform cycle CY obtained by performing the above-described feedback process for each phase period PH in the series CYS of waveform cycles CY. The power supply controller determines the plurality of designated phase periods DP such that the larger the change in the source frequency f in sections in the series of source frequencies f obtained by smoothing the series of source frequencies f, the smaller the intervals of the plurality of designated phase periods DP.

[0107] In one embodiment, the power supply controller may acquire a voltage waveform of the electrical bias EB. In this embodiment, the power supply controller may identify the above-described first period

P_1, second period P_2, and third period P_3 from the acquired voltage waveform, and set the intervals of the plurality of designated phase periods DP in each of the first period P_1, the second period P_2, and the third period P_3 as described above.

[0108] Hereinafter, several embodiments in which the adjustment of the source frequency f by the power supply controller in the method MT is performed by a shift and/or scaling process (hereinafter referred to as "SS process") will be described.

[0109] In the SS process as well, when the source radio frequency power HF and the electrical bias EB are supplied simultaneously and continuously as illustrated in FIG. 5(a), the series CYS includes a plurality of waveform cycles CY that repeat continuously. Also, in the SS process as well, when pulses of the source radio frequency power HF and pulses of the electrical bias EB synchronized with each other are supplied as illustrated in FIG. 5(b), the series CYS includes waveform cycles CY of the same order in each of the plurality of pulse periods PP. Alternatively, in the SS process, for each of the 1st through K_1-th waveform cycles CY within each of the plurality of pulse periods PP, waveform cycles CY of the same order in each of the plurality of pulse periods PP may form the series CYS, and the (K_1+1)-th through last waveform cycles CY within each of the plurality of pulse periods PP may form the series CYS. Alternatively, in the SS process, for each of the 1st through K_1-th waveform cycles CY within each of the plurality of pulse periods PP, waveform cycles CY of the same order in each of the plurality of pulse periods PP may form the series CYS, and in each of the (K_1+1)-th through last waveform cycles CY within each of the plurality

of pulse periods PP, the source frequency for each phase period of the K_1-th waveform cycle CY may be used for the same phase period. Hereinafter, the SS process applied to each series CYS will be described.

[0110] Initially in the method MT including the SS process, the power supply controller supplies the source radio frequency power HF from the radio frequency power supply 41 in operation STa using a basic time series TS_B, which is a predetermined time series of frequencies, as the time series of the source frequency f within the waveform cycle CY. The time series of the source frequency f includes a plurality of frequencies, and the plurality of frequencies are used as the frequencies of the source radio frequency power HF for the plurality of phase periods PH within the waveform cycle CY, respectively. The basic time series TS_B is prepared in advance. The basic time series TS_B may be determined by performing the above-described first feedback process or second feedback process in advance.

[0111] Also, through operations STb through STf, the degree of reflection R_D in the waveform cycle CY is obtained. In the SS process, the degree of reflection R_D is a representative value, for example an average value, of a plurality of evaluation values obtained from the plurality of digital values V_D in the waveform cycle CY.

[0112] Next, in operation STg, the power supply controller adjusts the time series of the source frequency f to create a modified time series TS_M of the source frequency f. Then, in operation STa, the power supply controller supplies the source radio frequency power HF having the plurality of frequencies of the time series TS_M as the source frequencies f respectively for the plurality of phase periods PH within the subsequent

waveform cycle CY in the series CYS from the radio frequency power supply 41. Then, operations STb through STg are performed again. In the method MT including the SS process, operations STa through STg are repeated so as to reduce the degree of reflection R_D in the waveform cycle CY in the series CYS.

[0113] In operation STg, a time series TS1, a time series TS2, or a time series TS3 is used as the time series TS_M. The time series TS1 is a time series of frequencies obtained by applying a phase shift amount to the basic time series TS_B with respect to the waveform cycle CY. The time series TS2 is a time series of frequencies obtained by scaling (that is, expanding or compressing) the basic time series TS_B in the frequency direction. The time series TS3 is a time series of frequencies including the same number of frequencies as the basic time series TS_B. The time series TS3 is a time series of frequencies obtained by scaling (expanding or compressing) two or more of the plurality of time zones of the basic time series TS_B in the time direction.

[0114] Hereinafter, several examples of the method MT including the SS process will be described.

[0115] [First Example]

[0116] Referring to FIGS. 14 and 15, a first example of the method MT including the SS process, that is, a control method of the first example (hereinafter referred to as "method MTA"), will be described. FIG. 14 is a flowchart illustrating the control method of the first example. FIG. 15 is a diagram for explaining the control method of the first example illustrated in FIG. 14. In FIG. 15, the horizontal axis represents time, and the vertical axis represents the electrical bias EB and the source

frequency f. FIG. 15 illustrates an example of a waveform of the electrical bias EB in the waveform cycle CY. FIG. 15 also illustrates the basic time series TS_B and the modified time series TS_M used as the source frequency f for each of the plurality of phase periods PH within the waveform cycle CY. In the method MTA, the above-described time series TS1 is used as the modified time series TS_M.

[0117] The method MTA is applied to each series CYS. As illustrated in FIG. 14, the method MTA starts with operation STAa1. Operation STAa1 corresponds to operation STa. In operation STAa1, the power supply controller supplies the source radio frequency power HF having the plurality of frequencies of the basic time series TS_B as the source frequencies f respectively for the plurality of phase periods PH within the waveform cycle CY from the radio frequency power supply 41. As described above with respect to the method MT, operation STb may also be performed in the method MTA.

[0118] Next, operation STAf1 is performed. Operation STAf1 corresponds to operations STc through STf. In operation STAf1, the degree of reflection R_D in the waveform cycle CY is obtained.

[0119] Next, operation STAg1 is performed. Operation STAg1 corresponds to operation STg. In operation STAg1, the power supply controller prepares the time series TS_M obtained by applying a phase shift amount to the basic time series TS_B relative to the waveform cycle CY.

[0120] Next, operation STAa2 is performed. Operation STAa2 corresponds to operation STa. In operation STAa2, the power supply controller supplies the source radio frequency power HF having the

plurality of frequencies of the time series TS_M as the source frequencies f respectively for the plurality of phase periods PH within the waveform cycle CY from the radio frequency power supply 41.

[0121] Next, operation STAf2 is performed. In operation STAf2, the degree of reflection R_D in the waveform cycle CY is obtained, similarly to operation STAf1.

[0122] Next, operation STAJ1 is performed. Operation STAJ1 corresponds to operation STJ. The determination in operation STAJ1 can be performed by the power supply controller. When it is determined in operation STAJ1 that the stop condition is not satisfied, operation STAJ2 is performed.

[0123] In operation STAJ2, it is determined whether the degree of reflection R_D obtained in operation STAf2 is less than or equal to a specified value. The determination in operation STAJ2 can be performed by the power supply controller. The degree of reflection R_D being less than or equal to the specified value indicates that the matching state is good. When it is determined in operation STAJ2 that the degree of reflection R_D is less than or equal to the specified value, the processing from operation STAa2 is repeated. On the other hand, when it is determined in operation STAJ2 that the degree of reflection R_D is greater than the specified value, operation STAJ3 is performed.

[0124] In operation STAJ3, the degree of reflection R_D in the waveform cycle CY obtained in operation STAf2 and the degree of reflection R_D obtained immediately before in the processing for the series CYS are compared with each other, and it is determined whether the degree of reflection R_D has improved, that is, whether the degree of reflection R_D

has been reduced. The determination in operation STAJ3 is performed by the power supply controller. When it is determined in operation STAJ3 that the degree of reflection R_D has improved, operation STAg2 is performed. On the other hand, when it is determined in operation STAJ3 that the degree of reflection R_D has not improved, operation STAg3 is performed.

[0125] Operation STAg2 corresponds to operation STg. Operation STAg2 can be performed by the power supply controller. In operation STAg2, the phase shift amount is changed in the same direction as the phase shift amount used immediately before in the processing for the series CYS. When the phase shift amount used immediately before in the processing for the series CYS has increased relative to the phase shift amount used prior to that, in operation STAg2, the phase shift amount is increased, as indicated by the rightward arrow in FIG. 15. When the phase shift amount used immediately before in the processing for the series CYS has decreased relative to the phase shift amount used prior to that, in operation STAg2, the phase shift amount is decreased. Then, the time series TS_M obtained by applying the changed phase shift amount to the basic time series TS_B is prepared. Then, operation STAa2 is performed again using the time series TS_M prepared in operation STAg2.

[0126] Operation STAg3 corresponds to operation STg. Operation STAg3 can be performed by the power supply controller. In operation STAg3, the phase shift amount is changed in the opposite direction to the phase shift amount used immediately before in the processing for the series CYS. When the phase shift amount used immediately before has increased relative to the phase shift amount used before that, in operation

STAg3, the phase shift amount is decreased, as indicated by the leftward arrow in FIG. 15. When the phase shift amount used immediately before in the processing for the series CYS has decreased relative to the phase shift amount used before that, in operation STAg3, the phase shift amount is increased. Then, the time series TS_M obtained by applying the changed phase shift amount to the basic time series TS_B is prepared. Then, operation STAa2 is performed again. That is, operation STAa2 is performed again using the time series TS_M prepared in operation STAg3.

[0127] The method MTA ends when it is determined in operation STJ1 that the stop condition is satisfied.

[0128] [Second Example]

[0129] Hereinafter, a second example of the method MT including the SS process, that is, a control method of the second example (hereinafter referred to as "method MTB"), will be described with reference to FIGS. 16 through 20. FIG. 16 is a flowchart illustrating the control method of the second example. Each of FIGS. 17 through 20 is a diagram for explaining the control method of the second example illustrated in FIG. 16. In each of FIGS. 17 through 20, the horizontal axis represents time, and the vertical axis represents the electrical bias EB and the source frequency f. Each of FIGS. 17 through 20 illustrates an example of a waveform of the electrical bias EB in the waveform cycle CY. Each of FIGS. 17 through 20 also illustrates the basic time series TS_B and the modified time series TS_M used as the source frequency f for each of the plurality of phase periods PH within the waveform cycle CY. In the method MTB, the above-described time series TS2 is used as the modified time series TS_M.

[0130] The method MTB is applied to each series CYS. As illustrated in FIG. 16, the method MTB starts with operation STBa1. Operation STBa1 is the same operation as operation STAa1. Next, operation STBf1 is performed. Operation STBf1 is the same operation as operation STAf1.

[0131] Next, operation STBg1 is performed. Operation STBg1 corresponds to operation STg. In operation STBg1, the power supply controller prepares the time series TS_M obtained by scaling, that is, expanding or compressing, the basic time series TS_B in the frequency direction.

[0132] The time series TS_M prepared in operation STBg1 may be a time series obtained by scaling the basic time series TS_B in the frequency direction while maintaining the minimum frequency f_{min} in the basic time series TS_B, as illustrated in FIG. 17. Hereinafter, the time series modified as illustrated in FIG. 17 is referred to as time series TS21. The time series TS_M prepared in operation STBg1 may be a time series obtained by scaling the basic time series TS_B in the frequency direction while maintaining the maximum frequency f_{max} in the basic time series TS_B, as illustrated in FIG. 18. Hereinafter, the time series modified as illustrated in FIG. 18 is referred to as time series TS22. The time series TS_M prepared in operation STBg1 may be a time series obtained by scaling the basic time series TS_B in the frequency direction while maintaining frequencies equal to or lower than a specified frequency f_{sp} in the basic time series TS_B, as illustrated in FIG. 19. Hereinafter, the time series modified as illustrated in FIG. 19 is referred to as time series TS23. The time series TS_M prepared in operation STBg1 may be a time

series obtained by scaling the basic time series TS_B in the frequency direction while maintaining frequencies equal to or higher than the specified frequency f_{sp} in the basic time series TS_B, as illustrated in FIG. 20. Hereinafter, the time series modified as illustrated in FIG. 20 is referred to as time series TS24. In operation STBg1, any one of the time series TS21 through TS24 is prepared as the time series TS_M.

[0133] Next, operation STBa2 is performed. Operation STBa2 corresponds to operation STa. In operation STBa2, the power supply controller supplies the source radio frequency power HF having the plurality of frequencies of the time series TS_M as the source frequencies f respectively for the plurality of phase periods PH within the waveform cycle CY from the radio frequency power supply 41.

[0134] Next, operation STBf2 is performed. In operation STBf2, the degree of reflection R_D in the waveform cycle CY is obtained, similarly to operation STBf1.

[0135] Next, operation STBJ is performed. The determination in operation STBJ can be performed by the power supply controller. In operation STBJ, the stop condition is satisfied, for example, when the cycle including operation STBa2 has been performed a predetermined number of times.

[0136] When it is determined in operation STBJ that the stop condition is not satisfied, operation STBg2 is performed. Operation STBg2 corresponds to operation STg. Operation STBg2 can be performed by the power supply controller. In operation STBg2, the time series TS_M is prepared by changing the scaling factor in the frequency direction with respect to the basic time series TS_B, as indicated by the arrows in FIGS.

17 through 20. The time series TS_M is prepared by the power supply controller. Then, operation STBa2 is performed again using the time series TS_M prepared in operation STBg2. That is, in the method MTB, the cycle including operation STBa2 is repeated. In the repetition of the cycle including operation STBa2, any one of the time series TS21 through TS24 may be used and the scaling factor may be changed. In the repetition of the cycle including operation STBa2, the time series TS21 through TS24 may be used in order while changing the scaling factor. When it is determined in operation STBJ that the stop condition is satisfied, operation STBh is performed.

[0137] In operation STBh, the time series TS_M (first time series) that most improves, that is, most reduces, the degree of reflection R_D is selected based on the plurality of degrees of reflection R_D that have been obtained. The power supply controller supplies the source radio frequency power HF having the plurality of frequencies included in the selected time series TS_M as the source frequencies f respectively for the plurality of phase periods PH within the waveform cycle CY from the radio frequency power supply 41. After this operation STBh, the method MTB may end. Alternatively, after operation STBh, operation STBi may be performed. In operation STBi, the method MTA is performed using the time series TS_M selected in operation STBh as the basic time series.

[0138] [Third Example]

[0139] Hereinafter, a third example of the method MT including the SS process, that is, a control method of the third example (hereinafter referred to as “method MTC”), will be described with reference to FIGS.

21 and 22. FIG. 21 is a flowchart illustrating the control method of the third example. FIG. 22 is a diagram for explaining the control method of the third example illustrated in FIG. 21. In FIG. 22, the horizontal axis represents time, and the vertical axis represents the electrical bias EB and the source frequency f. FIG. 22 illustrates an example of a waveform of the electrical bias EB in the waveform cycle CY. FIG. 22 also illustrates the basic time series used as the source frequencies f respectively for the plurality of phase periods PH within the waveform cycle CY. In the method MTC, the above-described time series TS3 is used as the modified time series TS_M.

[0140] The method MTC is applied to each series CYS. As illustrated in FIG. 21, the method MTC may start with operation STCp1. In operation STCp1, the method MTA is performed using the basic time series TS_B. Next, operation STCp2 may be performed. In operation STCp2, the time series TS_M (first time series) among the plurality of time series used in operation STCp1 that most improves, that is, most reduces, the degree of reflection R_D is identified based on the plurality of degrees of reflection R_D obtained in operation STCp1, and is selected as the basic time series.

[0141] Next, operation STCp3 may be performed. In operation STCp3, the method MTB is performed using the basic time series selected in operation STCp2. Next, operation STCp4 may be performed. In operation STCp4, the time series TS_M (second time series) among the plurality of time series used in operation STCp3 that most improves, that is, most reduces, the degree of reflection R_D is identified based on the plurality of degrees of reflection R_D obtained in operation STCp3, and is

selected as the basic time series.

[0142] Next, operation STCg1 is performed. Operation STCg1 corresponds to operation STg. In operation STCg1, the power supply controller scales (expands or compresses) two or more of the plurality of time zones of the basic time series selected in operation STCp4 in the time direction to prepare a modified time series TS_M including the same number of frequencies as the basic time series TS_B. Alternatively, operations STAa1 and STAf1 of the method MTA may be performed without performing operations STCp1 through STCp4, and the time series TS_M may be prepared from the basic time series TS_B in operation STCg1.

[0143] The plurality of time zones may include zones Z1 through Z6, as illustrated in FIG. 22. In order to determine the zones Z1 through Z6, the minimum frequency f_{min}, the maximum frequency f_{max}, and the average frequency f_{ave} of the basic time series used in operation STCg1 are identified. Then, the frequency width, which is the difference between the minimum frequency f_{min} and the maximum frequency f_{max} included in the basic time series, is obtained. Then, the time zone corresponding to the range from the minimum frequency f_{min} to the sum of the minimum frequency f_{min} and 10% of the frequency width is determined as zone Z2. Also, the time zone corresponding to the range from the value obtained by subtracting 10% of the frequency width from the maximum frequency f_{max} to the maximum frequency f_{max} is determined as zone Z5. Also, the time zone from the start point of the waveform cycle CY to the start point of zone Z2 is determined as zone Z1. Also, the time zone from the end point of zone Z2 to the time point

corresponding to the average frequency f_{ave} is determined as zone Z3. Also, the time zone from the time point corresponding to the average frequency f_{ave} to the start point of zone Z5 is determined as zone Z4. Also, the time zone from the end point of zone Z5 to the end point of the waveform cycle CY is determined as zone Z6.

[0144] In operation STCg1, zone Z2 of the basic time series may be expanded in the time direction. Also, in order to generate the modified time series TS_M including the same number of frequencies as the basic time series TS_B, zones Z1 and Z3 of the basic time series may be compressed in the time direction.

[0145] Next, operation STCa is performed. Operation STCa corresponds to operation STa. In operation STCa, the power supply controller supplies the source radio frequency power HF having the plurality of frequencies of the time series TS_M as the source frequencies f respectively for the plurality of phase periods PH within the waveform cycle CY from the radio frequency power supply 41.

[0146] Next, operation STCf is performed. In operation STCf, the degree of reflection R_D in the waveform cycle CY is obtained, similarly to operation STAf1.

[0147] Next, operation STCJ is performed. Operation STCJ corresponds to operation STJ. The determination in operation STCJ can be performed by the power supply controller. In operation STCJ, the stop condition is satisfied, for example, when the cycle including operation STCa has been performed a predetermined number of times.

[0148] When it is determined in operation STCJ1 that the stop condition is not satisfied, operation STCg2 is performed. Operation STCg2

corresponds to operation STg. Operation STCg2 can be performed by the power supply controller. In operation STCg2, the scaling factor in the time direction for two or more of the plurality of time zones of the basic time series is changed. The time series TS_M is prepared by operation STCg2. Then, operation STCa is performed again using the time series TS_M prepared in operation STCg2. That is, the cycle including operation STCa is repeated. On the other hand, when it is determined in operation STCJ that the stop condition is satisfied, operation STCh described below is performed.

[0149] In the repetition of the cycle including operation STCa, similarly to operation STCg1, expanding zone Z2 of the basic time series in the time direction and compressing zones Z1 and Z3 of the basic time series in the time direction may be performed while changing the scaling factor of zone Z2 in the time direction. This processing is performed until it is determined based on the degree of reflection R_D obtained in operation STCf that the degree of reflection R_D is no longer improving.

[0150] Next, in the repetition of the cycle including operation STCa, expanding zone Z5 of the basic time series in the time direction and compressing zones Z4 and Z6 of the basic time series in the time direction may be performed while changing the scaling factor of zone Z5 in the time direction. This processing is performed until it is determined based on the degree of reflection R_D obtained in operation STCf that the degree of reflection R_D is no longer improving.

[0151] In operation STCh, the time series TS_M that most improves, that is, most reduces, the degree of reflection R_D from the plurality of degrees of reflection R_D obtained in the repetition of the cycle including

operation STCa is identified and selected as the third time series. The selection of the third time series in operation STCh is performed by the power supply controller. Then, the power supply controller uses the plurality of frequencies included in the selected time series (third time series) as the source frequency f for each of the plurality of phase periods PH within the waveform cycle CY. The processing from operation STCp1 may be repeated using the third time series as the basic time series.

[0152] As described above, in the plasma processing apparatus 1, the time series of the source frequency f in the waveform cycle CY is changed to the time series TS1, the time series TS2, or the time series TS3 so as to improve the degree of reflection R_D in accordance with the degree of reflection R_D. These time series are easily obtained from the basic time series TS_B. Therefore, it is possible to easily suppress reflection of the source radio frequency power HF used for plasma generation.

[0153] Hereinafter, several other examples of the sensor 45 will be described. In another example, the sensor signal SS acquired by the sensor 45 may include, in addition to the voltage signal VS of the reflected wave of the source radio frequency power HF, a voltage signal of the forward wave of the source radio frequency power HF. In this case, an envelope signal is also obtained from the voltage signal of the forward wave in the detector 51, and a plurality of digital values are obtained in the A/D converter 52. In this case, the power supply controller may obtain, as the degree of reflection R_D, the reflectance, that is, (power level of reflected wave)/(power level of forward wave), using

the plurality of digital values obtained from the voltage signal VS of the reflected wave and the plurality of digital values obtained from the voltage signal of the forward wave.

[0154] In yet another example, the sensor 45 may include a voltage sensor and a current sensor. In this example, the sensor 45 is configured to measure a voltage V_{HF} and a current I_{HF} in a feed path connecting the radio frequency power supply 41 and the radio frequency electrode to each other. In this case, the sensor signal SS may be a signal representing an impedance ZL of the load of the radio frequency power supply 41 identified from the voltage V_{HF} and the current I_{HF}, a signal representing a phase difference θ between the voltage V_{HF} and the current I_{HF}, or a signal representing a reflection coefficient Γ identified from the voltage V_{HF} and the current I_{HF}. In this example as well, the power supply controller can identify the degree of reflection R_D using the plurality of digital values obtained from the sensor signal SS via the detector 51 and the A/D converter 52. The degree of reflection R_D may be a representative value (for example, an average value) of the difference between the impedance Z_L and a characteristic impedance (for example, 50 Ω) in each of the waveform cycle CY or the plurality of phase periods PH. Alternatively, the degree of reflection R_D may be a representative value (for example, an average value) of the phase difference θ in each of the waveform cycle CY or the plurality of phase periods PH. Alternatively, the degree of reflection R_D may be a representative value (for example, an average value) of the reflection coefficient Γ in each of the waveform cycle CY or the plurality of phase periods PH.

[0155] Hereinafter, an example of a processing circuit that can be used as one or more processing circuits in the plasma processing apparatus 1, such as the controller 2 and/or the power supply controller, will be described. FIG. 23 is a block diagram of processing circuitry for performing computer-based operations described herein. FIG. 23 illustrates processing circuitry 130 that may be used to control any computer-based control processes, descriptions or blocks in flowcharts can be understood as representing modules, segments or portions of code which include one or more executable instructions for implementing specific logical functions or steps in the process, and alternate implementations are included within the scope of the exemplary embodiments of the present advancements in which functions can be executed out of order from that shown or discussed, including substantially concurrently or in reverse order, depending upon the functionality involved, as would be understood by those skilled in the art. The various elements, features, and processes described herein may be used independently of one another or may be combined in various ways. All possible combinations and sub-combinations are intended to fall within the scope of this disclosure.

[0156] In FIG. 23, the processing circuitry 130 includes a CPU 1200 which performs one or more of the control processes described above/below. The process data and instructions may be stored in memory 1202. These process data and instructions may also be stored on a storage medium disk 1204 such as a hard drive (HDD) or portable storage medium or may be stored remotely. Further, the claimed advancements are not limited by the form of the computer-readable

media on which the instructions of the inventive process are stored. For example, the instructions may be stored on CDs, DVDs, in FLASH memory, RAM, ROM, PROM, EPROM, EEPROM, hard disk or any other information processing device with which the processing circuitry 130 communicates, such as a server or computer.

[0157] Further, the claimed advancements may be provided as a utility application, background daemon, or component of an operating system, or combination thereof, executing in conjunction with CPU 1200 and an operating system such as Microsoft Windows, UNIX, Solaris, LINUX, Apple MAC-OS and other systems known to those skilled in the art.

[0158] The hardware elements in order to achieve the processing circuitry 130 may be realized by various circuitry elements. Further, each of the functions of the above described embodiments may be implemented by circuitry, which includes one or more processing circuits. A processing circuit includes a particularly programmed processor, for example, processor (CPU) 1200, as shown in FIG. 23. A processing circuit also includes devices such as an application specific integrated circuit (ASIC) and conventional circuit components arranged to perform the recited functions.

[0159] In FIG. 23, the processing circuitry 130 includes a CPU 1200 which performs the processes described above. The processing circuitry 130 may be a general-purpose computer or a particular, special-purpose machine. In one embodiment, the processing circuitry 130 becomes a particular, special-purpose machine when the processor 1200 is programmed to control the plasma generator 12 and the gas supply 20, or additionally or alternatively, to control each component of the plasma

processing apparatus 1 in the above-described adjustment of the source frequency f.

[0160] Alternatively, or additionally, the CPU 1200 may be implemented on an FPGA, ASIC, PLD or using discrete logic circuits, as one of ordinary skill in the art would recognize. Further, CPU 1200 may be implemented as multiple processors cooperatively working in parallel to perform the instructions of the inventive processes described above.

[0161] The processing circuitry 130 in FIG. 23 also includes a network controller 1206, such as an Intel Ethernet PRO network interface card from Intel Corporation of America, for interfacing with network 1228. As can be appreciated, the network 1228 can be a public network, such as the Internet, or a private network such as a LAN or WAN network, or any combination thereof and can also include PSTN or ISDN sub-networks. The network 1228 can also be wired, such as an Ethernet network, or can be wireless such as a cellular network including EDGE, 3G and 4G wireless cellular systems. The wireless network can also be Wi-Fi, Bluetooth (registered trademark), or any other wireless form of communication that is known.

[0162] The processing circuitry 130 further includes a display controller 1208, such as a graphics card or graphics adaptor for interfacing with display 1210, such as a monitor. A general purpose I/O interface 1212 interfaces with a keyboard and/or mouse 1214 as well as a touch screen panel 1216 on or separate from display 1210. The general purpose I/O interface also connects to a variety of peripherals 1218 including printers and scanners.

[0163] The storage controller 1224 connects the storage medium disk

1204 with communication bus 1226, which may be an ISA, EISA, VESA, PCI, or similar, for interconnecting all of the components of the processing circuitry 130. A description of the general features and functionality of the display 1210, keyboard and/or mouse 1214, as well as the display controller 1208, storage controller 1224, network controller 1206, sound controller 1220, and general purpose I/O interface 1212 is omitted herein for brevity as these features are known.

[0164] The exemplary circuit elements described in the context of the present disclosure may be replaced with other elements and structured differently than the examples provided herein. Moreover, circuitry configured to perform features described herein may be implemented in multiple circuit units (e.g., chips), or the features may be combined in circuitry on a single chipset.

[0165] The functions and features described herein may also be executed by various distributed components of a system. For example, one or more processors may execute these system functions, wherein the processors are distributed across multiple components communicating in a network. The distributed components may include one or more client and server machines, which may share processing, in addition to various human interface and communication devices (e.g., display monitors, smart phones, tablets, personal digital assistants (PDAs)). The network may be a private network, such as a LAN or WAN, or may be a public network, such as the Internet. Input to the system may be received via direct user input and received remotely either in real-time or as a batch process. Additionally, some implementations may be performed on modules or hardware not identical to those described.

Accordingly, other implementations are within the scope that may be claimed.

[0166] Although various example embodiments have been described above, various additions, omissions, substitutions, and changes may be made without being limited to the example embodiments described above. It is also possible to combine elements in different embodiments to form other embodiments.

[0167] From the above description, it will be understood that various embodiments of the present disclosure have been described herein for purposes of illustration, and that various modifications may be made without departing from the scope and spirit of the present disclosure. Accordingly, the various embodiments disclosed herein are not intended to be limiting, and the true scope and spirit are indicated by the appended claims.

Reference Signs List

[0168] 1: plasma processing apparatus, 10: chamber, 30S: power supply system, 41: radio frequency power supply, 42: bias supply, 45: sensor, 51: detector, 52: A/D converter.

CLAIMS

WHAT IS CLAIMED IS:

[Claim 1]

A plasma processing apparatus comprising:

a chamber;

a substrate support in the chamber;

a radio frequency power supply configured to supply source radio frequency power to generate a plasma from a gas in the chamber;

a bias supply configured to supply an electrical bias to the substrate support to attract ions from the plasma to a substrate on the substrate support;

a sensor configured to acquire a sensor signal reflecting a degree of reflection of the source radio frequency power;

a detector configured to detect an envelope signal of the sensor signal;

an A/D converter configured to perform A/D conversion on the envelope signal output from the detector; and

a power supply controller configured to control the radio frequency power supply,

wherein the power supply controller is configured to, in accordance with the degree of reflection in a waveform cycle of the electrical bias identified from a plurality of digital values generated by the A/D converter from the envelope signal in the waveform cycle, or in accordance with the degree of reflection in each of a plurality of phase periods that divide the waveform cycle, adjust a source frequency of the

source radio frequency power for each of the plurality of phase periods to reduce the degree of reflection in a subsequent waveform cycle of the electrical bias, and

wherein a sampling frequency of the A/D converter is not less than twice a product of a bias frequency, which is a reciprocal of a time length of the waveform cycle, and a number of the plurality of phase periods within the waveform cycle, and is not greater than a minimum frequency of the source frequency adjustable by the radio frequency power supply.

[Claim 2]

The plasma processing apparatus according to claim 1, wherein the detector includes:

a detection circuit;

an attenuator and a first filter connected between the sensor and the detection circuit; and

a second filter and an amplifier connected between the detection circuit and the A/D converter,

the detection circuit is configured to detect a first envelope signal from a first signal generated by attenuation of the sensor signal in the attenuator and filtering in the first filter, and

the detector is configured to output, to the A/D converter, a second envelope signal generated by filtering of the first envelope signal in the second filter and amplification in the amplifier.

[Claim 3]

The plasma processing apparatus according to claim 2,

wherein an upper cutoff frequency of the first filter is greater than or equal to a maximum frequency of the source frequency adjustable by the radio frequency power supply and is less than or equal to twice the minimum frequency, and

wherein a lower cutoff frequency of the first filter is less than or equal to the minimum frequency.

[Claim 4]

The plasma processing apparatus according to claim 3,

wherein the second filter is a low-pass filter, and

wherein an upper cutoff frequency of the second filter has a value between the product of the bias frequency and the number of the plurality of phase periods within the waveform cycle and the upper cutoff frequency of the first filter.

[Claim 5]

The plasma processing apparatus according to claim 4, wherein the upper cutoff frequency of the second filter is less than or equal to the minimum frequency.

[Claim 6]

The plasma processing apparatus according to any one of claims 1 to 5,

wherein the sensor is a directional coupler, and

wherein the sensor signal is a voltage signal of a reflected wave

of the source radio frequency power.

[Claim 7]

A power supply system comprising:

a radio frequency power supply configured to supply source radio frequency power to generate a plasma from a gas in a chamber of a plasma processing apparatus;

a bias supply configured to supply an electrical bias to a substrate support to attract ions from the plasma to a substrate on the substrate support in the chamber;

a sensor configured to acquire a sensor signal reflecting a degree of reflection of the source radio frequency power;

a detector configured to detect an envelope signal of the sensor signal;

an A/D converter configured to perform A/D conversion on the envelope signal output from the detector; and

a power supply controller configured to control the radio frequency power supply,

wherein the power supply controller is configured to, in accordance with the degree of reflection in a waveform cycle of the electrical bias identified from a plurality of digital values generated by the A/D converter from the envelope signal in the waveform cycle, or in accordance with the degree of reflection in each of a plurality of phase periods that divide the waveform cycle, adjust a source frequency of the source radio frequency power for each of the plurality of phase periods to reduce the degree of reflection in a subsequent waveform cycle of the

electrical bias, and

wherein a sampling frequency of the A/D converter is not less than twice a product of a bias frequency, which is a reciprocal of a time length of the waveform cycle, and a number of the plurality of phase periods within the waveform cycle, and is not greater than a minimum frequency of the source frequency adjustable by the radio frequency power supply.

[Claim 8]

The power supply system according to claim 7,

wherein the sensor is a directional coupler, and

wherein the sensor signal is a voltage signal of a reflected wave of the source radio frequency power.

[Claim 9]

A control method comprising:

(a) supplying source radio frequency power from a radio frequency power supply to generate a plasma from a gas in a chamber of a plasma processing apparatus;

(b) supplying an electrical bias from a bias supply to a substrate support to attract ions from the plasma to a substrate on the substrate support in the chamber;

(c) acquiring, in a sensor, a sensor signal reflecting a degree of reflection of the source radio frequency power;

(d) detecting, in a detector, an envelope signal of the sensor signal;

(e) performing, in an A/D converter, A/D conversion on the envelope signal output from the detector;

(f) identifying, from a plurality of digital values generated by the A/D converter from the envelope signal in a waveform cycle of the electrical bias, the degree of reflection in the waveform cycle or the degree of reflection in each of a plurality of phase periods that divide the waveform cycle; and

(g) adjusting, by a power supply controller, a source frequency of the source radio frequency power for each of the plurality of phase periods to reduce the degree of reflection in a subsequent waveform cycle of the electrical bias, in accordance with the degree of reflection identified in (f),

wherein a sampling frequency of the A/D converter is not less than twice a product of a bias frequency, which is a reciprocal of a time length of the waveform cycle, and a number of the plurality of phase periods within the waveform cycle, and is not greater than a minimum frequency of the source frequency adjustable by the radio frequency power supply.

[Claim 10]

The control method according to claim 9,

wherein the sensor is a directional coupler, and

wherein the sensor signal is a voltage signal of a reflected wave of the source radio frequency power.