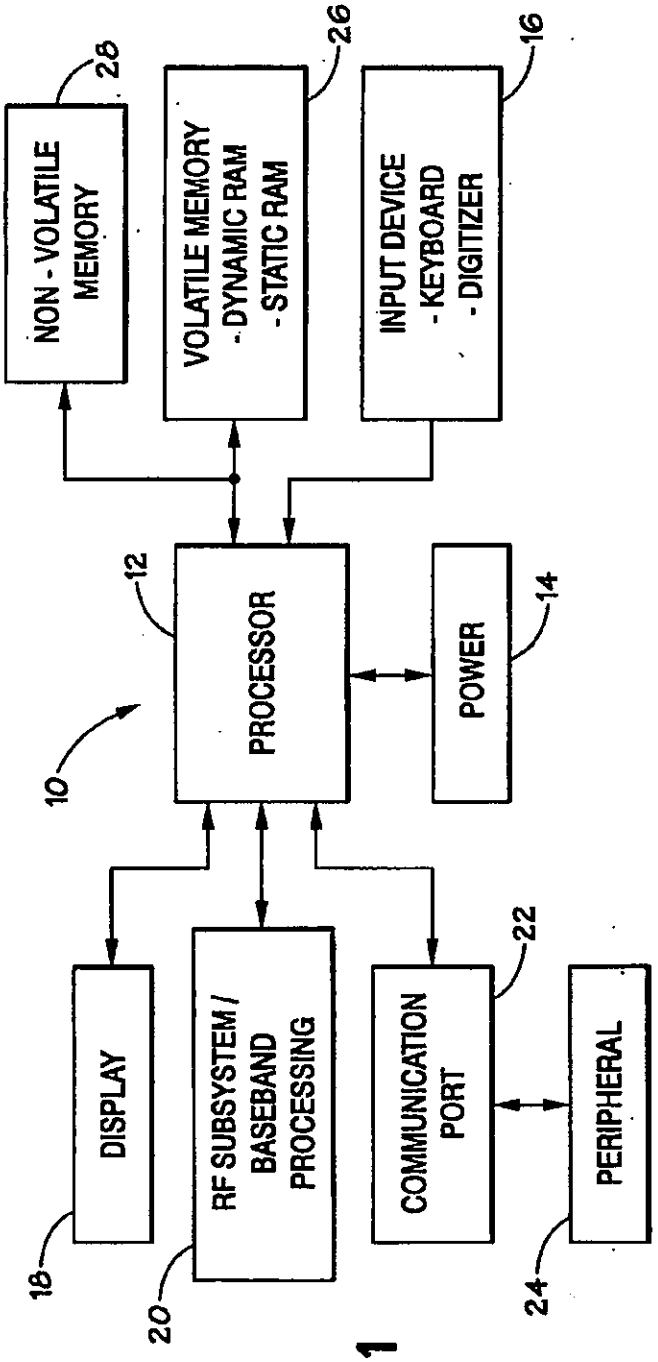

NON - VOLATILE MEMORY
28
VOLATILE MEMORY
- DYNAMIC RAM
- STATIC RAM
26
INPUT DEVICE
- KEYBOARD
- DIGITIZER
16
PROCESSOR
12
POWER
14
10
DISPLAY
18
RF SUBSYSTEM / BASEBAND PROCESSING
20
COMMUNICATION PORT
22
PERIPHERAL
24

FIG. 1

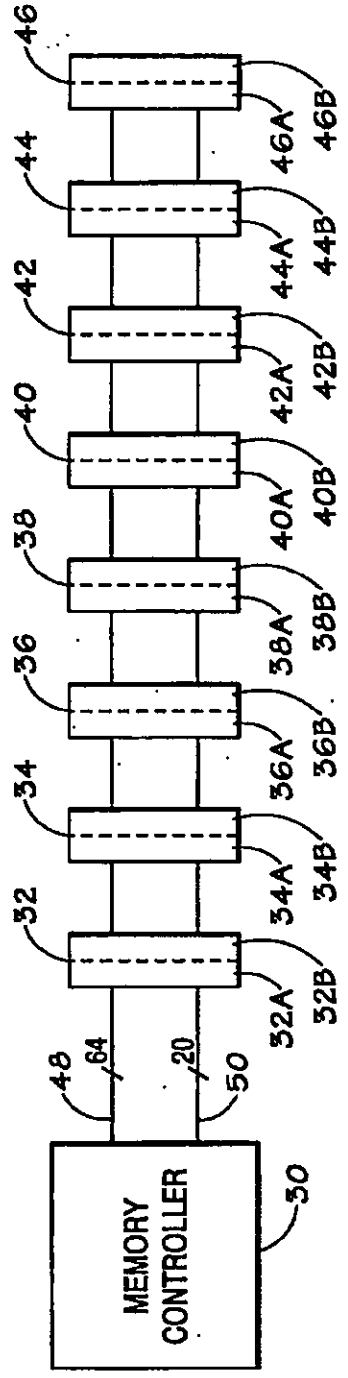

46
46A
46B
44
44A
44B
42
42A
42B
40
40A
40B
38
38A
38B
36
36A
36B
34
34A
34B
32
32A
32B
48
64
20
50
MEMORY CONTROLLER
30

FIG. 2

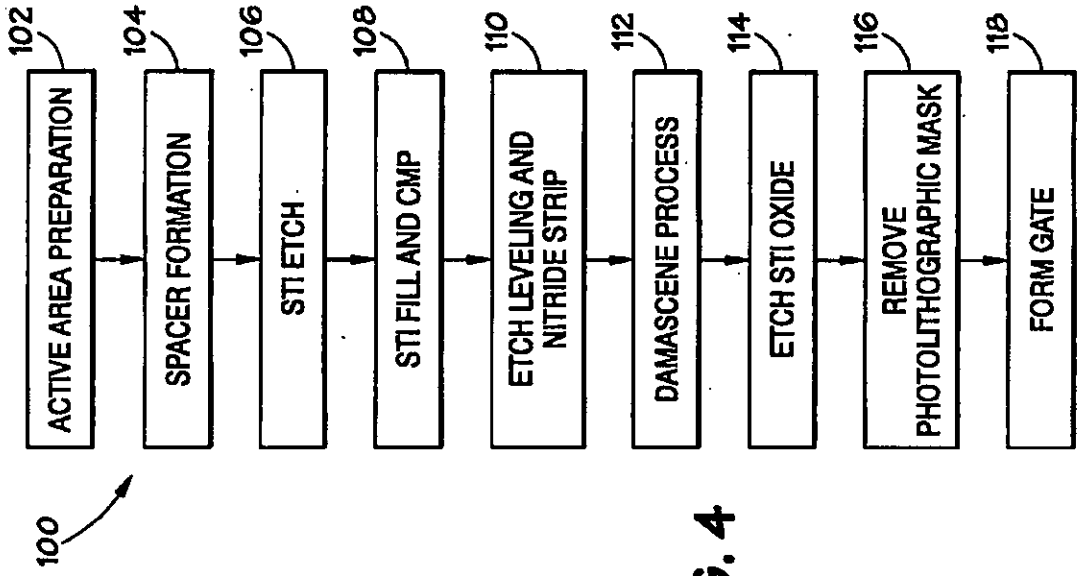

102
104
106
108
110
112
114
116
118
ACTIVE AREA PREPARATION
SPACER FORMATION
STI ETCH
STI FILL AND CMP
ETCH LEVELING AND NITRIDE STRIP
DAMASCENE PROCESS
ETCH STI OXIDE
REMOVE PHOTOLITHOGRAPHIC MASK
FORM GATE
100

FIG. 4

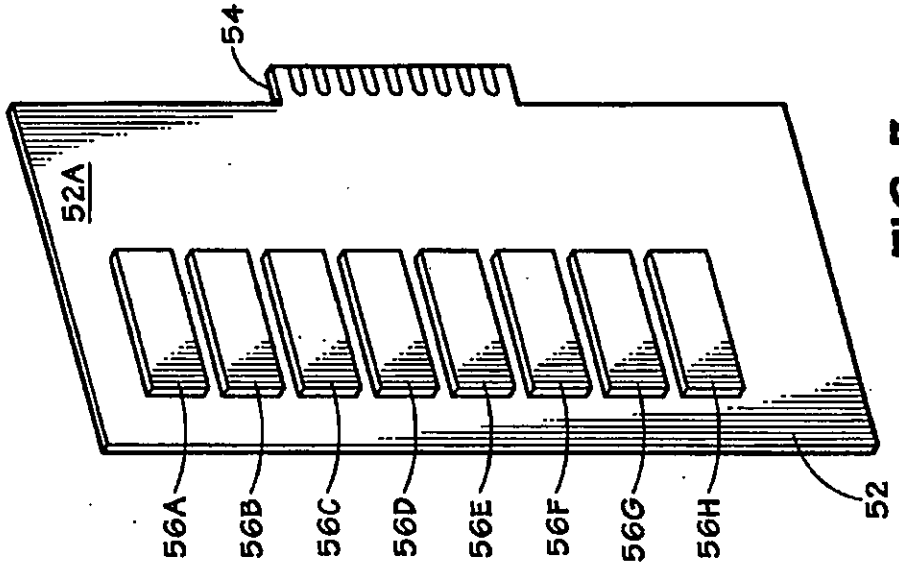

54
52A
56A
56B
56C
56D
56E
56F
56G
56H
52

FIG. 3

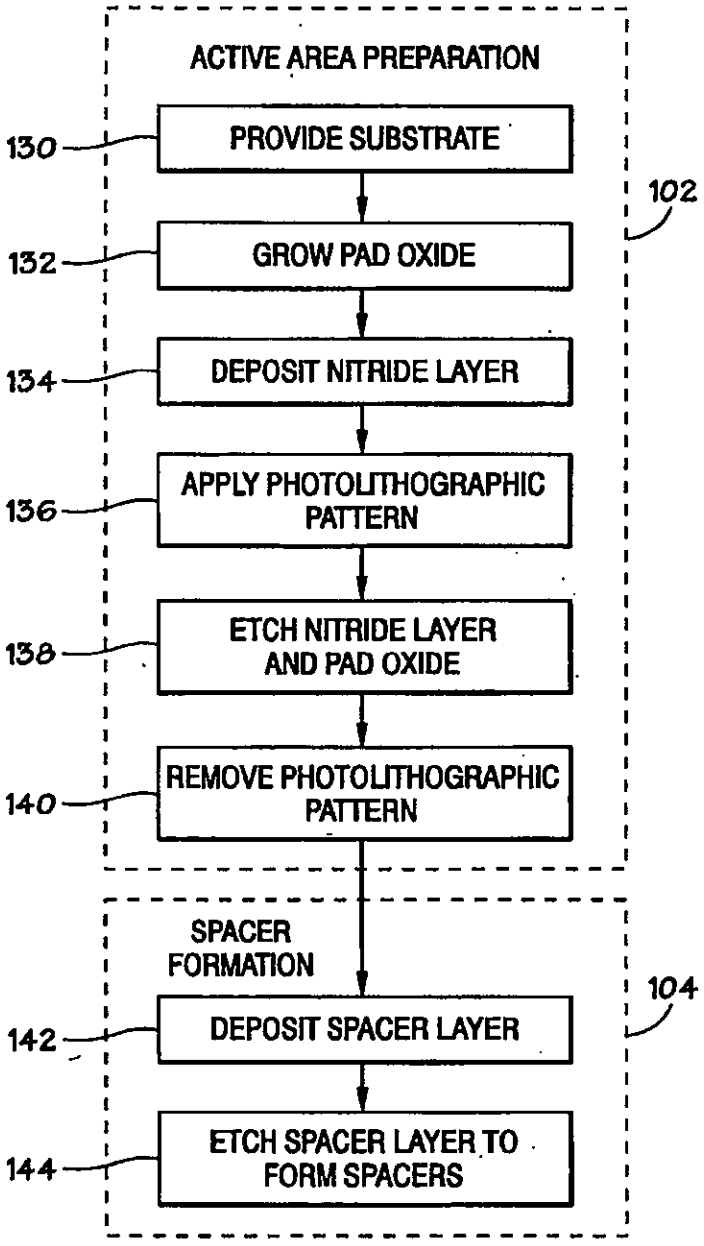

ACTIVE AREA PREPARATION
130
PROVIDE SUBSTRATE
102
132
GROW PAD OXIDE
134
DEPOSIT NITRIDE LAYER
136
APPLY PHOTOLITHOGRAPHIC PATTERN
138
ETCH NITRIDE LAYER AND PAD OXIDE
140
REMOVE PHOTOLITHOGRAPHIC PATTERN
SPACER FORMATION
104
142
DEPOSIT SPACER LAYER
144
ETCH SPACER LAYER TO FORM SPACERS

FIG. 5

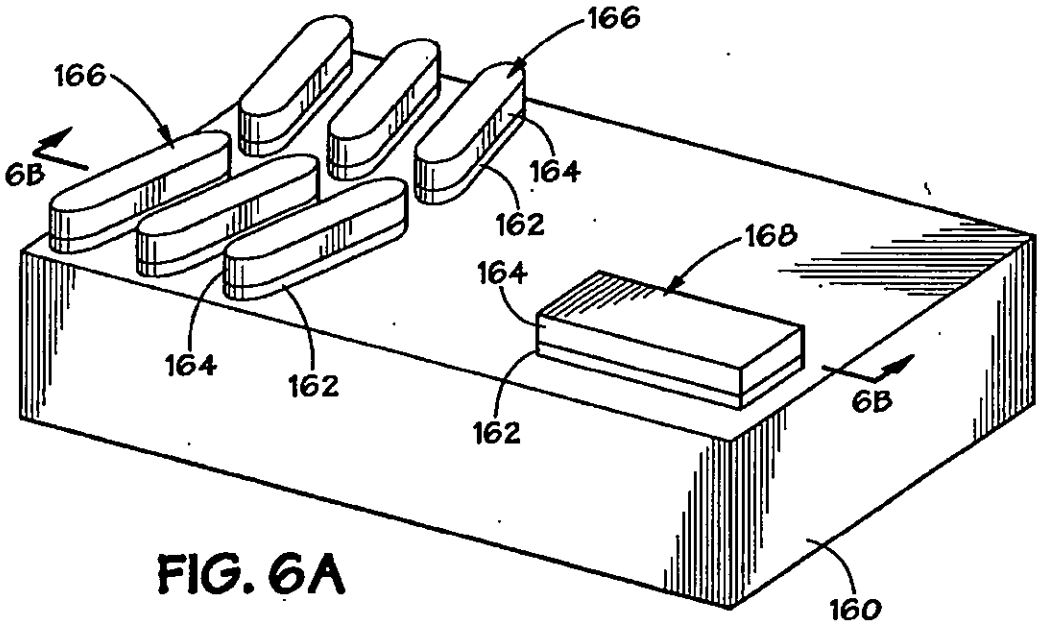


FIG. 6A

FIG. 6B

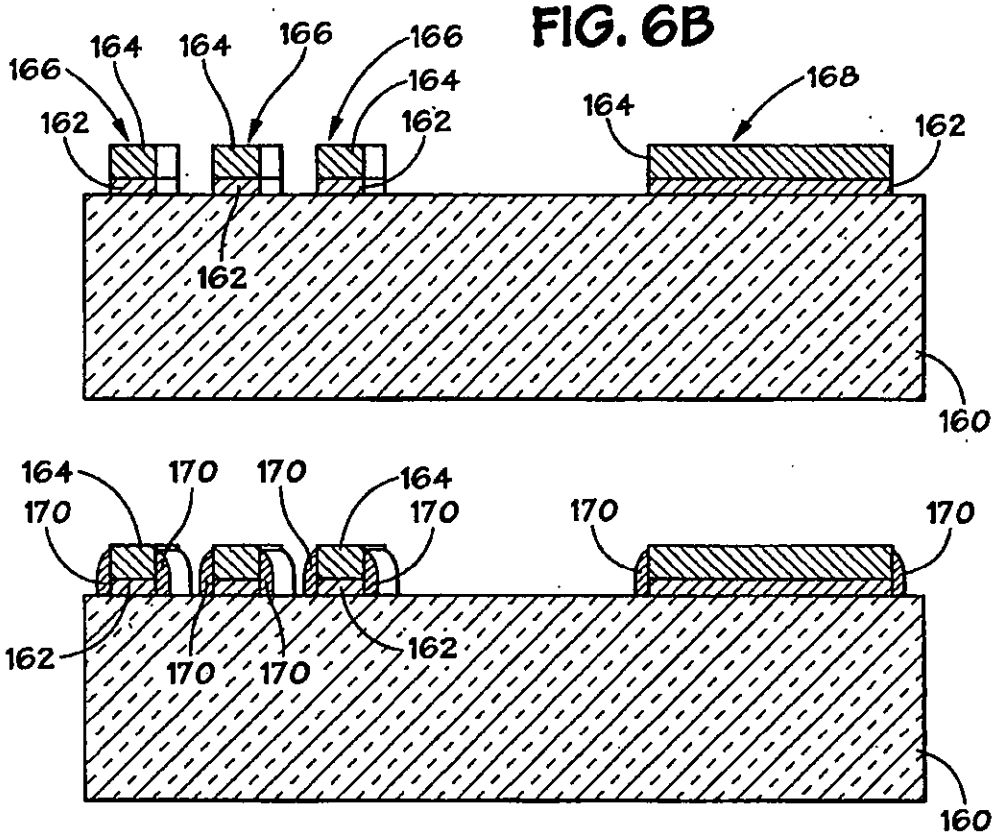


FIG. 7

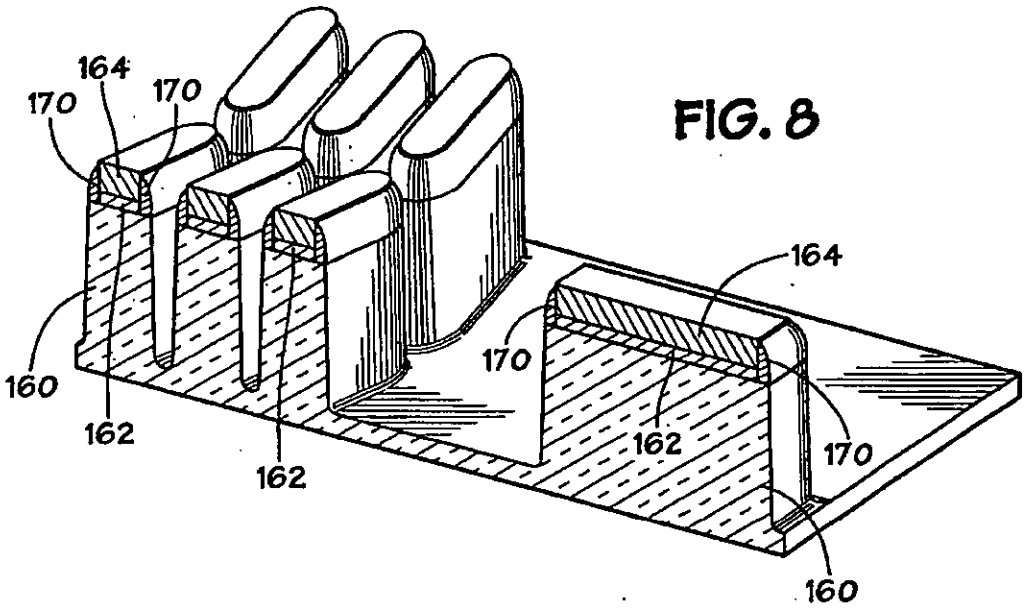


FIG. 8

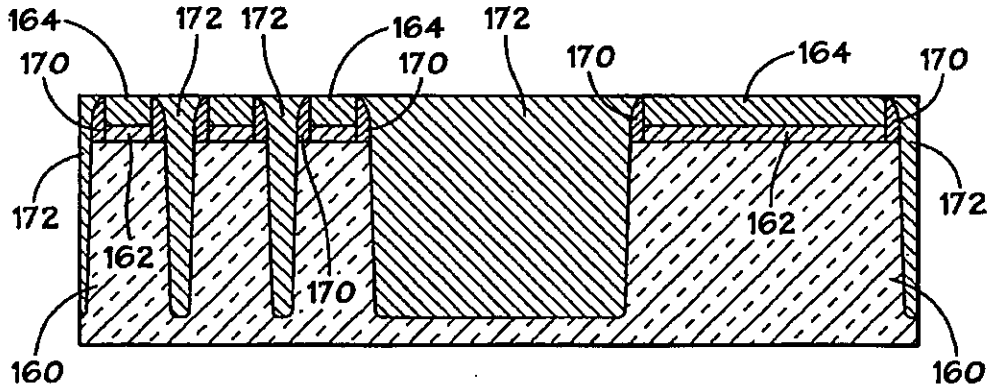


FIG. 9

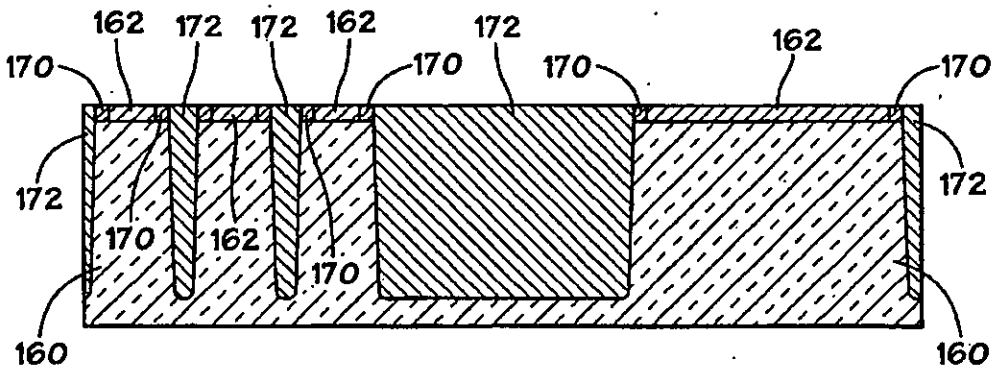
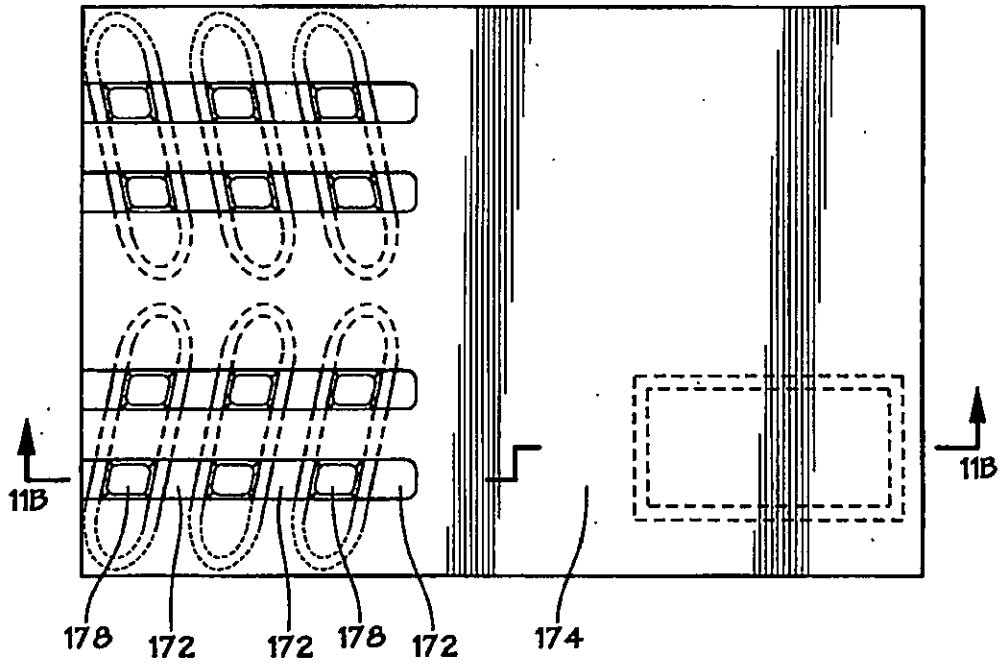


FIG. 10

FIG. 11A



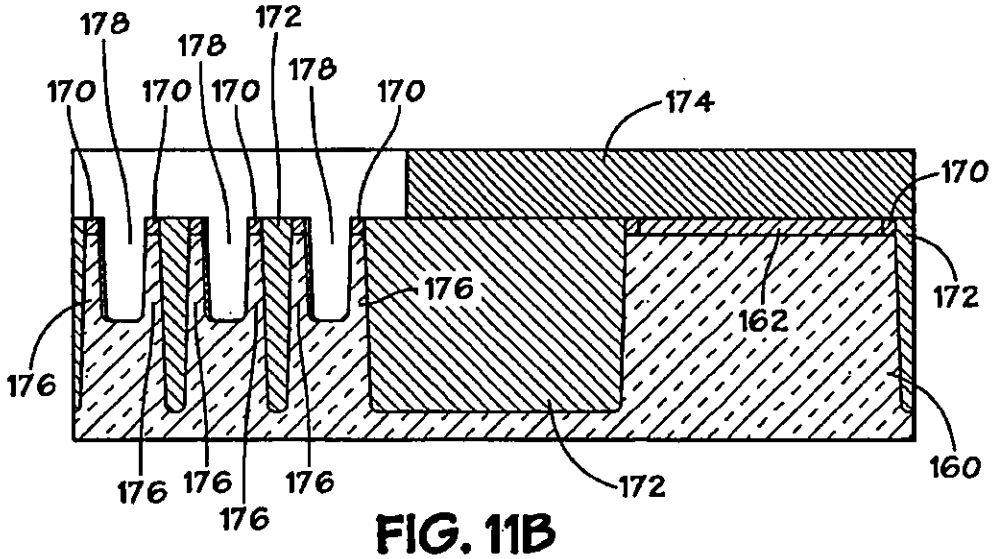
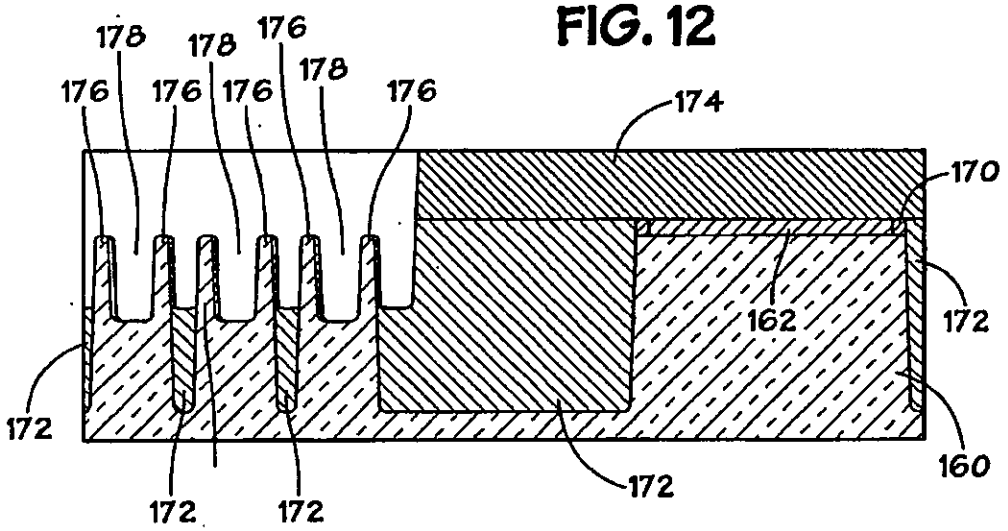


FIG. 11B

FIG. 12


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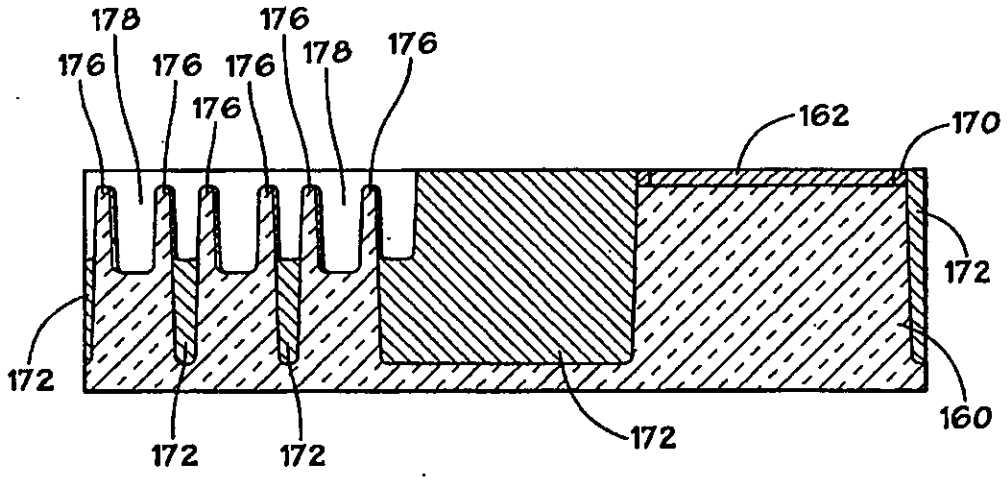
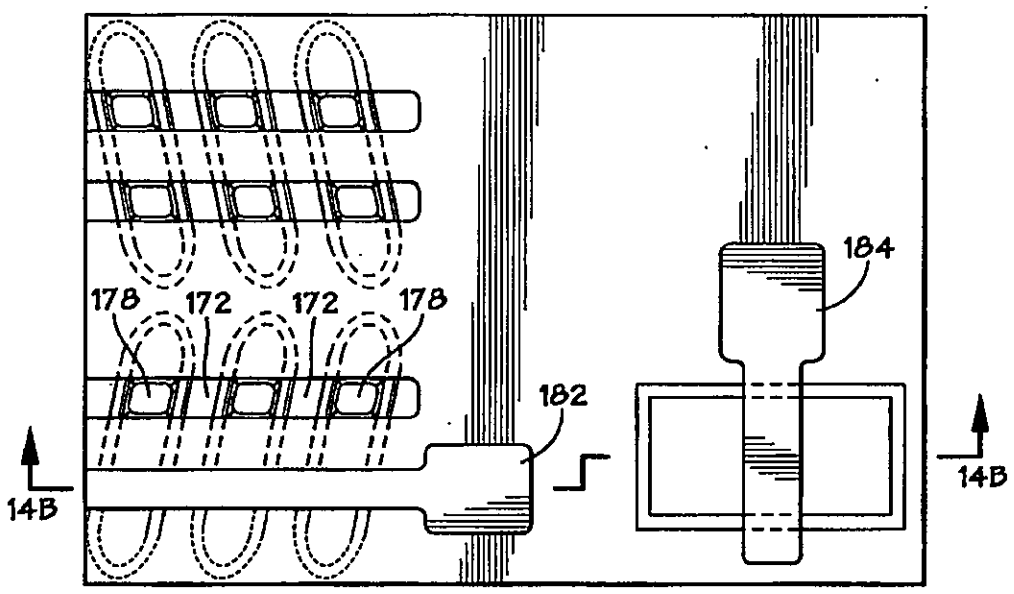

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FIG. 13

FIG. 14A



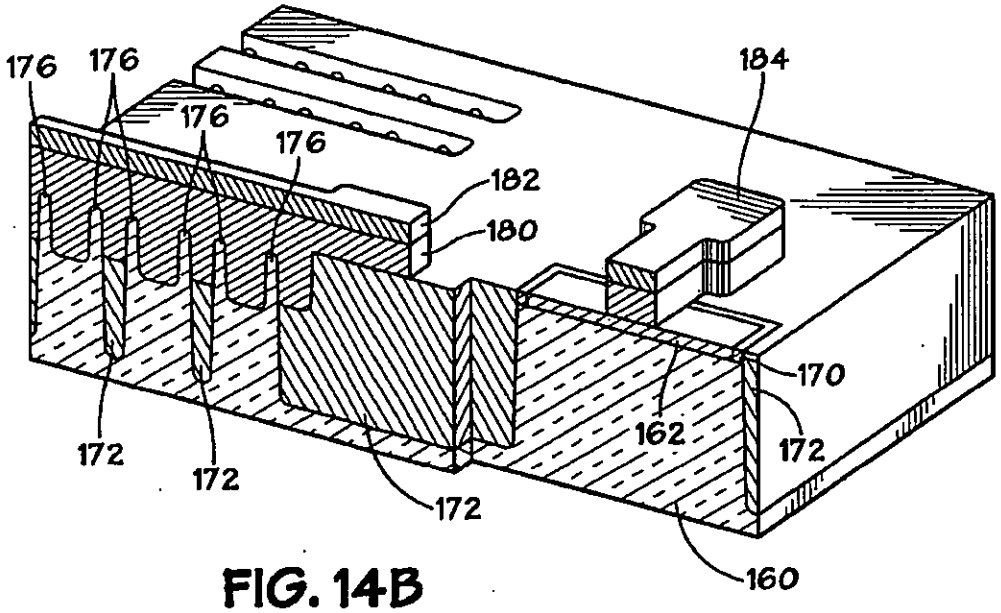


FIG. 14B