28/8/02
20020519 51

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

162162

(43) International Publication Date
27 September 2001 (27.09.2001)

PCT

(10) International Publication Number
WO 01/71803 A1

(51) International Patent Classification[7]: H01L 21/8247, 21/8246

(21) International Application Number: PCT/US01/07975

(22) International Filing Date: 12 March 2001 (12.03.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/190,475 17 March 2000 (17.03.2000) US
09/728,554 1 December 2000 (01.12.2000) US

(71) Applicant: ADVANCED MICRO DEVICES, INC. [US/US]; One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).

(72) Inventors: SHIELDS, Jeffrey, A.; 445 Kenmore Avenue, Sunnyvale, CA 94086 (US). PHAM, Tuan, D.; 287 Cannikin Drive, San Jose, CA 95116 (US). RAMSBEY, Mark, T.; 402 Cumulus Avenue, Sunnyvale, CA 94087 (US). SUN, Yu; 20395 Glasgow Drive, Saratoga, CA 95070 (US). HUI, Angela, T.; 362 Pilgrim Loop, Fremont, CA 94539 (US). CHAN, Maria, Chow; 3427 San Saba Drive, San Jose, CA 95148 (US).

(74) Agent: RODDY, Richard, J.; Advanced Micro Devices, Inc., One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).

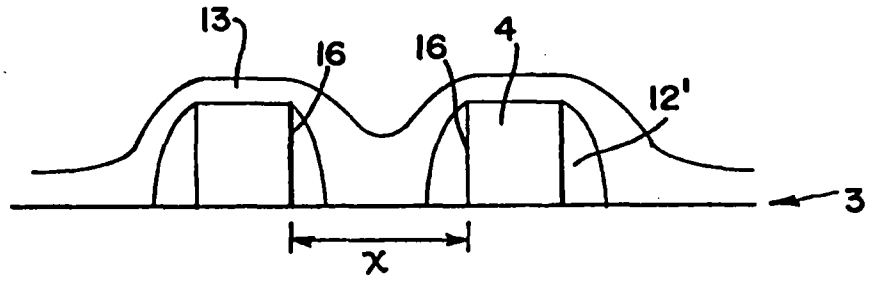
(81) Designated States *(national)*: BR, CN, JP, KR, SG.

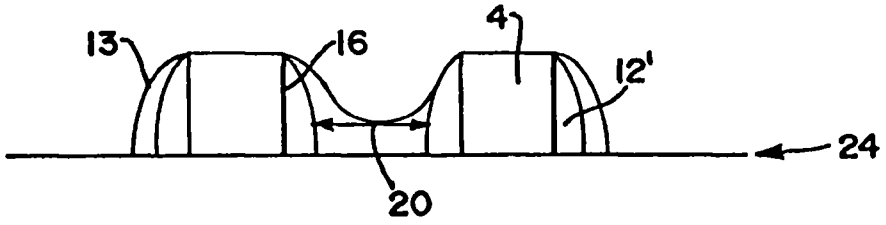
(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: A DUAL SPACER PROCESS FOR NON-VOLATILE MEMORY DEVICES





(57) Abstract: In a two-step spacer fabrication process for a non-volatile memory device (1), a thin oxide layer (12) is deposited on a wafer substrate (3) leaving a gap in the core (24) of the non-volatile memory device (1). Implantation and/or oxide-nitride-oxide removal can be accomplished through this gap. After implantation, a second spacer (13) is deposited. After the second spacer deposition, a periphery spacer etch is performed. By the above method, a spacer is formed.

WO 01/71803 A1

ACTION