

CLAIMS:

What is claimed is:

1. A non-volatile memory (NVM) device, comprising:
 - a NVM array to store data;
 - a command interface coupled to the NVM array, the command interface to receive a controlled power off command from a controller; and
 - a status register unit coupled to the NVM array, the status register unit to store information indicating whether the NVM device is implementing a background operation, the information to be read by the controller after the controlled power off command is received, and the NVM device to safely suspend the background operation in response to the controlled power off command prior to loss of supply power when the NVM device is determined to be implementing the background operation, wherein the NVM device is configured to complete the suspended background operation after the supply power is restored.
2. The integrated circuit device of claim 1, wherein the background operation is safely suspended automatically prior to the loss of the supply power.
3. A non-volatile memory (NVM) device, comprising:
 - a NVM array to store data;
 - a command interface coupled to the NVM array, the command interface to receive a controlled power off command from a controller; and
 - a status register unit coupled to the NVM array, the status register unit to store information indicating whether the NVM device is implementing a background operation, and the NVM device to safely suspend the background operation in response to the controlled power off command prior to loss of supply power when the NVM device is determined to be implementing the background operation, wherein the NVM device is configured to complete the suspended background operation after the supply power is restored, wherein the command interface is configured to send a memory acknowledgement to the controller in response to the controlled power off command through a status register.
4. The integrated circuit device of claim 1, wherein the background operation further comprises a memory array refresh or a wear-leveling algorithm.

5. The integrated circuit device of claim 1, wherein the status register unit is configured to store information indicating whether the NVM device has safely suspended or completed the background operation.
6. The integrated circuit device of claim 1, wherein the status register unit is configured to store information used by the NVM device in resuming the suspended background operation upon restoration of the supply power.
7. A data processing device, comprising:
 - a processing unit having one or more processor cores; and
 - system memory coupled to the processing unit, the system memory having a non-volatile memory (NVM) device comprising:
 - a NVM array to store data;
 - a command interface coupled to the NVM array, the command interface to receive a controlled power off command from the processing unit; and
 - a status register unit coupled to the NVM array, the status register unit to store information indicating whether the NVM device is implementing a background operation, the information to be read by the processing unit after the controlled power off command is received, the NVM device to safely suspend the background operation in response to the controlled power off command prior to loss of supply power when the NVM device is determined to be implementing the background operation, wherein the NVM device is configured to complete the suspended background operation after the supply power is restored.
8. The data processing device of claim 7, further comprising:
 - a power management unit, coupled to the processing unit, to remove the supply power from the NVM device after the background operation is safely suspended.
9. A data processing device, comprising:
 - a processing unit having one or more processor cores; and
 - system memory coupled to the processing unit, the system memory having a non-volatile memory (NVM) device comprising:
 - a NVM array to store data;
 - a command interface coupled to the NVM array, the command interface to receive a controlled power off command from the processing unit; and
 - a status register unit coupled to the NVM array, the status register unit to store information indicating whether the NVM device is implementing a background

operation the NVM device to safely suspend the background operation in response to the controlled power off command and prior to loss of supply power when the NVM device is determined to be implementing the background operation, wherein the NVM device is configured to complete the suspended background operation after the supply power is restored, wherein the command interface is configured to send a memory acknowledgement through a status register to the processing unit in response to the controlled power off command.

10. The data processing device of claim 7, wherein the data processing device is a wireless communication device further comprising:

a transceiver coupled to the processing unit, the transceiver to receive over-the-air signals.

11. A method, comprising:

issuing a controlled power off command to a memory device using a controller;

reading a status register unit of the memory device;

determining whether the memory device is performing a background operation based on reading the status register unit of the memory device, the status register unit to store information safely suspending the background operation in response to the controlled power off command when the memory device is determined to be performing the background operation;

safely removing supply power;

subsequently restoring the supply power to the memory device; and

completing the suspended background operation after restoring the supply power to the memory device.

12. The method of claim 11, further comprising:

detecting a predicted controlled power loss event issuing a controlled power off command in response to the detection.

13. The method of claim 11, further comprising:

receiving a memory acknowledgement at the controller from the memory device in response to the controlled power of command or waiting a certain time period prior to safely suspending the background operation or completing the background operation.

14. The method of claim 11, wherein if the memory device is not performing the background operation then the supply power is safely removed.

15. The method of claim 11, wherein the memory device is configured to implement the background task without the host controller having an awareness of the background operation until reading the status register unit of the memory device.

CLAIMS:

What is claimed is:

1. A non-volatile memory (NVM) device, comprising:
 - a NVM array to store data;
 - a command interface coupled to the NVM array, the command interface to receive a controlled power off command from a controller; and
 - a status register unit coupled to the NVM array, the status register unit to store information indicating whether the NVM device is implementing a background operation, the NVM device to safely suspend the background operation or to complete the background operation prior to loss of a supply power if the NVM device is implementing the background operation.
2. The integrated circuit device of claim 1, wherein background operation is safely completed or suspended automatically prior to the loss of the supply power.
3. The integrated circuit device of claim 1, the device is configured to complete the suspended background operation after power is restored.
4. The integrated circuit device of claim 1, wherein the command interface to send a memory acknowledgement to the controller in response to the controlled power off command through a status register.

5. The integrated circuit device of claim 1, wherein the background operation further comprises a memory array refresh or a wear-leveling algorithm.
6. The integrated circuit device of claim 1, wherein the status register unit to store information indicating whether the NVM device has safely suspended or completed the background operation.
7. The integrated circuit device of claim 1, wherein the status register unit to store information used by the NVM device in resuming the suspended background operation upon restoration of the supply power.
8. A data processing device, comprising:
- a processing unit having one or more processor cores; and
 - system memory coupled to the processing unit, the system memory having a non-volatile memory (NVM) device comprising:
 - a NVM array to store data;
 - a command interface coupled to the NVM array, the command interface to receive a controlled power off command from the processing unit;
 - a status register unit coupled to the NVM array, the status register unit to store information indicating whether the NVM device is implementing a background operation, the NVM device to safely suspend the background operation or to complete the background operation prior to loss of a supply power if the NVM device is implementing the background operation.

9. The data processing device of claim 8, further comprising:

a power management unit, coupled to the processing unit, to remove the supply power from the NVM device after the background operation is safely completed or suspended.

10. The data processing device of claim 8, the NVM device is configured to complete the suspended background operation after power is restored by the power management unit.

11. The data processing device of claim 8, wherein the command interface to send a memory acknowledgement through a status register to the processing unit in response to the controlled power off command.

12. The data processing device of claim 8, wherein the data processing device is a wireless communication device further comprising:

a transceiver coupled to the processing unit, the transceiver to receive over-the-air signals.

13. A method, comprising:

issuing a controlled power off command to a memory device using a controller;

determining whether the memory device is performing a background operation;

safely suspending the background operation or completing the background operation if the memory device is performing the background operation; and

safely removing a supply power.

14. The method of claim 13, further comprising:

detecting a controlled power loss event predicted to occur with the controlled power off command being issued in response to the detection of the power loss event; and

reading a status register unit of the memory device to determine whether the memory device is performing the background operation.

15. The method of claim 13, further comprising:

subsequently restoring power to the memory device.

16. The method of claim 15, further comprising:

completing the suspended background operation after restoring power to the memory device.

17. The method of claim 13, further comprising:

receiving a memory acknowledgement at the host controller from the memory device in response to the controlled power off command or waiting a certain time period prior to safely suspending the background operation or completing the background operation.

18. The method of claim 13, wherein if the memory device is not performing the background operation then the power supply is safely removed.

19. The method of claim 13, wherein the memory device to implement the background task without the host controller having an awareness of the background operation until reading the status register unit of the memory device.