

WHAT IS CLAIMED IS:

1. A substrate processing system, comprising:

a measurement device configured to measure errors of substrates after the substrates are subjected to processing of a first process by a first processing apparatus that performs processing of the first process on the substrates;

a transfer device configured to transfer the substrates between apparatuses including the first processing apparatus, a second processing apparatus that performs processing of a second process on the substrates after the first process, and the measurement device;

a map creating device configured to create, for each of the substrates, an error map indicating a distribution of the errors on the substrates; and

an evaluation device configured to calculate, for each of the substrates, an evaluation value indicating a degree of importance of the errors based on the error map,

wherein the evaluation device instructs the transfer device on a transfer destination of the substrates subjected to the first process according to a determination result as to whether or not the evaluation value is equal to or larger than a predetermined first threshold value,

wherein the map creating device includes:

an error amount specifier configured to specify, for each of the substrates, an error amount, which is a numerical value indicating an amount of errors, with respect to each of chip regions, which are regions on the substrates where chips are arranged;

an updater configured to update, for each of the substrates, the error amount in the chip region containing the errors to a total value of the error amount in the chip region containing the errors and error amounts in other chip regions adjacent to the chip region containing the errors; and

a creator configured to specify, for each of the substrates, a predetermined percentage of chip regions in a descending order of error amounts among the chip regions on the substrates and create an error map indicating a distribution of the specified chip regions.

2. The substrate processing system of Claim 1, wherein when the evaluation device determines that the evaluation value is equal to or larger than the predetermined first threshold value, the evaluation device instructs the transfer device to discard the substrates subjected to the first process without transferring the substrates to the second processing apparatus.

3. The substrate processing system of Claim 1 or 2, wherein the updater updates the error amounts in the chip regions for the substrates having the total value of the error amounts specified for the chip regions equal to or larger than a predetermined value.

4. The substrate processing system of any one of Claims 1 to 3, wherein the evaluation device includes:

a deterioration level specifier configured to refer to data in which reference maps as different predetermined error maps are respectively associated with deterioration levels, which are numerical values indicating degrees of deterioration of causes of errors constituting a distribution of the reference maps, and specify, for each of the substrates, a deterioration level associated with the reference map having the highest similarity to the error map created by the map creating device; and

an evaluation value calculator configured to calculate, for each of the substrates, a product of the deterioration level and a degree of influence of the first process as the evaluation value of the substrates subjected to the processing of the first process.

5. A substrate processing system, comprising:

a measurement device configured to measure errors of substrates after the substrates are subjected to processing of a first process by a first processing apparatus that performs processing of the first process on the substrates;

a transfer device configured to transfer the substrates between apparatuses including the

first processing apparatus, a second processing apparatus that performs processing of a second process on the substrates after the first process, and the measurement device;

a map creating device configured to create, for each of the substrates, an error map indicating a distribution of the errors on the substrates; and

an evaluation device configured to calculate, for each of the substrates, an evaluation value indicating a degree of importance of the errors based on the error map,

wherein the evaluation device instructs the transfer device on a transfer destination of the substrates subjected to the first process according to a determination result as to whether or not the evaluation value is equal to or larger than a predetermined first threshold value,

wherein the evaluation device includes:

a deterioration level specifier configured to refer to data in which reference maps as different predetermined error maps are respectively associated with deterioration levels, which are numerical values indicating degrees of deterioration of causes of errors constituting a distribution of the reference maps, and specify, for each of the substrates, a deterioration level associated with the reference map having the highest similarity to the error map created by the map creating device; and

an evaluation value calculator configured to calculate, for each of the substrates, a product of the deterioration level and a degree of influence of the first process as the evaluation value of the substrates subjected to the processing of the first process.

6. The substrate processing system of Claim 5, wherein when the evaluation device determines that the evaluation value is equal to or larger than the predetermined first threshold value, the evaluation device instructs the transfer device to discard the substrates subjected to the first process without transferring the substrates to the second processing apparatus.

7. The substrate processing system of Claim 5 or 6, wherein the map creating device includes: an error amount specifier configured to specify, for each of the substrates, an error

amount, which is a numerical value indicating an amount of errors, with respect to each of chip regions, which are regions on the substrates where chips are arranged.

8. The substrate processing system of Claim 7, wherein the map creating device includes:
an updater configured to update, for each of the substrates, the error amount in the chip region containing the errors to a total value of the error amount in the chip region containing the errors and error amounts in other chip regions adjacent to the chip region containing the errors;
and

a creator configured to specify, for each of the substrates, a predetermined percentage of chip regions in a descending order of error amounts among the chip regions on the substrates and create an error map indicating a distribution of the specified chip regions.

9. The substrate processing system of Claim 8, wherein the updater updates the error amounts in the chip regions for the substrates having the total value of the error amounts specified for the chip regions equal to or larger than a predetermined value.

10. The substrate processing system of any one of Claims 4 to 9, wherein the deterioration level specifier refers to data in which the reference maps as different predetermined error maps are associated with the causes of errors in the distribution of the reference maps, and further specifies, for each of the substrates, a cause associated with the reference map having the highest similarity to the error map created by the map creating device, and

wherein the evaluation device includes an outputter configured to output the cause specified by the deterioration level specifier in association with identification information of each of the substrates.

11. The substrate processing system of any one of Claims 4 to 10, wherein the evaluation value calculator stops the first processing apparatus when the evaluation value is equal to or larger than a second threshold value larger than the first threshold value.

12. A substrate processing method, comprising:

(a) measuring, for each of substrates, errors of the substrates after the substrates are subjected to processing of a first process by a first processing apparatus;

(b) creating, for each of the substrates, an error map indicating a distribution of the errors on the substrates;

(c) calculating, for each of the substrates, an evaluation value indicating a degree of importance of the errors based on the error map;

(d) determining a transfer destination of the substrates subjected to the first process according to a determination result as to whether or not the evaluation value is equal to or larger than a predetermined first threshold value;

(e) acquiring, for each of the substrates, information on chip regions, which are regions on the substrates where chips are arranged; and

(f) specifying, for each of the substrates, an error amount, which is a numerical value indicating an amount of errors, with respect to each of the chip regions;

(g) updating, for each of the substrates, the error amount in the chip region containing the errors to a total value of the error amount in the chip region containing the errors and error amounts in other chip regions adjacent to the chip region containing the errors, and

(h) specifying, for each of the substrates, a predetermined percentage of chip regions in a descending order of error amounts among the chip regions on the substrates and creating an error map indicating a distribution of the specified chip regions.

13. A map creating device, comprising:

an error amount specifier configured to specify, for each of substrates, an error amount,

which is a numerical value indicating an amount of errors, with respect to each of chip regions, which are regions on the substrates where chips are arranged;

a creator configured to specify, for each of the substrates, a predetermined percentage of chip regions in a descending order of error amounts among the chip regions on the substrates, and create an error map indicating a distribution of the specified chip regions; and

an updater configured to update, for each of the substrates, the error amount in the chip region containing the errors to a total value of the error amount in the chip region containing the errors and the error amounts in other chip regions adjacent to the chip region containing the errors.