CLAIMS

1. A method of forming an electrical connection structure, the method comprising:

   forming a cavity on a front surface of a substrate, the substrate comprising an electrically conductive pad, by etching through the electrically conductive pad;

   forming one or more dielectric liner layers covering an inner surface of the cavity;

   forming a via hole extending from the cavity by etching through the one or more dielectric liner layers;

   forming one or more further dielectric liner layers covering an inner surface of the via hole;

   depositing a suitable electrically conductive material into the cavity and the via hole to form a conductive via having a first portion in the cavity and a second portion in the via hole, a diameter of the first portion different from a diameter of the second portion;

   conducting chemical mechanical polishing (CMP) on the front surface of the substrate after depositing the suitable electrically conductive material;

   forming a capping layer over the front surface of the substrate after conducting the chemical mechanical polishing (CMP);

   providing a passivation mask over the capping layer so that at least a portion of the capping layer is exposed;

   removing the portion of the capping layer and a portion of the substrate over a portion of the electrically conductive pad via etching so that the portion of the electrically conductive pad is exposed;

   removing a remaining portion of the capping layer to expose the conductive via; and

   forming a redistribution layer over the front surface of the substrate, the redistribution layer connecting the electrically conductive pad and the conductive via,

wherein the redistribution layer comprises one or more electrically conductive lines to electrically connect the exposed portion of the electrically conductive pad and the exposed portion of the conductive via.

2. The method according to claim 1,

wherein a diameter of the first portion is greater than a diameter of the second portion.

3. The method according to claim 1, the method further comprising:

providing a through via mask over the one or more dielectric liner layers after forming the one or more dielectric liner layers to cover the inner surface of the cavity and before forming the via hole so that the through via mask exposes at least a portion of the one or more dielectric liner layers covering a portion of a bottom surface of the cavity for subsequent forming of the via hole.

4. The method according to claim 3,

wherein forming the via hole comprises etching the portion of the one or more dielectric liner layers and the portion of the bottom surface of the cavity.

5. The method according to claim 1, further comprising:

depositing an oxide over the front surface of the substrate and conducting chemical mechanical polishing (CMP) on the deposited oxide to form a planarized cover oxide layer before forming the cavity such that the planarized cover oxide layer is over the electrically conductive pad; and

providing a cavity mask over the planarized cover oxide layer after forming the planarized cover oxide layer and before forming the cavity.

6. The method according to claim 5,

wherein the cavity mask exposes a portion of the planarized cover oxide layer over a portion of the electrically conductive pad for etching of the portion of the

planarized cover oxide layer and the portion of the electrically conductive pad to form the cavity.

7. The method according to claim 1,

wherein the suitable electrically conductive material is selected from a group consisting of copper, tungsten, and doped polysilicon.

8. The method according to claim 1 or claim 7, further comprising:

forming an under bump metallization on the redistribution layer;

wherein the under bump metallization is in contact with the one or more electrically conductive lines.

9. The method according to any one of claims 1 to 8, further comprising:

removing a portion of the substrate so that a back surface of the substrate opposite the front surface is formed to expose the conductive via.

10. The method according to claim 9, further comprising:

forming a backside metallization so that the backside metallization is in contact with the conductive via.

11. The method according to any one of claims 1 to 10,

wherein the electrically conductive pad comprises aluminum or copper.

12. The method according to any one of claims 1 to 11,

wherein the electrical connection structure is formed by a via last from top (VLFT) approach.

13. An electrical connection structure comprising:

an electrically conductive pad comprised in a substrate;

a cavity on a front surface of the substrate, the cavity extending through the electrically conductive pad;

one or more dielectric liner layers covering an inner surface of the cavity;

a via hole extending from the cavity through the one or more dielectric liner layers;

one or more further dielectric liner layers covering an inner surface of the via hole;

a conductive via comprising a suitable electrically conductive material, the conductive via having a first portion in the cavity and a second portion in the via hole, a diameter of the first portion different from a diameter of the second portion; and

a redistribution layer comprising one or more electrically conductive lines to electrically connect an exposed portion of the electrically conductive pad and an exposed portion of the conductive via.

14. The electrical connection structure according to claim 13,

wherein a diameter of the first portion is greater than a diameter of the second portion.

15. The electrical connection structure according to claim 13 or claim 14,

wherein the conductive via extends from the front surface of the substrate to a back surface of the substrate opposite the front surface.

16. The electrical connection structure according to claim 13, further comprising:

a backside metallization so that the conductive via is between the backside metallization and the redistribution layer.

17. The electrical connection structure according to claim 16, further comprising:

one or more solder bumps in contact with the backside metallization.