



- (51) International Patent Classification:  
*H01L 21/304* (2006.01)
- (21) International Application Number:  
PCT/US2014/054273
- (22) International Filing Date:  
5 September 2014 (05.09.2014)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:  
14/038,164 26 September 2013 (26.09.2013) US
- (71) Applicant: MICRON TECHNOLOGY, INC. [US/US];  
Mail Stop 525, 8000 South Federal Way, Boise, Idaho  
83707-0006 (US).
- (72) Inventor: ALBINI, Giulio; 1924 South Teal Lane, Boise,  
Idaho 83706 (US).
- (74) Agents: PULLEY, Stephen, E. et al.; Traskbritt, 230  
South 500 East, Suite 300, P. O. Box 2550, Salt Lake City,  
Utah 84110-2550 (US).
- (81) Designated States (*unless otherwise indicated, for every  
kind of national protection available*): AE, AG, AL, AM,  
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,  
BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM,  
DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,  
HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR,  
KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG,  
MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM,  
PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC,  
SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN,  
TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) Designated States (*unless otherwise indicated, for every  
kind of regional protection available*): ARIPO (BW, GH,  
GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ,  
TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU,  
TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE,  
DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU,  
LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,

[Continued on next page]

- (54) Title: METHODS OF FORMING SEMICONDUCTOR DEVICES AND STRUCTURES WITH IMPROVED PLANARIZATION UNIFORMITY, AND RESULTING STRUCTURES AND SEMICONDUCTOR DEVICES

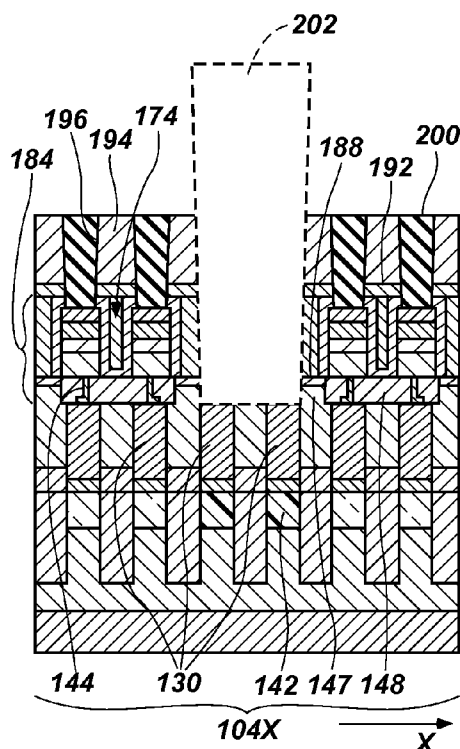


**FIG. 16B**

(57) Abstract: Semiconductor devices and structures, such as phase change memory devices, include peripheral conductive pads coupled to peripheral conductive contacts in a peripheral region. An array region may include memory cells coupled to conductive lines. Methods of forming such semiconductor devices and structures include removing memory cell material from a peripheral region and, thereafter, selectively removing portions of the memory cell material from the array region to define individual memory cells in the array region. Additional methods include planarizing the structure using peripheral conductive pads and/or spacer material over the peripheral conductive pads as a planarization stop material. Yet further methods include partially defining memory cells in the array region, thereafter forming peripheral conductive contacts, and thereafter fully defining the memory cells.



SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG). **Published:**

— *with international search report (Art. 21(3))*

**Declarations under Rule 4.17:**

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*