ENHANCEMENT OF DRY ETCH OF HIGH ASPECT RATIO FEATURES USING FLUORINE

FIELD OF THE INVENTION

(001) The present invention relates to processes and apparatus for the dry etching of silicon and particularly to the dry etching of high aspect ratio vias or holes in silicon substrates for use in semiconductor or other electronic devices.

BACKGROUND OF THE INVENTION

(002) The existing method for dry etching of high aspect ratio features, e.g. vias or holes, in silicon substrates, is know as the Bosch process. The Bosch process, also known as pulsed or time-multiplexed etching, was originally designed for use in MEMs etching, but has been used successfully in the formation of off-chip interconnect holes. The Bosch process employs repeated cycles of an alternating step process to achieve nearly vertical etched holes. The first step comprises a plasma etch, wherein plasma containing some ions that attack the silicon substrate in a nearly vertical direction is used. For silicon etching, the most common plasma ions are sulfur hexafluoride (SF_6). The second step in the Bosch process comprises deposition of a chemically inert passivation layer, most commonly using a C_4F_8 source gas. Each step lasts for several seconds. The passivation layer serves to protect the entire substrate from further chemical attack in subsequent etching steps. However, the directional ions bombard the substrate and etch through the passivation layer at the bottom of the hole formed by the prior etch step to ultimately expose and further etch the substrate. The passivation layer along the sides of the hole helps to protect against further etching and to create the vertical holes. Each cycle of etch and passivation results in a very small further etching at the bottom of the previously etched holes. After repeated cycles of etch and passivation, a high

aspect via can be achieved. These completed vias can then be lined with a dielectric layer; e.g. SiO_2, a metal barrier layer; e.g. Ta/TaN, and a copper seed layer. The vias are then completely filled with copper to serve as off-chip interconnects between dies.

(003) In an alternative to the Bosch process, known as the non-Bosch process or steady state process, etching and passivation are carried out in a continuous process until the entire via is etched, rather than the alternating cycles of the Bosch process. The etching gas for non-Bosch processes is the same, i.e. SF_6, but passivation gases are usually O_2 or HBr. For example, when using O_2 as the passivation gas, a layer of SiO_2 is formed on the sidewall of the via, which is more resistant to etch by SF_6 than the silicon substrate.

(004) While the Bosch process is generally useful in forming high aspect ratio holes or vias, it also exhibits a number of disadvantages. One such disadvantage is that the overall process for etching a hole can be relatively slow. In particular, because each etch and passivation cycle results in such a small etch, the cycles must be repeated numerous times. For example, in order to etch through a 0.5 mm silicon wafer, as many as a thousand cycles might be required. Vias are commonly in the range of 5 μm to 150 μm in diameter and have depths that vary from 30 μm to 300 μm. The aspect ratios for such vias can be as high as 20:1. Because each etch and passivation step is time consuming, and because many multiple cycles are required, a single via forming process can take several hours. This results in very low throughput and high costs.

(005) Another disadvantage of the Bosch process and of non-Bosch processes is scalloping of the sidewalls that is caused by undercutting from the isotropic etch process when using SF_6 as the etch gas. While the purpose of the passivation step is to protect against direct attack to the sidewalls of the deepening etch site, some damage occurs as plasma ions

collide with and sputter off of the sidewalls. This results in a scalloped or undulating profile for the sidewall. This can lead to non-conformal coating of subsequent passivation layers and therefore greater inconsistency in the via diameter. Ultimately, this can result in non-conformity of the dielectric layer, the metal barrier layer and the seed layer. This in turn leads to poor filling of the via with copper and to consequently higher interconnect electrical resistivity. Fluctuations in the diameter of the etched vias can be as much as 100 nm to 500 nm. While cycle times can be adjusted, this problem can not be completely overcome. Shorter cycle times can yield smoother walls, but require more etch cycles and consequently longer overall process times. Longer cycle times increase the etch rate and therefore reduce the overall process time, but result in more scalloping of the side walls.

(006) A further disadvantage of the Bosch and non-Bosch processes is the use of SF_6, which has been deemed to be a global warming gas. Therefore a reduction in the use of SF_6 is desirable.

(007) For all of the above reasons, there remains a need in the art for improvements to processes and apparatus for the dry etching of silicon and particularly to the dry etching of high aspect ratio vias in silicon substrates.

SUMMARY OF THE PRESENT INVENTION

(008) The present invention addresses the disadvantages noted above regarding the Bosch process and non-Bosch processes by the addition of F_2 gas into the etch chamber. The F_2 is highly reactive with silicon and reacts at the silicon surface in either its molecular state or in an activated state. By adding a small percentage of F_2 to the process, in either molecular state (thermally activated) or dissociated state (plasma) etch rates can be increased without degradation of the sidewalls of the via holes. It is believed that by adding F_2 during the etch step in the Bosch process or to the etch gas in a non-Bosch process several advantages can be achieved. For example,

the etch cycle can be significantly reduced and less undercutting occurs. Therefore, the amount of scalloping of the sidewalls is also reduced. This in turn leads to shorter overall process times and lower costs, without sacrifice of the integrity of the via being formed. Also, use of F_2 allows for a reduction in the use of SF_6.

DETAILED DESCRIPTION OF THE INVENTION

(009) The present invention provides advantages in the technology of dry etching of high aspect features; e.g. vias or holes, in a silicon substrate. In particular, the present invention provides improvements over the standard Bosch and non-Bosch processes and overcomes the disadvantages noted above with respect to such processes.

(010) The advantages of the present invention are accomplished by adding F_2 gas into the etch chamber. The addition of F_2 to the etch chamber can be done in accordance with several different embodiments. In one embodiment the F_2 gas is added with SF_6 into a plasma source as a percentage of the SF_6 flow rate. The sum of partial pressures of F_2 and SF_6 is maintained at the same level as that when using SF_6 gas alone. This results in a reduction in the amount of SF_6 used. In a further embodiment, SF_6 gas is completely replaced with a mixture of F_2 and a diluent gas such as N_2, Ar, He, etc. The F_2 and diluent gas are then supplied as the plasma source for etching. Another embodiment of the present invention combines F_2 in molecular state with either a diluent gases or with a reduced amount of plasma activated SF_6. A still further embodiment provides for the use of F_2 as the etchant gas and C_4F_8 or another fluorocarbon gas as the passivation gas. Other combinations using F_2 are also possible.

(011) As noted above, the use of F_2 in accordance with the present invention provides numerous advantages over the standard Bosch and non-Bosch processes. In particular, by using F_2 at least as a component of the etching

gas, etch rates can be increased. This increase of etch rate can be accomplished without degradation of the sidewalls of the via holes resulting in smooth via holes. The increased etch rate allows for shorter overall process times and corresponding lower processing costs. Moreover, the use of F_2 allows for a reduction or elimination of the use of SF_6. The reduction or elimination of SF_6 also reduces process costs, by reducing or eliminating the expense related to the abatement thereof. This will also help semiconductor manufacturing facilities meet the restrictions imposed by the Kyoto Protocol and guidelines established in the Chemical Restrictions Table of the International Technology Roadmap for Semiconductors.

(012) The present invention has been described with respect to improvements to the Bosch and non-Bosch processes for the etching of vias or holes in silicon substrates. The present invention may also be applied in plasma thinning of wafers where isotropic etching is required. The advantages for wafer thinning are again reduction of time and cost of the process as well as the reduction or elimination of the use of the global warming gas SF_6. In addition, the process of the present invention can be used to etch other films or stacks than the silicon substrate described. In particular, the present invention can be use for etching films of silicon dioxide, silicon nitride, doped silicon dioxide, low k dielectrics, copper, tungsten, silicon carbide and others. Etching of can be carried out on such films by themselves, in conjunction with silicon, or in a stack of various film layers.

(013) It is anticipated that other embodiments and variations of the present invention will become readily apparent to the skilled artisan in the light of the foregoing description, and it is intended that such embodiments and variations likewise be included within the scope of the invention as set out in the appended claims.

CLAIMS

What is claimed:

1. In a method of dry etching a substrate using an etching gas, the improvement comprising using F_2 gas as at least a portion of the etching gas.

2. A method according to claim 1 wherein the substrate is a silicon substrate or a silicon substrate having a layer of silicon dioxide, silicon nitride, doped silicon dioxide, low k dielectrics, copper, tungsten or silicon carbide thereon.

3. A method according to claim 1 wherein the etching gas is

4. A method according to claim 1 wherein the dry etching is a Bosch type process.

5. A method according to claim 1 wherein the dry etching is a non-Bosch type process.

6. A method according to claim 1 wherein the dry etching is a process of forming via holes in the substrate.

7. A method according to claim 1 wherein the dry etching is a process of thinning the substrate.

8. A method of etching via holes in a substrate comprising:
dry etching the substrate using etching gas having F_2 gas as at least a portion of the etching gas;
wherein the via holes formed have an aspect ration of 20:1.

9. A silicon substrate having via holes etched therein, said via holes having an aspect ration of 20:1.