Integrated Circuit Structure and Method of Fabrication

ABSTRACT OF THE DISCLOSURE

According to the present invention, the integrated circuit includes isolation field regions on a semiconductor substrate. Gate dielectrics are formed on a surface of a substrate. Gate electrodes are formed on the gate dielectrics. A photo resist is formed covering the active regions. Dummy patterns are selectively etched. A dummy substrate is selectively etched. The photo resist is then removed. A pair of spacers is formed along opposite sidewalls of the gate electrode and the gate dielectric. The source and drain are formed on the surface of said substrate and on opposite sides of the gate. Silicide is formed on the gate electrode, source, and drain. A layer of inter-level dielectric is then formed. A contact opening and metal wiring are then formed.

Fig. 2