trapped charge carriers possibly originating from the trapping layer itself or from the subjacent carrier substrate. In this way, the appearance of the conductive plane under the electrically insulating layer and the drop in the resistivity of the carrier substrate are prevented.

However, the effectiveness of such a charge-trapping layer is not always optimal, and the effects of coupling loss and of generation of unwanted harmonics may nevertheless occur.

In particular, the polysilicon layer, which makes contact with the carrier substrate, which is made of single-crystal silicon, has a tendency to recrystallize under the effect of heat treatments applied to the substrate during its fabrication and the fabrication of the radio-frequency components. Specifically, the carrier substrate serves as a seed for the recrystallization. The recrystallization of the polysilicon layer, as it reduces the number of grains, also reduces the capacity of said layer to trap electric charge.

BRIEF DESCRIPTION OF THE INVENTION

One goal according to embodiments of the invention is to provide a semiconductor-on-insulator substrate that allows the aforementioned drawbacks to be overcome.

Embodiments of the invention aim to provide such a substrate allowing interactions between mobile charge carriers in the substrate and the electromagnetic fields generated by the radio-frequency components of the active layer to be limited.

Embodiments of the invention therefore aim to limit or even prevent the effects of the coupling loss between the radio frequency components and the substrate, and generation of unwanted harmonics.

An aspect of the invention provides a semiconductor-on-insulator substrate for radio-frequency applications, comprising:

- a silicon carrier substrate,
- an electrically insulating layer arranged on the carrier substrate,
- a single-crystal layer arranged on the electrically insulating layer,

the substrate mainly being characterized in that it further comprises a layer of silicon carbide SiC arranged between the carrier substrate and the electrically insulating layer, which has a thickness comprised between 1 nm and 5 nm, the surface of the layer of silicon carbide SiC that is on the side of the electrically insulating layer having a roughness higher than or equal to 10 nm RMS.

The presence of a rough SiC layer allows the drop in resistivity usually observed at the interface between the carrier substrate and the charge-trapping layer to be limited, and a semiconductor-on-insulator substrate that has a better radio-frequency performance to be obtained.

A thickness comprised between 1 nm and 5 nm for the rough SiC layer allows the level of roughness due to the level of roughness of the carrier substrate on which it rests to be reproduced, and thus the surface area of this SiC layer to be maximized.

According to example embodiments, the substrate has the various following features, either implemented alone or in technically possible combinations thereof:

- the single-crystal layer is a semiconductor layer, i.e. it comprises a semiconductor;
- the single-crystal layer is a ferroelectric layer, i.e. it comprises a ferroelectric material. Preferably, the ferroelectric material is chosen from: $LiTaO_3$, $LiNbO_3$, $LiAlO_3$, $BaTiO_3$, $PbZrTiO_3$, $KNbO_3$, $BaZrO_3$, $CaTiO_3$, $PbTiO_3$, $KTaO_3$.
- the surface of the silicon-carbide layer has a roughness higher than or equal to 10 nm RMS, and preferably higher than or equal to 100 nm RMS;
- the substrate further comprises a polysilicon charge-trapping layer arranged between the silicon-carbide layer and the electrically insulating layer;
- the carrier substrate is single-crystal;
- the electrically insulating layer is a silicon-oxide layer.

Another aspect of the invention provides a process for fabricating a semiconductor-on-insulator substrate for radio-frequency applications, mainly characterized in that it comprises the following steps:

- providing a silicon carrier substrate,
- roughening a free surface of the carrier substrate via a selective etch,
- forming a silicon-carbide layer on the roughened surface, a surface of the silicon-carbide layer that is on the side opposite the carrier substrate having a roughness higher than or equal to 10 nm RMS,
- forming a bonding layer on the rough surface of the silicon-carbide layer,
- transferring an electrically insulating layer and a single-crystal layer to the bonding layer, the electrically insulating layer being at the interface with the bonding layer.

The etch is said to be “selective” in that the silicon from which the carrier substrate is made is not etched uniformly over the entire free surface of the carrier substrate, privileged regions of this surface (corresponding to particular crystal planes) being etched faster than other regions. In this way, the roughening operation is controlled.

The parameterization of the selective etch allows the depth desired for the cavities formed in the thickness of the carrier substrate, from its free surface, to be selected and adjusted, and therefore the roughness expected for the surface of the subsequently formed SiC layer to be adjusted.

According to example embodiments, the process has the various following features, either implemented alone or in technically possible combinations thereof:

CLAIMS

1. A semiconductor-on-insulator substrate for radio-frequency applications, comprising:
- a silicon carrier substrate,
- an electrically insulating layer arranged on the carrier substrate,
- a single-crystal layer arranged on the electrically insulating layer,
the substrate being characterized in that it further comprises a layer of silicon carbide SiC arranged between the carrier substrate and the electrically insulating layer, which has a thickness comprised between 1 nm and 5 nm, the surface of the layer of silicon carbide SiC that is on the side of the electrically insulating layer having a roughness higher than or equal to 10 nm RMS.

2. The substrate as claimed in claim 1, wherein the single-crystal layer is a semiconductor layer.

3. The substrate as claimed in claim 1, wherein the single-crystal layer comprises a ferroelectric material.

4. The substrate as claimed in claim 3, wherein the ferroelectric material is chosen from: $LiTaO_3$, $LiNbO_3$, $LiAlO_3$, $BaTiO_3$, $PbZrTiO_3$, $KNbO_3$, $BaZrO_3$, $CaTiO_3$, $PbTiO_3$, $KTaO_3$.

5. The substrate as claimed in one of the preceding claims, further comprising a polysilicon charge-trapping layer arranged between the silicon-carbide layer and the electrically insulating layer.

6. The substrate as claimed in one of the preceding claims, wherein the carrier substrate is single-crystal.

7. The substrate as claimed in one of the preceding claims, wherein the electrically insulating layer is a silicon-oxide layer.

8. A process for fabricating a semiconductor-on-insulator substrate for radio-frequency applications, characterized in that it comprises the following steps:
- providing a silicon carrier substrate,
- roughening a free surface of the carrier substrate via a selective etch,
- forming a silicon-carbide layer on the roughened surface, a surface of the silicon-carbide layer that is on the side opposite the carrier substrate having a roughness higher than or equal to 10 nm RMS,

- forming a bonding layer on the rough surface of the silicon-carbide layer,
- transferring an electrically insulating layer and a single-crystal layer to the bonding layer, the electrically insulating layer being at the interface with the bonding layer.

9. The fabricating process as claimed in claim 8, wherein the single-crystal layer is a semiconductor layer.

10. The fabricating process as claimed in claim 8, wherein the single-crystal layer comprises a ferroelectric material.

11. The fabricating process as claimed in claim 10, wherein the ferroelectric material is chosen from: $LiTaO_3$, $LiNbO_3$, $LiAlO_3$, $BaTiO_3$, $PbZrTiO_3$, $KNbO_3$, $BaZrO_3$, $CaTiO_3$, $PbTiO_3$, $KTaO_3$.

12. The fabricating process as claimed in one of claims 8 to 11, wherein the roughening step comprises a selective etch along crystal planes of the free surface of the carrier substrate.

13. The fabricating process as claimed in one of claims 8 to 11, wherein the roughening step comprises:
- nucleating silicon-carbide islands on the free surface of the carrier substrate by exposing said free surface to a precursor gas containing carbon-containing chemical species so as to cause a reaction of said carbon-containing chemical species with the silicon of the carrier substrate,
- carrying out the selective etch of regions of the free surface of the carrier substrate separating the islands.

14. The fabricating process as claimed in claim 12 or claim 13, wherein the selective etch is a dry etch.

15. The fabricating process as claimed in claim 14, wherein the dry etch is carried out with hydrochloric acid.

16. The fabricating process as claimed in one of claims 8 to 15, wherein the silicon-carbide layer is formed by exposing said roughened surface to a precursor gas containing carbon-containing chemical species so as to cause a reaction of said carbon-containing chemical species with the silicon of the carrier substrate.

17. The fabricating process as claimed in one of claims 8 to 16, wherein the silicon-carbide layer on the roughened surface of the carrier substrate is formed by chemical vapor deposition.

18. The fabricating process as claimed in one of claims 8 to 17, further comprising, before the electrically insulating layer and the single-crystal layer are transferred, depositing a polysilicon charge-trapping layer on the silicon-carbide layer.

19. The process as claimed in one of claims 8 to 17, wherein the transferring step comprises:

- providing a donor substrate covered with an electrically insulating layer,
- forming a weakened region in the donor substrate, so as to define a single-crystal layer,
- bonding the donor substrate to the carrier substrate via the electrically insulating layer and the bonding layer,
- detaching the donor substrate along the weakened region, so as to transfer the single-crystal layer to the carrier substrate.