

CLAIMS

What is claimed is:

1. A method of making a semiconductor device, comprising:
providing a plurality of semiconductor die comprising a copper column disposed over the active surface of each of the semiconductor die;
forming an embedded die panel by disposing an encapsulant around each of the semiconductor die;
measuring a true position of each semiconductor die within the embedded die panel; and
forming a unit-specific pattern to align with the true position of each semiconductor die in the embedded die panel.
2. The method of claim 1, further comprising forming the embedded die panel by:
providing a carrier;
mounting the plurality of semiconductor die face down on the carrier; and
disposing the encapsulant around each of the plurality of semiconductor die and around each copper column.
3. The method of claim 1, further comprising forming the embedded die panel by:
providing a carrier;
mounting the plurality of semiconductor die face up on the carrier; and
disposing the encapsulant around each of the plurality of semiconductor die and around each copper column.
4. The method of claim 3, further comprising removing the carrier to expose a backside of each semiconductor die.
5. The method of claim 1, further comprising:
forming a fan-in redistribution layer (RDL) extending over the active surface of each semiconductor die; and
forming the copper columns over the fan-in RDL.

6. The method of claim 1, further comprising forming the unit-specific pattern as a fan-out structure disposed over the plurality of semiconductor die, over the encapsulant, and coupled to the copper columns.
7. The method of claim 1, further comprising forming the unit-specific pattern as a conductive layer directly on the encapsulant and coupled to the copper columns.
8. A method of making a semiconductor device, comprising:
 - providing a plurality of semiconductor die comprising an interconnect structure disposed over the active surface of each semiconductor die;
 - forming an embedded die panel by disposing an encapsulant around each of the plurality of semiconductor die;
 - measuring a true position of each semiconductor die within the embedded die panel; and
 - forming a unit-specific pattern to align with the true position of each semiconductor die in the embedded die panel.
9. The method of claim 8, wherein providing the interconnect structures further comprises forming the interconnect structures as copper columns.
10. The method of claim 9, further comprising forming bumps over each copper column such that the bumps align with a respective outline of each semiconductor device.
11. The method of claim 9, further comprising:
 - forming each of the semiconductor die comprising a contact pad; and
 - forming the copper columns over the contact pads of each of the respective semiconductor die.
12. The method of claim 8, further comprising forming a backside coating over a backside of each of the plurality of semiconductor die before forming the encapsulant around the semiconductor die.

13. The method of claim 8, further comprising disposing a backside coating over a backside of each of the plurality of semiconductor die and over a surface of the encapsulant disposed around the plurality of semiconductor die.
14. The method of claim 8, further comprising measuring the true position of each semiconductor die with respect to a global fiducial.
15. A method of making a semiconductor device, comprising:
providing a die panel comprising a plurality of semiconductor die comprising interconnect structures and embedded in an encapsulant;
measuring a true position of each semiconductor die within the die panel; and
forming a unit-specific pattern aligned with the true position of each interconnect structure.
16. The method of claim 15, further comprising forming the encapsulant around the semiconductor die without forming the encapsulant over backsides of the semiconductor die such that the backsides of the semiconductor die are exposed with respect to the encapsulant.
17. The method of claim 15, further comprising forming the unit-specific patterns to align with the true position of each semiconductor die in the die panel by selecting from a number of pre-determined unit-specific pattern designs a unit-specific pattern with a best fit for the true position of each of the plurality of semiconductor die.
18. The method of claim 15, further comprising forming bumps over each unit-specific pattern such that the bumps align with a respective outline of each semiconductor device.
19. The method of claim 15, wherein providing the interconnect structures further comprises forming the interconnect structures as copper columns.
20. The method of claim 19, further comprising:
forming the unit-specific pattern as a conductive layer;

forming an insulating layer of polybenzoxazoles, polyimide, or epoxy solder mask over the unit-specific pattern;

forming openings in the insulating layer over the unit-specific pattern to define land grid array pads; and

forming low profile bumps over the land grid array pads.

Claims

1. A method of making a plurality of semiconductor packages, comprising:
providing a plurality of semiconductor die comprising a copper column disposed over the active surface of each of the semiconductor die;
forming an embedded die panel by disposing an encapsulant around each of the semiconductor die;
measuring a true position of each semiconductor die within the embedded die panel;
and
forming a plurality of unit-specific patterns over the plurality of semiconductor die and on a surface of the embedded die panel using a mask-less patterning system to align one of the plurality of unit-specific patterns with the true position of each semiconductor die in the embedded die panel; and
singulating the embedded die panel to form the plurality of semiconductor packages comprising semiconductor die and unit-specific patterns over the semiconductor die.
2. The method of claim 1, further comprising forming the embedded die panel by:
providing a carrier;
mounting the plurality of semiconductor die face down on the carrier; and
disposing the encapsulant around each of the plurality of semiconductor die and around each copper column.
3. The method of claim 1, further comprising forming the embedded die panel by:
providing a carrier;
mounting the plurality of semiconductor die face up on the carrier; and

disposing the encapsulant around each of the plurality of semiconductor die and around each copper column.

4. The method of claim 3, further comprising removing the carrier to expose a backside of each semiconductor die.

5. The method of claim 1, further comprising:

forming a fan-in redistribution layer (RDL) extending over the active surface of each semiconductor die; and

forming the copper columns over the fan-in RDL.

6. The method of claim 1, further comprising forming the unit-specific pattern as a fan-out structure disposed over the plurality of semiconductor die, over the encapsulant, and coupled to the copper columns.

7. The method of claim 1, further comprising forming the unit-specific pattern as a unique unit-specific pattern comprising a conductive layer formed over the encapsulant and coupled to the copper columns.

8. A method of making a plurality of semiconductor packages, comprising:

providing a plurality of semiconductor die comprising an interconnect structure disposed over the active surface of each semiconductor die;

forming an embedded die panel by disposing an encapsulant around each of the plurality of semiconductor die;

measuring a true position of each semiconductor die within the embedded die panel;

and

forming a unit-specific pattern over each of the semiconductor die with a mask-less patterning system to align each of the unit-specific patterns with the true position of each respective semiconductor die in the embedded die panel; and

singulating the embedded die panel to form the plurality of semiconductor packages.

9. The method of claim 8, wherein providing the interconnect structures further comprises forming the interconnect structures as copper columns.

10. The method of claim 8, further comprising forming bumps over each of the interconnect structures such that the bumps align with a respective outline of each of the semiconductor packages.

11. The method of claim 9, further comprising:
forming each of the semiconductor die comprising a contact pad; and
forming the copper columns over the contact pads of each of the respective semiconductor die.

12. The method of claim 8, further comprising forming a backside coating over a backside of each of the plurality of semiconductor die before forming the encapsulant around the semiconductor die.

13. The method of claim 8, further comprising disposing a backside coating over a backside of each of the plurality of semiconductor die and over a surface of the encapsulant disposed around the plurality of semiconductor die.

14. The method of claim 8, further comprising measuring the true position of each semiconductor die with respect to a global fiducial.
15. A method of making a semiconductor package, comprising:
providing a die panel comprising a semiconductor die embedded in an encapsulant with an interconnect structure coupled to an active surface of the semiconductor die;
measuring a true position of the interconnect structure within the die panel; and
forming a unit-specific pattern over the semiconductor die with a mask-less patterning system to align the unit-specific pattern with the true position of the interconnect structure.
16. The method of claim 15, further comprising forming the encapsulant around the semiconductor die without forming the encapsulant over backsides of the semiconductor die such that the backsides of the semiconductor die are exposed with respect to the encapsulant.
17. The method of claim 15, further comprising forming the unit-specific patterns to align with the true position of each semiconductor die in the die panel by selecting from a number of pre-determined unit-specific pattern designs a unit-specific pattern with a best fit for the true position of each of the plurality of semiconductor die.
18. The method of claim 15, further comprising forming a bump over the unit-specific pattern such that the bump is aligned with an outline of the semiconductor package.
19. The method of claim 15, wherein providing the interconnect structures further comprises forming the interconnect structures as copper columns.

20. The method of claim 19, further comprising:

forming the unit-specific pattern as a conductive layer;

forming an insulating layer of polybenzoxazoles, polyimide, or epoxy solder mask over the unit-specific pattern;

forming openings in the insulating layer over the unit-specific pattern to define land grid array pads; and

forming low profile bumps over the land grid array pads.