A METHOD TO FORM A SELF-ALIGNED CMOS INVERTER USING VERTICAL DEVICE INTEGRATION

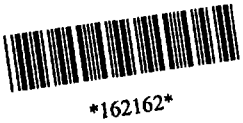
ABSTRACT

A method to form a closely-spaced, vertical NMOS and PMOS transistor pair in an integrated circuit device is achieved. A substrate comprises silicon implanted oxide (SIMOX) wherein an oxide layer is sandwiched between underlying and overlying silicon layers. Ions are selectively implanted into a first part of the overlying silicon layer to form a drain, channel region, and source for an NMOS transistor. The drain is formed directly overlying the oxide layer, the channel region is formed overlying the drain, and the source is formed overlying the channel region. Ions are selectively implanted into a second part of the overlying silicon layer to form a drain, channel region, and source for a PMOS transistor. The drain is formed directly overlying the oxide layer, the PMOS channel region is formed overlying the drain, and the source is formed overlying the channel region. The PMOS transistor drain is in contact with said NMOS transistor drain. A gate trench is etched through the NMOS and PMOS sources and channel regions. The gate trench terminates at the NMOS and PMOS drains and exposes the sidewalls of the NMOS and PMOS channel regions. A gate oxide layer is formed overlying the NMOS and PMOS channel regions and lining the gate trench. A polysilicon layer is deposited and etched back to form polysilicon sidewalls and to thereby form gates for the closely-spaced, vertical NMOS and PMOS transistor pair.

FIGURE 4



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