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(54) **Title:** SPECULATIVE TRANSITIONS AMONG MODES WITH DIFFERENT PRIVILEGE LEVELS IN A BLOCK-BASED MICROARCHITECTURE

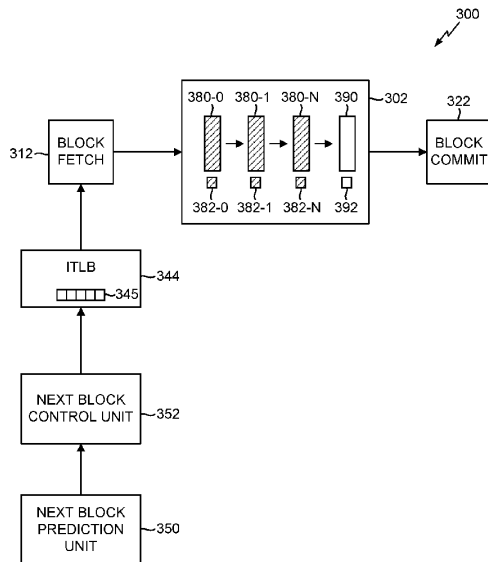


FIG. 3

(57) **Abstract:** The disclosure relates to processing in-flight blocks in a processor pipeline according to an expected execution mode to reduce synchronization delays that could otherwise arise due to transitions among processor modes with varying privilege levels (e.g., user mode, supervisor mode, hypervisor mode, etc.). More particularly, a program counter associated with an instruction block to be fetched may be translated to one or more execute permissions associated with the instruction block and the instruction block may be associated with a speculative execution mode based at least in part on the one or more execute permissions. Accordingly, the instruction block may be processed relative to the speculative execution mode while in-flight within the processor pipeline.

[Continued on next page]

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