CLAIMS

WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

a first package substrate;

a first semiconductor device on the first package substrate;

a second package substrate on an upper part of the first semiconductor device, the second package substrate including a conductor; and

a heat-dissipating material layer between the first semiconductor device and the second package substrate, the heat-dissipating material layer having a thermal conductivity of 0.5 W/m·K to 20 W/m·K, and the heat-dissipating material layer being in direct contact with an upper surface of the first semiconductor device and the conductor of the second package substrate,

wherein the first semiconductor device is connected to the first package substrate via a first connection terminal.

2. The semiconductor package of claim 1, wherein the second package substrate includes:

a lower pad connected to the first package substrate through a second connection terminal, the lower pad on a first surface of the second package substrate facing the first semiconductor device;

a lower wiring on the first surface of the second package substrate, the lower wiring not connected to the first package substrate through the second connection terminal; and

a lower insulator layer on the first surface of the second package substrate, the lower insulator layer exposing the lower pad and the lower wiring therethrough.

3. The semiconductor package of claim 2, wherein the conductor of the second package substrate is the lower wiring of the second package substrate.

4. The semiconductor package of claim 2 or claim 3, wherein

an exposed portion of the lower wiring is exposed through an opening in the lower insulator layer, and

the heat-dissipating material layer contacts the lower wiring over an entire area of the exposed portion of the lower wiring exposed.

5. The semiconductor package of any one of claims 2 to 4, wherein

the lower insulator layer includes a plurality of openings that expose a lower surface of the lower wiring, and

the heat-dissipating material layer contacts the lower wiring through the plurality of openings.

6. The semiconductor package of claim 4, wherein the lower insulator layer includes:

a first part encompassing a periphery of the opening; and

a second part in a form of islands encompassed by and spaced apart from the first part, and

the opening is defined by the first part and the second part.

7. The semiconductor package of any one of claims 2 to 6, wherein a dimension of the lower wiring in a direction parallel to a lower surface of the second package substrate is 2.5 times to 100 times a dimension of the lower pad.

8. The semiconductor package of any one of claims 2 to 6, wherein a plan area of the lower wiring projected onto a lower surface of the second package substrate is 5 times to 10,000 times a plan area of the lower pad.

9. The semiconductor package of any one of claims 2 to 8, wherein the lower wiring includes a perforated portion passing through the lower wiring.

10. The semiconductor package of claim 9, wherein the lower wiring includes two or more perforated portions.

11. The semiconductor package of any one of claims 2 to 10, wherein the lower wiring includes:

a plurality of first extension portions extending in a first direction; and

a plurality of second extension portions overlapping the first extension portions and extending in a second direction.

12. The semiconductor package of any one of claims 1 to 11, wherein

the heat-dissipating material layer includes a polymer matrix and insulating inorganic particles dispersed in the polymer matrix, and

the insulating inorganic particles include at least one of a metal oxide, a metalloid oxide, a metal nitride, and a metalloid nitride.

13. The semiconductor package of any one of claims 1 to 11, wherein

the heat-dissipating material layer includes a polymer matrix and insulating inorganic particles dispersed in the polymer matrix, and

the insulating inorganic particles include silica, a silicon nitride, a silicon carbide, alumina, titania, zirconia, ceria, an aluminum nitride (AlN), a boron nitride (BN), or nano-diamond.

14. A package-on-package (PoP) type package comprising:

a first package, the first package including a first semiconductor device on a first package substrate;

a second package on an upper part of the first package,

the second package including a second semiconductor device on a second package substrate, the second package substrate being between the first semiconductor device and the second semiconductor device,

the second package substrate including a core layer, an upper wiring extending on an upper surface of the core layer, a lower wiring extending on a lower surface of the core layer, an upper insulator layer covering the upper surface of the core layer and at least a portion of the upper wiring, and a lower insulator layer covering the lower surface of the core layer and at least a portion of the lower wiring, the lower insulator layer at least partially exposing the lower wiring to provide an exposed lower wiring; and

a heat-dissipating material layer in physical contact with the exposed lower wiring through the lower insulator layer and an upper surface of the first semiconductor device,

wherein the first semiconductor device is connected to the first package substrate via a first connection terminal.

15. The PoP type package of claim 14, further comprising:

a second connection terminal connecting the first package substrate to the second package substrate in a side direction of the first semiconductor device,

wherein the second package substrate further includes a lower terminal in contact with the second connection terminal at a lower part of the core layer, and

the first package substrate includes an upper terminal in contact with the second connection terminal.

16. The PoP type package of claim 15, wherein the heat-dissipating material layer encompasses a side surface of the second connection terminal.

17. The PoP type package of any one of claims 14 to 16, wherein a side surface of the heat-dissipating material layer is coplanar with a side surface of the first package substrate.

18. The PoP type package of claim 17, wherein a side surface of the second package substrate is coplanar with the side surface of the heat-dissipating material layer.

19. The PoP type package of any one of claims 14 to 18, wherein

the first semiconductor device is a logic chip, and

the second semiconductor device is a memory chip.

20. A package-on-package (PoP) type package comprising:

a first package,

the first package including a first semiconductor device on a first package substrate,

the first package substrate including a first core layer, a first upper pad on an upper part of the first core layer, and a first lower pad on a lower part of the first core layer, and

a second package on an upper part of the first package, the second package including a second semiconductor device on a second package substrate, the second package substrate being between the first semiconductor device and the second semiconductor device,

the second package substrate including a second core layer, a second upper pad on an upper part of the second core layer, a second lower pad on a lower part of the second core layer,

a lower wiring extending on the lower part of the second core layer, a lower insulator layer forming a lower surface of the second package substrate while exposing the lower wiring at least partially to provide an exposed lower wiring; and

a heat-dissipating material layer between the first package substrate and the second package substrate,

the heat-dissipating material layer including insulating inorganic particles dispersed in a polymer matrix,

a thermal conductivity of the insulating inorganic particles being 10 times a thermal conductivity of the lower insulator layer or greater, and

the heat-dissipating material layer being in physical contact with the exposed lower wiring of the second package substrate and an upper surface of the first semiconductor device,

wherein the first semiconductor device is connected to the first package substrate via a first connection terminal.