CLAIMS

1. A modular semiconductive device, comprising:

an at least partially embedded multi-die interconnect bridge (EMIB) in an opening in a glass substrate, wherein the glass substrate includes a die side and a land side, and wherein the glass substrate is an inorganic substrate;

a dielectric film disposed over the die side of the glass substrate, over the EMIB, and in the opening in the glass substrate;

a first plurality of through-glass vias (TGVs) that communicate from the die side to the land side;

a first semiconductive device coupled to the EMIB and to at least one first TGV of a plurality of TGVs, wherein the first semiconductive device includes a first plurality of substrate bond pads that couple to the at least one first TGV, and at least one first EMIB bond pad that couples to the EMIB, and wherein the first semiconductive device has an active surface facing away from the EMIB; and

a subsequent semiconductive device coupled to the EMIB and to at least one second TGV of the plurality of TGVs, wherein the subsequent semiconductive device includes a second plurality of substrate bond pads that couple to the at least one second TGV, and at least one second EMIB bond pad that couples to the EMIB, and wherein the subsequent semiconductive device has an active surface facing away from the EMIB.

2. The modular semiconductive device of claim 1, further including at least one first chiplet coupled to the first semiconductive device, wherein the at least one first chiplet is on the active surface of the first semiconductive device.

3. The modular semiconductive device of claim 1, further including:

at least one first chiplet coupled to the first semiconductive device, wherein the at least one first chiplet is on the active surface of the first semiconductive device; and

at least one subsequent chiplet coupled to the first semiconductive device, wherein the at least one subsequent chiplet is on the active surface of the first semiconductive device.

4. The modular semiconductive device of claim 1, further including:

at least one first chiplet coupled to the first semiconductive device, wherein the at least one first chiplet is on the active surface of the first semiconductive device;

at least one subsequent chiplet coupled to the first semiconductive device, wherein the at least one subsequent chiplet is on the active surface of the first semiconductive device; and

at least one heat slug on the active surface of the first semiconductive device.

5. The modular semiconductive device of claim 1, further including:

at least one first chiplet coupled to the subsequent semiconductive device, wherein the at least one first chiplet is on the active surface of the subsequent semiconductive device; and

at least one subsequent chiplet coupled to the subsequent semiconductive device, wherein the at least one subsequent chiplet is on the active surface of the subsequent semiconductive device.

6. The modular semiconductive device of claim 1, further including:

at least one first chiplet coupled to the subsequent semiconductive device, wherein the at least one first chiplet is on the active surface of the subsequent semiconductive device;

at least one subsequent chiplet coupled to the subsequent semiconductive device, wherein the at least one subsequent chiplet is on the active surface of the subsequent semiconductive device; and

at least one heat slug on the active surface of the subsequent semiconductive device.

7. The modular semiconductive device of claim 1, further including:

at least one first chiplet coupled to the first semiconductive device, wherein the at least one first chiplet is on the active surface of the first semiconductive device; and

at least one subsequent chiplet coupled to the subsequent semiconductive device, wherein the at least one subsequent chiplet is on the active surface of the subsequent semiconductive device.

8. The modular semiconductive device of claim 1, wherein the first semiconductive device contacts the first plurality of substrate bond pads, the one substrate bond pad contacts a solder film, the solder film contacts a die-level via, the die-level via contacts a second-level via, and the second-level via contacts the one TGV of the plurality of TGVs.

9. The modular semiconductive device of claim 1, wherein the glass substrate has a first Z-height, and wherein the EMIB has a second Z-height that is within 96 percent of the first Z-height of the glass-substrate.

10. The modular semiconductive device of claim 1, wherein the opening in the glass substrate is a through-hole in the glass substrate.

11. The modular semiconductive device of claim 1, wherein the opening in the glass substrate is a recess in the glass substrate.

12. The modular semiconductive device of claim 1, further including a semiconductor package substrate bonded to the at least one first TGV and the at least one second TGV of the plurality of TGVs.

13. The modular semiconductive device of claim 1, further including:

a semiconductor package substrate bonded to the at least one first TGV and the at least one second TGV of the plurality of TGVs; and

a printed wiring board bonded to the semiconductor package substrate.

14. The modular semiconductive device of claim 1, further including:

a semiconductor package substrate bonded to the at least one first TGV and the at least one second of the plurality of TGVs;

a printed wiring board bonded to the semiconductor package substrate;

at least one first chiplet coupled to the first semiconductive device, wherein the at least one first chiplet is on the active surface of the first semiconductive device; and

at least another first chiplet coupled to the subsequent semiconductive device, wherein the at least another first chiplet is on the active surface of the subsequent semiconductive device.

15. The modular semiconductive device of claim 1, further including:

a semiconductor package substrate bonded to the at least one first TGV and the at least one second of the plurality of TGVs;

a printed wiring board bonded to the semiconductor package substrate;

a first chiplet coupled to the first semiconductive device, wherein the first chiplet is on the active surface of the first semiconductive device;

a subsequent chiplet coupled to the first semiconductive device, wherein the subsequent chiplet is on the active surface of the first semiconductive device;

an another first chiplet coupled to the subsequent semiconductive device, wherein the first chiplet is on the active surface of the subsequent semiconductive device; and

an another subsequent chiplet coupled to the subsequent semiconductive device, wherein the subsequent chiplet is on the active surface of the subsequent semiconductive device.

16. A semiconductor device package, comprising:

an at least partially embedded multi-die interconnect bridge (EMIB) in an opening in a glass substrate, wherein the glass substrate includes a die side and a land side, and wherein the glass substrate is an inorganic material;

a dielectric film disposed over the die side of the glass substrate, over the EMIB, and in the opening in the glass substrate;

a first plurality of through-glass vias (TGVs) that communicate from the die side to the land side;

a first semiconductive device coupled to the EMIB and to at least one first TGV of a plurality of TGVs, wherein the first semiconductive device includes a first plurality of substrate bond pads that couple to the at least one first TGV, and at least one first EMIB bond pad that couples to the EMIB, and wherein the first semiconductive device has an active surface facing away from the EMIB;

a subsequent semiconductive device coupled to the EMIB and to at least one second TGV of the plurality of TGVs, wherein the subsequent semiconductive device includes a second plurality of substrate bond pads that couple to the at least one second TGV, and at least one second EMIB bond pad that couples to the EMIB, and wherein the subsequent semiconductive device has an active surface facing away from the EMIB;

a semiconductor package substrate bonded to the plurality of TGVs, wherein the first semiconductive device and the subsequent semiconductive device are electrically coupled to the semiconductor package substrate;

at least one first chiplet coupled to the first semiconductive device, wherein the at least one first chiplet is on the active surface of the first semiconductive device; and

at least another first chiplet coupled to the subsequent semiconductive device, wherein the at least another first chiplet is on the active surface of the subsequent semiconductive device.

17. The semiconductor device package of claim 16, further including:

a printed wiring board bonded to the semiconductor package substrate;

at least one heat slug on the active surface of the first semiconductive device; and

at least one heat slug on the active surface of the subsequent semiconductive device.

18. The semiconductor device package of claim 16, further including:

a printed wiring board bonded to the semiconductor package substrate;

an external shell that is a part of the printed wiring board, wherein the external shell is an outer surface of a hand-held computing system;

at least one heat slug on the active surface of the first semiconductive device; and at least one heat slug on the active surface of the subsequent semiconductive device.

19. The semiconductor device package of claim 16, wherein the first semiconductive device is a part of a chipset.