



SG 9701737-0

## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

|                                                                                                           |    |                                                                                                                   |
|-----------------------------------------------------------------------------------------------------------|----|-------------------------------------------------------------------------------------------------------------------|
| (51) International Patent Classification <sup>5</sup> :<br>H01L 23/053, 23/12, 23/48, 23/52, 21/76, 21/48 | A1 | (11) International Publication Number: WO 96/15552<br>(43) International Publication Date: 23 May 1996 (23.05.96) |
|-----------------------------------------------------------------------------------------------------------|----|-------------------------------------------------------------------------------------------------------------------|

(21) International Application Number: PCT/US95/14681

(22) International Filing Date: 13 November 1995 (13.11.95)

(30) Priority Data:  
08/337,000 10 November 1994 (10.11.94) US

(71) Applicant: INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).

(72) Inventors: MOON, Peter, K.; 4901 S.W. 26th Drive, Portland, OR 97201 (US). SARANGI, Ananda, G.; 16795 S.W. Ivy Glenn Street, Beaverton, OR 97007 (US). DEETER, Timothy, L.; 3359 N.W. 125th Place, Portland, OR 97229 (US).

(74) Agents: BEREZNAK, Bradley, J. et al.; Blakely, Sokoloff, Taylor &amp; Zafman, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025-1026 (US).

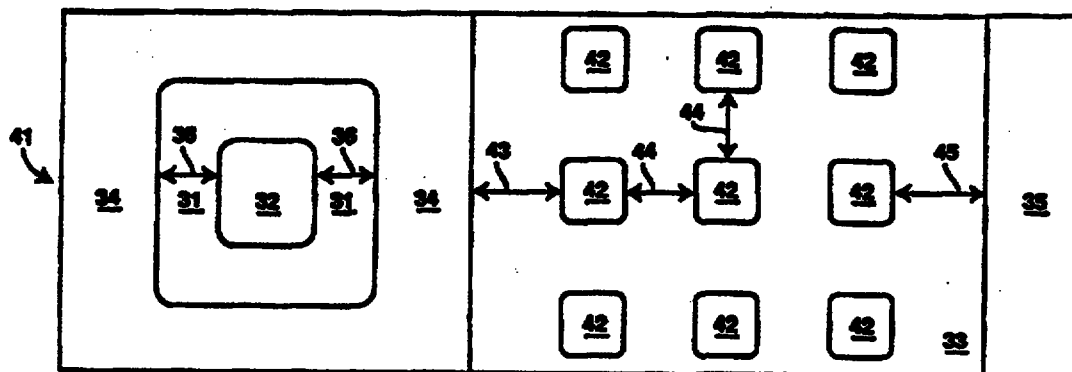
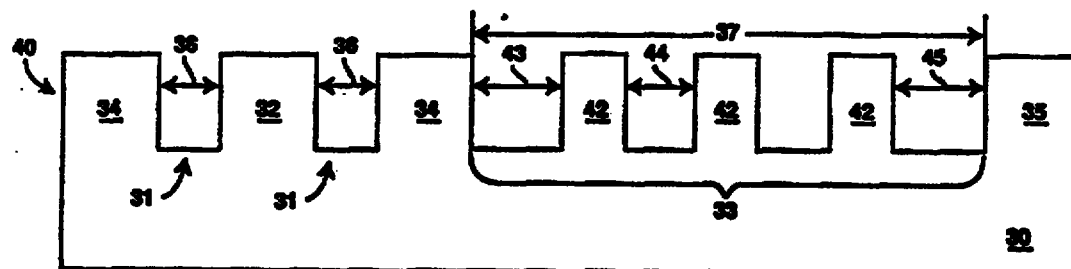
(81) Designated States: AL, AM, AT, AT (Utility model), AU, BB, BG, BR, BY, CA, CH, CN, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, HU, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), TJ, TM, TT, UA, UG, UZ, VN, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG), ARIPO patent (KE, LS, MW, SD, SZ, UG).

## Published

With international search report.

Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: FORMING A PLANAR SURFACE OVER A SUBSTRATE BY MODIFYING THE TOPOGRAPHY OF THE SUBSTRATE



## (57) Abstract

A method of forming a substantially planar surface over a trench isolation region (33) of a semiconductor substrate (30). Latent active regions (42) are formed within the trench isolation region (33). A dielectric layer (38) is then deposited over the surface of the semiconductor substrate (30). Then, the dielectric layer (38) is polished back to form a planar surface.