

The invention relates to a circuit arrangement for analysing control signals in accordance with the preamble of Claim 1.

In highly integrated data processors, restrictions are implemented in the provision of control ports in order either to be able to use standard housing sizes or to keep the dimensions of the housing and the number of terminal pins within limits. If, for example, only two control ports are provided, only $s^2 = 4$ different commands can be issued using static control signals. In order to be able to issue further commands, it is possible to use dynamic control signals which are superimposed upon the static control signals.

The aim of the invention is to provide a circuit arrangement for the analysis of control signals which reliably separates the differently formed control signals and analyses these for control purposes. This aim is fulfilled in the case of a circuit arrangement according to the preamble of Claim 1, by the features described in the characterising clause.

The particular problem which arises in the analysis of static and dynamic control signals consists in that the static control signals are static only for a relatively long period of time, but change their state in the event of a change in the command, which change can be confused with a dynamic change of state. Vice versa, the dynamic changes in state behave in the manner of short static changes in state so that a danger of confusion exists also in this respect. In the case of the circuit according to the invention, the static states are initially stored and the output of the store is then used as control signal. This ensures that a dynamic change in state can exert no influence upon the control signals obtained from the static control signals. The dynamic control signals are used to synchronize a flip-flop so that also in the event

of mis-synchronization due to a change in the static control signals, this error is then compensated.

A further development provides that synchronization is permitted only within a time window in which the dynamic control signals can occur and thus avoids mis-synchronization. Additional further developments and advantageous embodiments of the invention are disclosed in the claims, the description and the drawing, which illustrates an exemplary embodiment.

In the drawing:

Figure 1 is a circuit diagram embodying the invention as part of a receiver for digital satellite broadcasting;

Figure 2 is a pulse diagram in explanation of the circuit shown in Figure 1.

The receiver for digital satellite broadcasting is provided for the reception of sound radio programmes in accordance with the specifications of the sound radio TV-SAT transmission method. The interleaving of the programmes into a frame structure and the accommodation of additional items of programme information in special service frames and special service super-frames and in an additional-information frame are described in detail in DE-OS 33 080 25 or Technical Guidelines ARD/ZDF No. 3R1 "Digital Satellite Broadcasting (DSR) - Specifications of the Sound Radio TV-SAT Transmission Method" published by the IRT Institute for Broadcasting Technology.

In addition to the other data items, a special service bit and two additional-information bits are transmitted in the main frame A in accordance with the specifications. Sixty four main frames are combined to form a special service frame SA in

the case of the special service bits and an additional-information frame in the case of the additional-information bits. In the additional-information frame a part of the available data is reserved for scale factors and another part for items of programme-accompanying information PI. The items of programme-accompanying information PI relate to the programmes whose sample values are previously transmitted. The number of available bits is not sufficient, however, to allow items of programme information to be transmitted in the additional-information frame for all the channels. Only in the case of stereo programmes, in the case of which the items of programme information are common to both channels, is it possible to accommodate complete items of programme information in an additional information frame. If, on the other hand, the channels are used individually, i.e. for mono-programmes, the items of programme information are transmitted alternately for the mono-channels, the allocation being so defined that at the start of a special service super-frame the programme information for the left mono-channel of programme 1 is transmitted. Depending upon which mono-channel is selected, following the commencement of the special service super-frame every following additional-information frame with an odd ordinal number or every following additional-information frame with an even ordinal number must thus be analysed.

Figure 1 illustrates a data processor 13, at the first control output of which control signals M1 occur and at the other control output of which control signals M2 occur. The state of the static control signals M1S and M2S indicates which operating mode exists. The coding is selected such that in the case of stereo, both outputs are set at logic L, in the case of two-tone transmissions both outputs are set at logic H, whereas in the case of mono-left M1S is set at logic H and

M2S at logic L, and in the case of mono-right M1S is set at logic L and M2S at logic H. A dynamic signal M1D which temporarily changes the state of M1 is emitted when it has been established by the data processor that the synchronizing word for the special service super-frame has been correctly recognised. For this purpose the signals are used, in the "mono" operating mode, to position a time window for items of programme information in such manner that only the items of programme information for the switched-on channel are analysed and the others are suppressed. In explanation of the mode of functioning of the circuit illustrated in Figure 1, additional reference is made to Figure 2 in which the signals are represented on different expanded scales.

The additional-information frames, as well as the special service frames, each contain 64 bits. Eight special service frames form a special service super-frame, as shown in Figure 2a. In Figure 2b signals which regularly occur in the additional information frame have been represented as continuous signals. These include a signal G9, which appears during the ninth clock signal, and a signal G89N which appears during the 19th and 19th clock signals. A window signal FE has also been represented, by which the data containing the items of programme-accompanying information can be output-coupled from the data stream. In the case of the "stereo operation" operating state shown below in Figure 2c, the items of programme-accompanying information for the stereo programmes are transmitted in every additional-information frame. Therefore it is permissible to analyse, in each additional-information frame, the PI bits occurring during the duration of the signal FE. In this case the control signals M1, M2 are set at logic L, whereby both flip-flops 1, 2, via their outputs and via the following NOR-linking elements 3, 4, produce a logic L at their outputs. Correspondingly, the

NAND-gates 6, 7 are disabled and produce a logic H across the AND gate 8. The signal FE occurring at a third input is now switched through during each additional-information frame.

Below the diagram for the stereo operation in Figure 2d the operating mode of "mono-left" has been shown. The static control signals are set accordingly at logic H in the case of M1 and at logic L in the case of M2. Following the recognition of the synchronizing word of the special service super-frame SAÜ, the data processor temporarily inverts the control signals and in this way emits a dynamic control signal M1D which is to be further used to select the window in which the items of programme information for the left mono-channel are contained. The static control signals occur at the inputs of the flip-flop 1 and the flip-flop 2 before the occurrence of the dynamic control signals M1D and are preliminarily stored. For the transfer into the stores, a clock signal T32N is used which is continuously present, and a signal G9, which is present during the ninth bit in the additional-information frame, is transferred via the AND linking element 5. The corresponding pulse diagram is shown in Figure 2e.

Changes in state at the inputs of the flip-flops 1 and 2 now no longer result in changes during the remaining time in the additional-information frame. On the occurrence of the dynamic signal M1D, which is expected during the 18th or 19th bit in the additional-information frame - compare the illustration in Figure 2f extended over time - a flip-flop 10 is set via a high-frequency clock signal T512N, which latter is fed via an Ex-OR-gate 11 in the form of a pulse to a NOR-gate 12 and resets the flip-flop 9 as resetting signal. The corresponding pulse diagram is shown in Figure 2g. As a result of the linking of the output Q of the flip-flop 9 to the output of the NOR-gate 3, via a NAND linking element 6 the

gate 8 is released only during additional-information frames with the ordinal number 1. The flip-flop 9, which has been brought into a determinate state, is thus switched over in the next additional-information frame by T32N in the time interval G9 and, as a result of the linking of its output signal to that of the NOR-gate 3, leads to the disabling of the NAND-gate 8 and thus also to the blockage of the window signal FE. Not until, in the third additional-information frame, the flip-flop 9 switches back into the original state, is the AND-gate 8 released so that the signal FE can be switched through and further processed as signal PIF.

Claims

1. A circuit arrangement for the analysis of control signals which are output from a data processor and which consist of static control signals and dynamic control signals superimposed upon the static control signals, characterised in that at least one store (1, 2) is provided which is supplied with the static control signals (M1S, M2S), and that a further store (9) is provided which is synchronized by the dynamic control signal (M1D).

2. A circuit arrangement as claimed in Claim 1, wherein the static control signals (M1S, M2S) serve to identify an operating mode and the dynamic control signals (M1D) serve to synchronize a selector circuit for data items characteristic of operating modes from a serial data stream, in particular for the analysis of items of programme information in digital satellite broadcasting, characterised in that a first and a second static control signal (M1S, M2S) are fed to two flip-flops (1, 2), which store the states of the control signals at predetermined times, that an edge detector (10, 11) for the dynamic control signals (M1D) is provided, the output signal of which is fed to a setting input (R) of a flip-flop (9) which is connected as frequency divider and which is clocked with the same clock signal (T32N) as the two other flip-flops (1, 2), and that the outputs of the flip-flops (1, 2) are linked to a window signal (FE) via a linking circuit (3, 4, 6, 7, 8).

3. A circuit arrangement as claimed in Claim 2, characterised in that the clock signal (T32N) for the flip-flops (1, 2, 9) is linked with an auxiliary signal (G9) occurring in a first time interval, and the dynamic control signal (M1D) is linked with a second auxiliary signal (G89),



and that the first auxiliary signal (G9) and the second auxiliary signal (G89) are offset in time in relation to one another.