

FIG. 1A

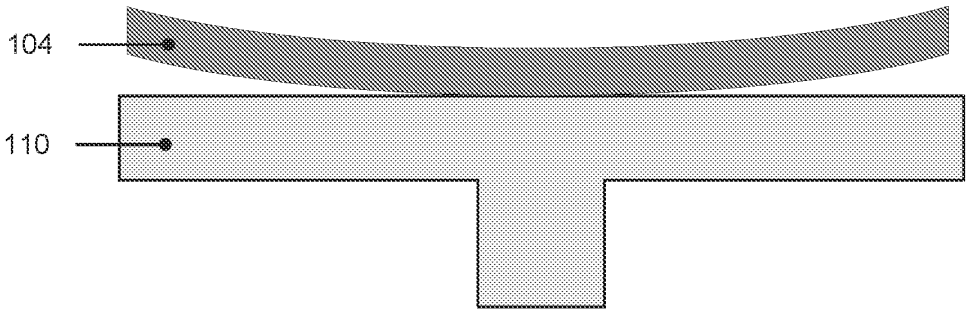

FIG. 1B

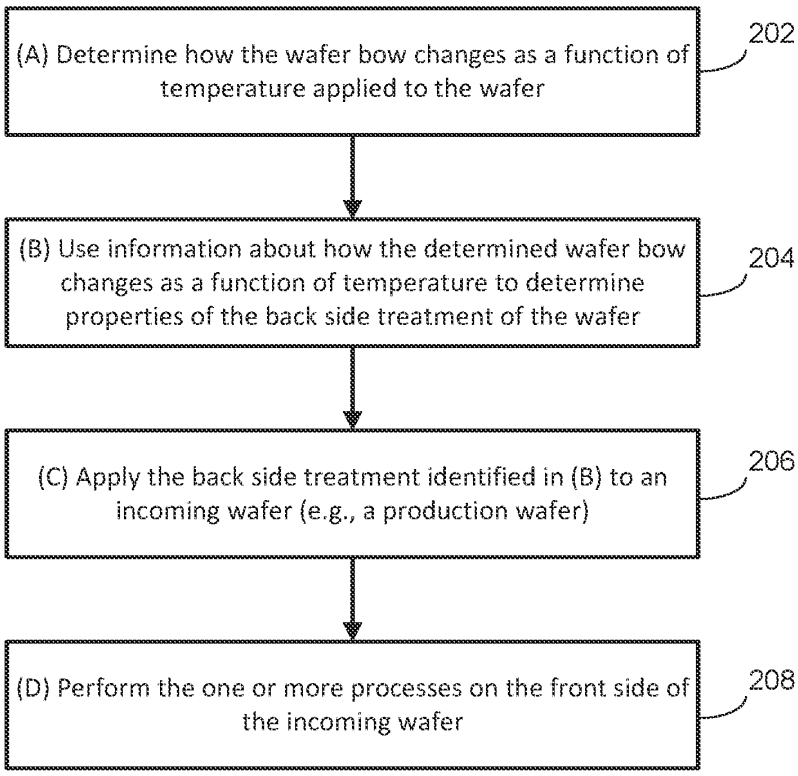
(A) Determine how the wafer bow changes as a function of temperature applied to the wafer
202
(B) Use information about how the determined wafer bow changes as a function of temperature to determine properties of the back side treatment of the wafer
204
(C) Apply the back side treatment identified in (B) to an incoming wafer (e.g., a production wafer)
206
(D) Perform the one or more processes on the front side of the incoming wafer
208

FIG. 2A

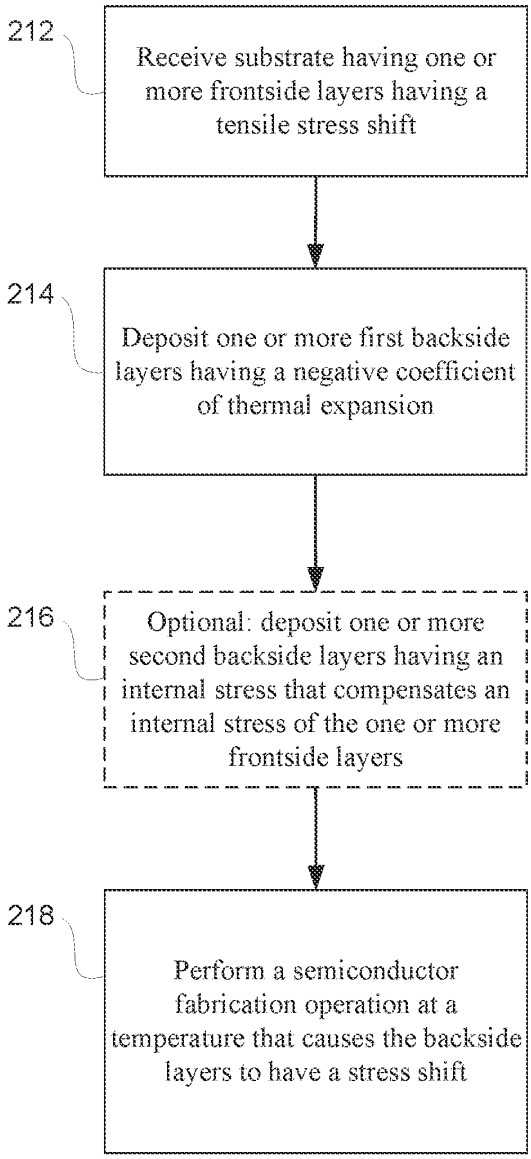
212
Receive substrate having one or more frontside layers having a tensile stress shift
214
Deposit one or more first backside layers having a negative coefficient of thermal expansion
216
Optional: deposit one or more second backside layers having an internal stress that compensates an internal stress of the one or more frontside layers
218
Perform a semiconductor fabrication operation at a temperature that causes the backside layers to have a stress shift

FIG. 2B

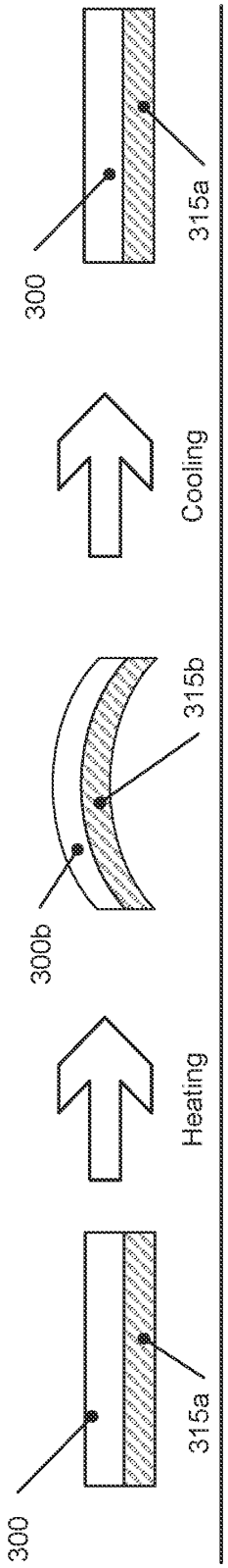
300
315a
Heating
300b
315b
Cooling
300
315a

FIG. 3A

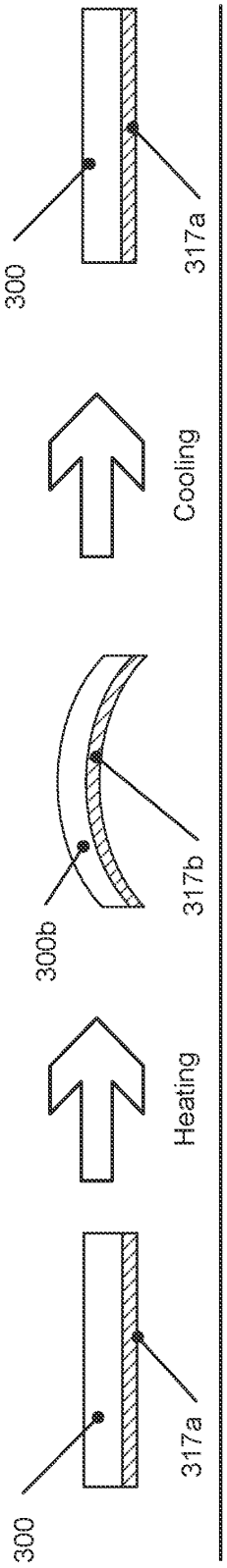
300
317a
Heating
300b
317b
Cooling
300
317a

FIG. 3B

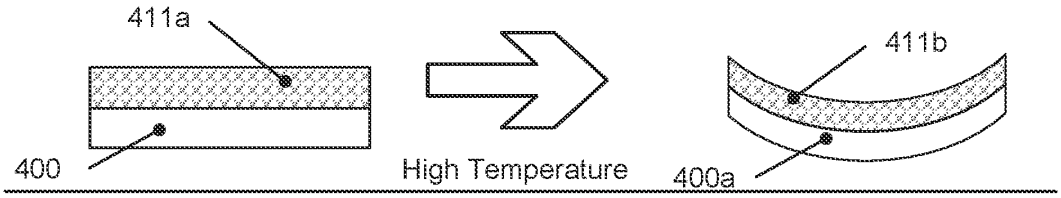

FIG. 4A

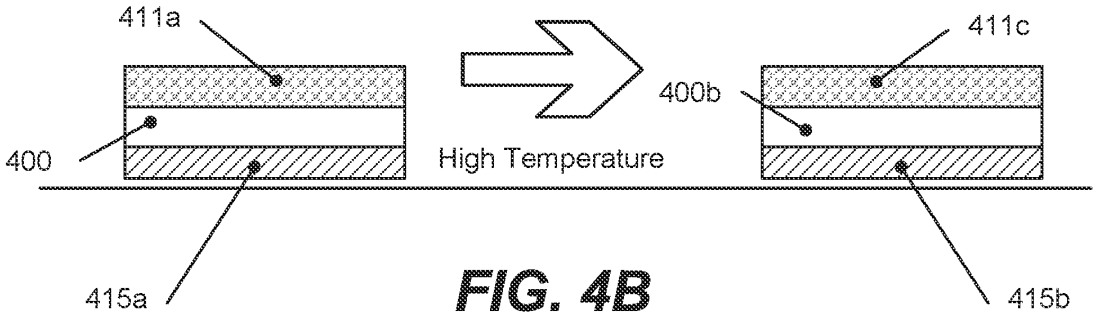

FIG. 4B

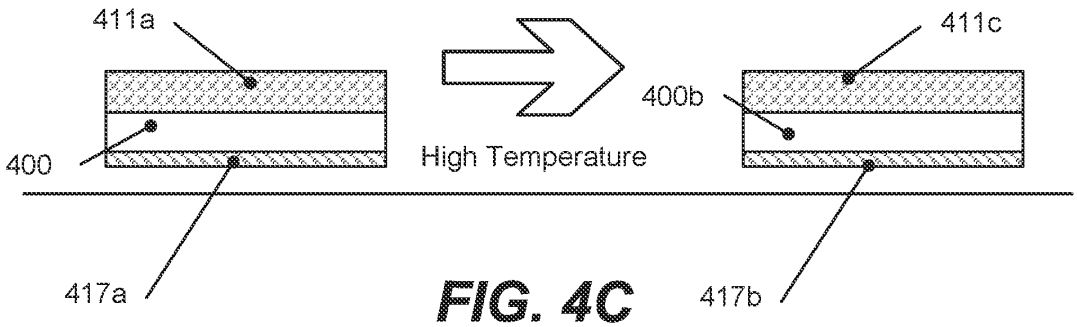

FIG. 4C

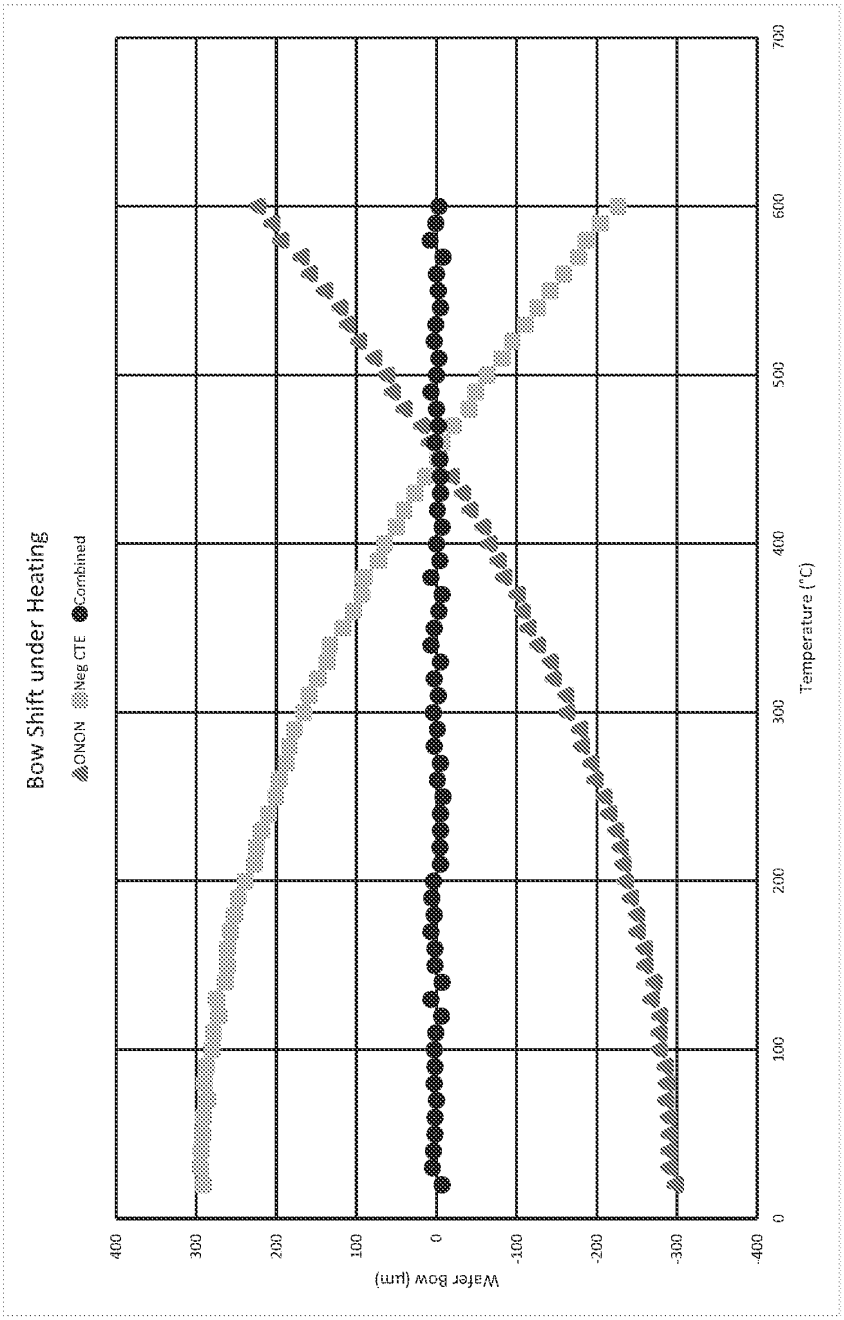
Bow Shift under Heating
ONON
Neg CTE
Combined
Wafer Bow (µm)
400
300
200
100
0
-100
-200
-300
-400
0
100
200
300
400
500
600
700
Temperature (°C)

FIG. 5

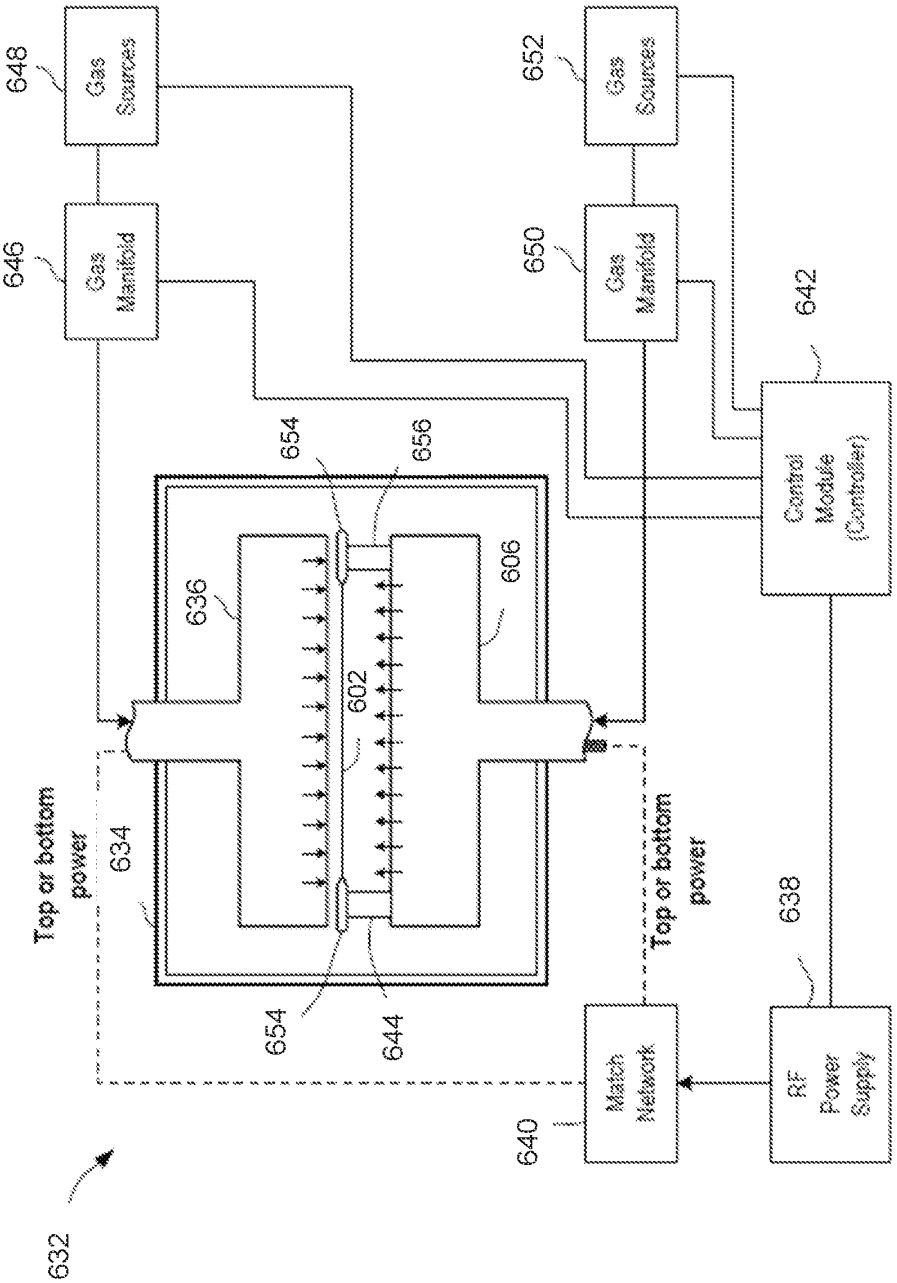
648
Gas Sources
646
Gas Manifold
652
Gas Sources
650
Gas Manifold
642
Control Module (Controller)
654
656
636
606
602
Top or bottom power
634
Top or bottom power
654
644
638
Match Network
RF Power Supply
640
632

FIG. 6A

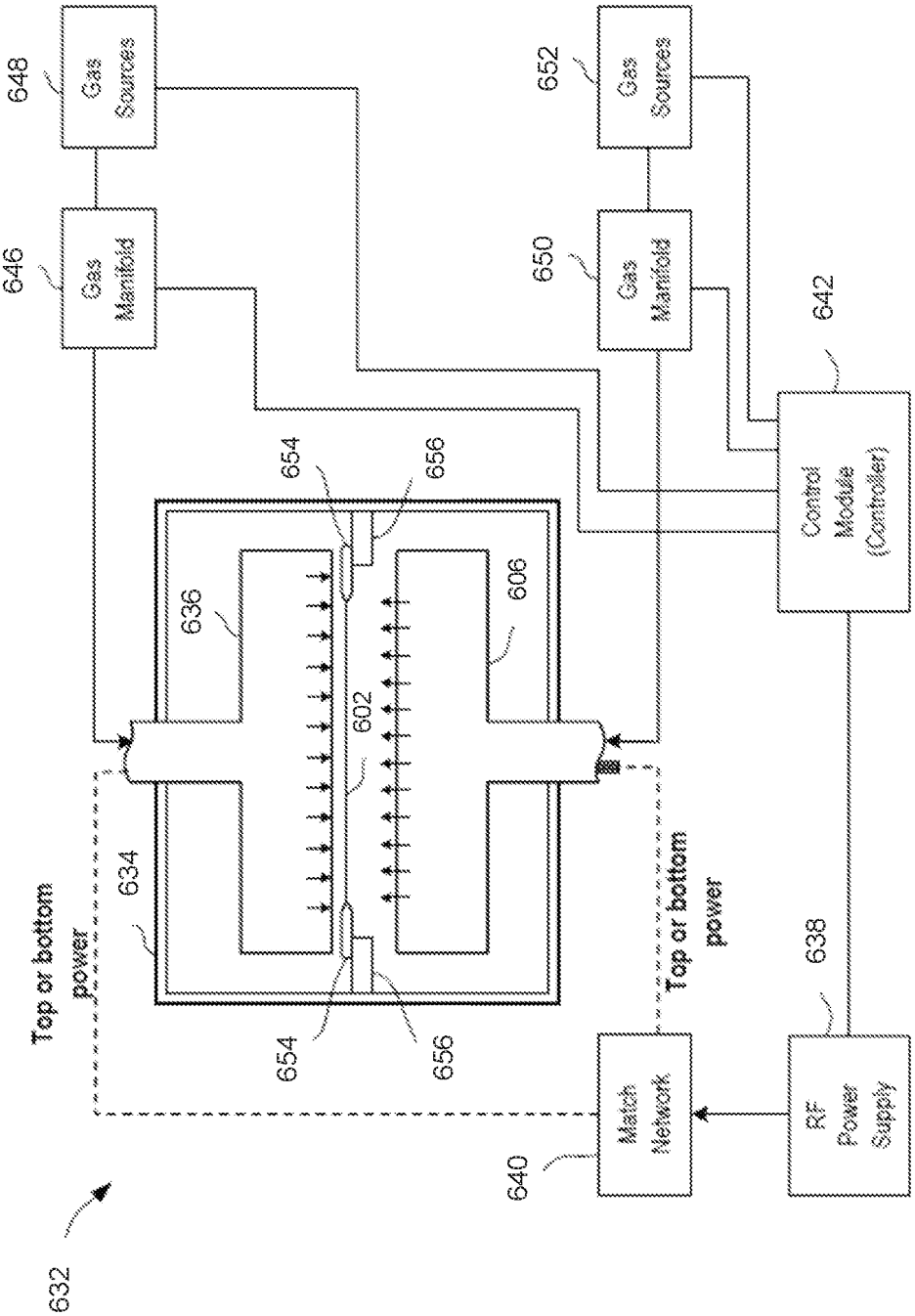
632
Top or bottom power
634
636
602
606
654
656
654
656
Top or bottom power
640
Match Network
638
RF Power Supply
642
Control Module (Controller)
646
Gas Manifold
648
Gas Sources
650
Gas Manifold
652
Gas Sources

FIG. 6B

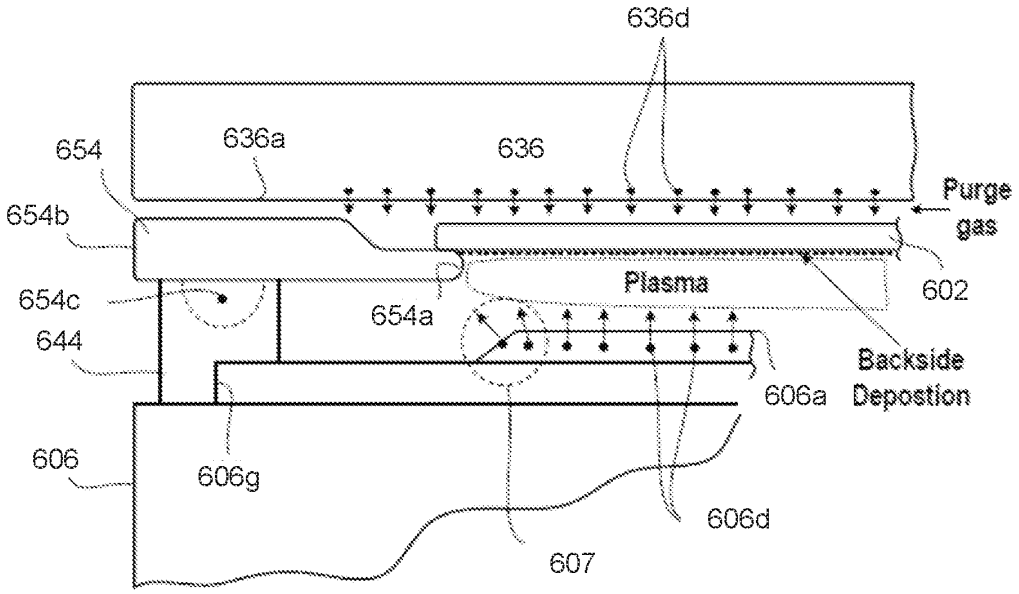
636d
654
636a
636
Purge gas
654b
602
Plasma
654c
654a
644
Backside Depostion
606a
606
606g
606d
607

FIG. 7A

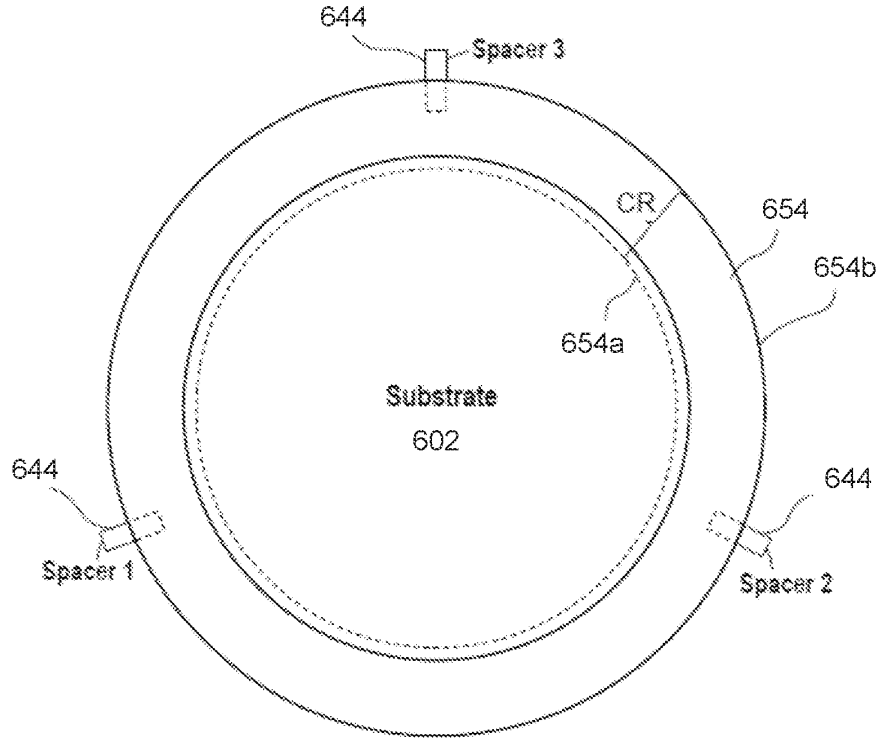
644
Spacer 3
CR
654
654b
654a
Substrate
602
644
644
Spacer 1
Spacer 2

FIG. 7B

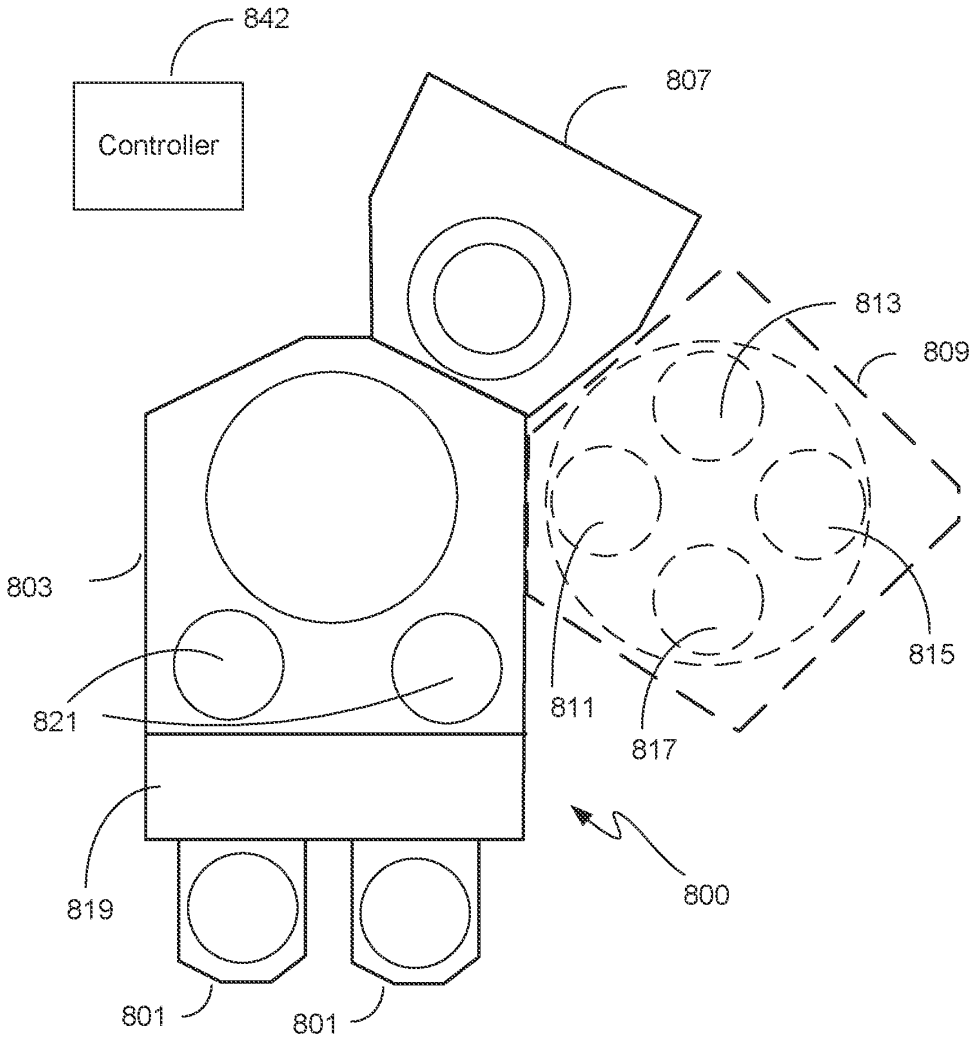

FIG. 8