DESCRIPTION

Title of Invention: PLASMA PROCESSING DEVICE, BIAS ELECTRIC POWER SUPPLY SYSTEM, AND PLASMA PROCESSING METHOD

Technical Field

[0001] Example embodiments of the present disclosure relate to a plasma processing apparatus, a bias power supply system, and a plasma processing method.

Background Art

[0002] A plasma processing apparatus is used in plasma processing of a substrate. The plasma processing apparatus described in Patent Literature 1 below has a first electrode and a second electrode in a substrate support in a chamber thereof. The first electrode is disposed below a substrate supporting surface on which a substrate is placed, and the second electrode is disposed below a ring supporting surface on which an edge ring is placed. A first bias power supply is connected to the first electrode, and a second bias power supply is connected to the second electrode.

Citation List

Patent Literature

[0003] [Patent Literature 1] Japanese Unexamined Patent Publication No. 2021-158134

Summary of Invention

Technical Problem

[0004] The present disclosure provides a technique for improving radial

uniformity of plasma processing of a substrate.

Solution to Problem

[0005] In one example embodiment, a plasma processing apparatus is provided. The plasma processing apparatus includes a chamber, a substrate support, a plasma generator, and a bias power supply system. The substrate support is disposed in the chamber. The substrate support includes a substrate supporting surface, an edge ring supporting surface, a first electrode, and a second electrode. The edge ring supporting surface surrounds the substrate supporting surface. The first electrode is disposed below the substrate supporting surface. The second electrode is disposed below the edge ring supporting surface. The plasma generator is configured to generate a plasma from a gas in the chamber. The bias power supply system is electrically coupled to the first electrode and the second electrode. The bias power supply system includes at least one DC power supply, a first switching circuit, a second switching circuit, and a single signal generator. The first switching circuit is electrically connected between the first electrode and each of the at least one DC power supply and ground. The second switching circuit is electrically connected between the second electrode and each of the at least one DC power supply and ground. The single signal generator is configured to generate a pulse control signal to control the first switching circuit to alternately connect the first electrode to the at least one DC power supply and ground, and to control the second switching circuit to alternately connect the second electrode to the at least one DC power supply and ground.

Advantageous Effects of Invention

[0006] According to one example embodiment, a technique for improving radial uniformity of plasma processing of a substrate is provided.

Brief Description of Drawings

[0007] [FIG. 1] FIG. 1 is a diagram for explaining a configuration example of a plasma processing system.

[FIG. 2] FIG. 2 is a diagram for explaining a configuration example of a capacitively coupled plasma processing apparatus.

[FIG. 3] FIG. 3 is a diagram illustrating a substrate support and a power supply in a plasma processing apparatus according to one example embodiment.

[FIG. 4] FIG. 4 is a diagram illustrating a bias power supply system according to one example embodiment.

[FIG. 5] FIG. 5 is a timing chart related to a bias power supply system according to one example embodiment.

[FIG. 6] FIG. 6 is a flowchart illustrating a plasma processing method according to one example embodiment.

[FIG. 7] FIG. 7 is a diagram illustrating connections of a plurality of switching elements that can be employed in a bias power supply system according to one example embodiment.

[FIG. 8] FIG. 8 is a diagram illustrating a substrate support and a power supply in a plasma processing apparatus according to another example embodiment.

[FIG. 9] FIG. 9 is a diagram illustrating a substrate support and a power supply in a plasma processing apparatus according to yet another example embodiment.

[FIG. 10] FIG. 10 is a block diagram of processing circuitry for performing computer-based operations described herein.

Description of Embodiments

[0008] Hereinafter, various example embodiments will be described in detail with reference to the drawings. In the drawings, the same or equivalent portions are denoted by the same reference signs.

[0009] FIG. 1 is a diagram for explaining a configuration example of a plasma processing system. In one embodiment, the plasma processing system includes a plasma processing apparatus 1 and a controller 2. The plasma processing system is an example of a substrate processing system, and the plasma processing apparatus 1 is an example of a substrate processing apparatus. The plasma processing apparatus 1 includes a plasma processing chamber 10, a substrate support 11, and a plasma generator 12. The plasma processing chamber 10 has a plasma processing space. The plasma processing chamber 10 further has at least one gas inlet for supplying at least one process gas into the plasma processing space and at least one gas outlet for exhausting gases from the plasma processing space. The gas inlet is connected to a gas supply 20 described below, and the gas outlet is connected to an exhaust system 40 described below. The substrate support 11 is disposed in the plasma processing space and has a substrate supporting surface for supporting a substrate.

[0010] The plasma generator 12 is configured to generate a plasma from the at least one process gas supplied into the plasma processing space. The plasma formed in the plasma processing space may be a capacitively coupled plasma (CCP: Capacitively Coupled Plasma), an inductively

coupled plasma (ICP: Inductively Coupled Plasma), an ECR plasma (Electron-Cyclotron-Resonance Plasma), a helicon wave plasma (HWP: Helicon Wave Plasma), a surface wave plasma (SWP: Surface Wave Plasma), or the like. Various types of plasma generators may also be used, including an AC (Alternating Current) plasma generator and a DC (Direct Current) plasma generator. In one embodiment, an AC signal (AC power) used in the AC plasma generator has a frequency in a range of 100 kHz to 10 GHz. Hence, the AC signal includes an RF (Radio Frequency) signal and a microwave signal. In one embodiment, the RF signal has a frequency in a range of 100 kHz to 150 MHz.

[0011] The controller 2 processes computer-executable instructions that cause the plasma processing apparatus 1 to perform various steps described in the present disclosure. The controller 2 may be configured to control individual components of the plasma processing apparatus 1 so as to execute the various steps described herein. In one embodiment, part or all of the controller 2 may be incorporated into the plasma processing apparatus 1. The controller 2 may include a processor 2a1, a storage 2a2, and a communication interface 2a3. The controller 2 is implemented by, for example, a computer 2a. The processor 2a1 may be configured to read a program from the storage 2a2 and perform various control operations by executing the read program. This program may be stored in the storage 2a2 in advance, or may be acquired via a medium when necessary. The acquired program is stored in the storage 2a2, read from the storage 2a2 by the processor 2a1, and executed. The medium may be any of various storage media readable by the computer 2a, or may be a communication line connected to the communication interface

2a3. The processor 2a1 may be a CPU (Central Processing Unit). The storage 2a2 may include a RAM (Random Access Memory), a ROM (Read Only Memory), an HDD (Hard Disk Drive), an SSD (Solid State Drive), or a combination thereof. The communication interface 2a3 may communicate with the plasma processing apparatus 1 via a communication line such as a LAN (Local Area Network).

[0012] An example configuration of a capacitively coupled plasma processing apparatus, which is an example of the plasma processing apparatus 1, will now be described below. FIG. 2 is a diagram for explaining a configuration example of the capacitively coupled plasma processing apparatus.

[0013] The capacitively coupled plasma processing apparatus 1 includes a plasma processing chamber 10, a gas supply 20, an electric power source 30, and an exhaust system 40. The plasma processing apparatus 1 further includes a substrate support 11 and a gas introduction unit. The gas introduction unit is configured to introduce at least one process gas into the plasma processing chamber 10. The gas introduction unit includes a showerhead 13. The substrate support 11 is disposed in the plasma processing chamber 10. The showerhead 13 is disposed above the substrate support 11. In one embodiment, the showerhead 13 functions as at least part of the ceiling of the plasma processing chamber 10. The plasma processing chamber 10 has a plasma processing space 10s defined by the showerhead 13, the sidewall 10a of the plasma processing chamber 10, and the substrate support 11. The plasma processing chamber 10 is grounded. The showerhead 13 and the substrate support 11 are electrically insulated from the housing

of the plasma processing chamber 10.

[0014] The substrate support 11 includes a main body 111 and a ring assembly 112. The main body 111 has a central region 111a for supporting a substrate W and an annular region 111b for supporting the ring assembly 112. A wafer is an example of the substrate W. The annular region 111b of the main body 111 surrounds the central region 111a of the main body 111 in plan view. The substrate W is disposed on the central region 111a of the main body 111, and the ring assembly 112 is disposed on the annular region 111b of the main body 111 so as to surround the substrate W on the central region 111a of the main body 111. Thus, the central region 111a is also called a substrate supporting surface for supporting the substrate W, and the annular region 111b is also called a ring supporting surface for supporting the ring assembly 112.

[0015] In one embodiment, the main body 111 includes a base 1110 and an electrostatic chuck 1111. The base 1110 includes a conductive member. The conductive member of the base 1110 can function as a lower electrode. The electrostatic chuck 1111 is disposed on the base 1110. The electrostatic chuck 1111 includes a ceramic member 1111a and an electrostatic electrode 1111b disposed in the ceramic member 1111a. The ceramic member 1111a has the central region 111a. In one embodiment, the ceramic member 1111a also has the annular region 111b. Any other member surrounding the electrostatic chuck 1111, such as an annular electrostatic chuck or an annular insulating member, may have the annular region 111b. In this case, the ring assembly 112 may be disposed on either the annular electrostatic chuck or the annular

insulating member, or on both the electrostatic chuck 1111 and the annular insulating member. At least one RF/DC electrode coupled to an RF source 31 and/or a DC source 32 described below may be disposed in the ceramic member 1111a. In this case, the at least one RF/DC electrode functions as the lower electrode. When a bias RF signal and/or a DC signal described below are supplied to the at least one RF/DC electrode, the RF/DC electrode is also called a bias electrode. It is noted that the conductive member of the base 1110 and the at least one RF/DC electrode may function as a plurality of lower electrodes. The electrostatic electrode 1111b may also function as a lower electrode. The substrate support 11 accordingly includes at least one lower electrode.

[0016] The ring assembly 112 includes one or more annular members. In one embodiment, the one or more annular members include one or more edge rings and at least one cover ring. The edge ring is formed of a conductive or insulating material, and the cover ring is formed of an insulating material.

[0017] The substrate support 11 may also include a temperature adjusting module configured to adjust at least one of the electrostatic chuck 1111, the ring assembly 112, and the substrate to a target temperature. The temperature adjusting module may include a heater, a heat transfer medium, a flow passage 1110a, or a combination thereof. A heat transfer fluid such as brine or gas flows through the flow passage 1110a. In one embodiment, the flow passage 1110a is formed in the base 1110, and one or more heaters are disposed in the ceramic member 1111a of the electrostatic chuck 1111. The substrate support 11 may further

include a heat transfer gas supply configured to supply a heat transfer gas to a gap between the rear surface of the substrate W and the central region 111a.

[0018] The showerhead 13 is configured to introduce at least one process gas from the gas supply 20 into the plasma processing space 10s. The showerhead 13 has at least one gas inlet 13a, at least one gas diffusion chamber 13b, and a plurality of gas introduction ports 13c. The process gas supplied to the gas inlet 13a passes through the gas diffusion chamber 13b and is introduced into the plasma processing space 10s from the plurality of gas introduction ports 13c. The showerhead 13 further includes at least one upper electrode. The gas introduction unit may include one or more side gas injectors (SGI: Side Gas Injector) attached to one or more openings formed in the sidewall 10a, in addition to the showerhead 13.

[0019] The gas supply 20 may include at least one gas source 21 and at least one flow rate controller 22. In one embodiment, the gas supply 20 is configured to supply at least one process gas from the corresponding gas source 21 through the corresponding flow rate controller 22 to the showerhead 13. Each flow rate controller 22 may include, for example, a mass flow controller or a pressure-controlled flow rate controller. Furthermore, the gas supply 20 may include at least one flow modulation device that modulates or pulses the flow rate of the at least one process gas.

[0020] The electric power source 30 includes an RF source 31 coupled to the plasma processing chamber 10 through at least one impedance matching circuit. The RF source 31 is configured to supply at least one

RF signal (RF power) to at least one lower electrode and/or at least one upper electrode. A plasma is thereby formed from the at least one process gas supplied into the plasma processing space 10s. Thus, the RF source 31 can function as at least part of the plasma generator 12. Furthermore, by supplying a bias RF signal to the at least one lower electrode, a bias potential is generated in the substrate W, and ionic components in the formed plasma can be attracted to the substrate W.

[0021] In one embodiment, the RF source 31 includes a first RF generator 31a and a second RF generator 31b. The first RF generator 31a is coupled to the at least one lower electrode and/or the at least one upper electrode through the at least one impedance matching circuit and is configured to generate a source RF signal (source RF power) for generating a plasma. In one embodiment, the source RF signal has a frequency in a range of 10 MHz to 150 MHz. In one embodiment, the first RF generator 31a may be configured to generate a plurality of source RF signals having different frequencies. The generated one or more source RF signals are supplied to the at least one lower electrode and/or the at least one upper electrode.

[0022] The second RF generator 31b is coupled to the at least one lower electrode through the at least one impedance matching circuit and is configured to generate a bias RF signal (bias RF power). The frequency of the bias RF signal may be the same as or different from the frequency of the source RF signal. In one embodiment, the bias RF signal has a frequency lower than the frequency of the source RF signal. In one embodiment, the bias RF signal has a frequency in a range of 100 kHz to 60 MHz. In one embodiment, the second RF generator 31b may be

configured to generate a plurality of bias RF signals having different frequencies. The generated one or more bias RF signals are supplied to the at least one lower electrode. In various embodiments, at least one of the source RF signal and the bias RF signal may be pulsed.

[0023] The electric power source 30 may also include a DC source 32 coupled to the plasma processing chamber 10. The DC source 32 includes a first DC generator 32a and a second DC generator 32b. In one embodiment, the first DC generator 32a is connected to the at least one lower electrode and is configured to generate a first DC signal. The generated first DC signal is applied to the at least one lower electrode. In one embodiment, the second DC generator 32b is connected to the at least one upper electrode and is configured to generate a second DC signal. The generated second DC signal is applied to the at least one upper electrode.

[0024] In various embodiments, the first and second DC signals may be pulsed. In this case, a sequence of voltage pulses is applied to the at least one lower electrode and/or the at least one upper electrode. The voltage pulses may have a rectangular, trapezoidal, or triangular pulse waveform, or a combined waveform thereof. In one embodiment, a waveform generator for generating a sequence of voltage pulses from the DC signal is connected between the first DC generator 32a and the at least one lower electrode. The first DC generator 32a and the waveform generator thereby function as a voltage pulse generator. When the second DC generator 32b and the waveform generator function as a voltage pulse generator, the voltage pulse generator is connected to the at least one upper electrode. The voltage pulses may have positive polarity

or negative polarity. The sequence of voltage pulses may also include one or more positive-polarity voltage pulses and one or more negative-polarity voltage pulses within one period. The first and second DC generators 32a, 32b may be provided in addition to the RF source 31, or the first DC generator 32a may be provided in place of the second RF generator 31b.

[0025] The exhaust system 40 may be connected to, for example, a gas outlet 10e provided in the bottom of the plasma processing chamber 10. The exhaust system 40 may include a pressure regulation valve and a vacuum pump. The pressure in the plasma processing space 10s is adjusted by the pressure regulation valve. The vacuum pump may include a turbomolecular pump, a dry pump, or a combination thereof.

[0026] Hereinafter, reference is made to FIG. 3. FIG. 3 is a diagram illustrating a substrate support and a power supply in a plasma processing apparatus according to one example embodiment. The substrate support 11, the power supply, and the configuration related to the power supply illustrated in FIG. 3 may be employed in the plasma processing apparatus 1.

[0027] As described above, the substrate support 11 includes the base 1110 and the electrostatic chuck 1111. The first RF generator 31a may be electrically connected to the base 1110 via a matcher 31am.

[0028] The substrate support 11 includes a first region R1 and a second region R2. In FIG. 3, the boundary between the first region R1 and the second region R2 is indicated by a dashed line. The first region R1 is a region intersecting an axis AX and has a substantially disk shape. The axis AX is a central axis of the substrate support 11 and may coincide

with a central axis of the chamber 10. The first region R1 includes, as an upper surface thereof, the above-described substrate supporting surface 111a. The second region R2 extends so as to surround the first region R1. The substrate W is placed on the substrate supporting surface 111a and is supported on the first region R1. The second region R2 is an annular region around the axis AX. The second region R2 includes, as an upper surface thereof, the above-described ring supporting surface 111b. The edge ring ER included in the ring assembly 112 is placed on the ring supporting surface 111b and is supported on the second region R2. The substrate W is disposed in a region surrounded by the edge ring ER.

[0029] The substrate support 11 includes a first electrode BE1 and a second electrode BE2. The first electrode BE1 extends below the substrate supporting surface 111a and is disposed in the first region R1. The first electrode BE1 may be a film formed of a conductive material. The first electrode BE1 may have a substantially circular planar shape. The first electrode BE1 may be disposed such that a center thereof is located on the axis AX.

[0030] The second electrode BE2 extends at least below the ring supporting surface 111b and extends at least in the second region R2. The second electrode BE2 may be a film formed of a conductive material. The second electrode BE2 may have a substantially annular planar shape. The second electrode BE2 may be disposed such that a center thereof is located on the axis AX. In one embodiment, an inner edge region of the second electrode BE2 may extend below an edge region of the first electrode BE1 and within the first region R1. That is,

the inner edge region of the second electrode BE2 may extend within the first region R1 so as to overlap the first electrode BE1 in the vertical direction (the direction in which the axis AX extends).

[0031] As illustrated in FIG. 3, the electrostatic chuck 1111 may include a dielectric portion 1111d. The dielectric portion 1111d may be the above-described ceramic member 1111a. A central portion of the dielectric portion 1111d may form the first region R1 and may have the substrate supporting surface 111a as an upper surface thereof. A peripheral portion of the dielectric portion 1111d may form the second region R2 and may have the ring supporting surface 111b as an upper surface thereof.

[0032] The electrostatic chuck 1111 may include a chuck electrode CE1 as part of the electrostatic electrode 1111b. The chuck electrode CE1 is disposed in the dielectric portion 1111d and in the first region R1. The chuck electrode CE1 may be a film formed of a conductive material. The chuck electrode CE1 may have a substantially circular planar shape. The chuck electrode CE1 may be disposed such that a center thereof is located on the axis AX. The chuck electrode CE1 may extend between the substrate supporting surface 111a and the first electrode BE1.

[0033] The electrostatic chuck 1111 may also include chuck electrodes CE2 and CE3 as another part of the electrostatic electrode 1111b. Each of the chuck electrodes CE2 and CE3 is disposed in the dielectric portion 1111d and in the second region R2. Each of the chuck electrodes CE2 and CE3 may be a film formed of a conductive material. Each of the chuck electrodes CE2 and CE3 may extend circumferentially around the axis AX and may have a substantially annular planar shape. The chuck

electrode CE2 is disposed on the inner side relative to the chuck electrode CE3. That is, a radial distance between the chuck electrode CE2 and the axis AX is smaller than a radial distance between the chuck electrode CE3 and the axis AX. Each of the chuck electrodes CE2 and CE3 may extend between the ring supporting surface 111b and the second electrode BE2.

[0034] The plasma processing apparatus 1 may further include a DC power supply 41p. The DC power supply 41p is electrically connected to the chuck electrode CE1 via a switch 41s. A filter 41f may further be connected between the DC power supply 41p and the chuck electrode CE1. The filter 41f is a low-pass filter configured to block or attenuate an RF signal such as a source RF signal. When a voltage from the DC power supply 41p is applied to the chuck electrode CE1, an electrostatic attraction force is generated between the electrostatic chuck 1111 and the substrate W. The substrate W is attracted to the first region R1 by the generated electrostatic attraction force and is held by the first region R1.

[0035] The plasma processing apparatus 1 may further include DC power supplies 42p and 43p. The DC power supply 42p is electrically connected to the chuck electrode CE2 via a switch 42s. A filter 42f may further be connected between the DC power supply 42p and the chuck electrode CE2. The filter 42f is a low-pass filter configured to block or attenuate an RF signal such as a source RF signal. The DC power supply 43p is electrically connected to the chuck electrode CE3 via a switch 43s. A filter 43f may further be connected between the DC power supply 43p and the chuck electrode CE3. The filter 43f is a low-pass filter configured to block or attenuate an RF signal such as a source RF signal.

When voltages from the DC power supplies 42p and 43p are applied to the chuck electrodes CE2 and CE3, an electrostatic attraction force is generated between the electrostatic chuck 1111 and the edge ring ER. The edge ring ER is attracted to the second region R2 by the generated electrostatic attraction force and is held by the second region R2. Voltages may be applied to the chuck electrode CE2 and the chuck electrode CE3 such that a potential difference is generated between them. That is, the second region R2 may function as a bipolar electrostatic chuck.

[0036] The plasma processing apparatus 1 further includes a bias power supply system 50 as the above-described first DC generator 32a. The bias power supply system 50 is electrically coupled to the first electrode BE1 and the second electrode BE2. The bias power supply system 50 includes at least one DC power supply, a first switching circuit 61, a second switching circuit 62, and a single signal generator 70.

[0037] The first switching circuit 61 is electrically connected between the first electrode BE1 and each of the at least one DC power supply and ground. The second switching circuit 62 is electrically connected between the second electrode BE2 and each of the at least one DC power supply and ground. In the example illustrated in FIG. 3, the bias power supply system 50 includes a DC power supply 51 and a DC power supply 52 as the at least one DC power supply. The DC power supply 51 is electrically connected to the first electrode BE1 via the first switching circuit 61. The DC power supply 52 is electrically connected to the second electrode BE2 via the second switching circuit 62. Each of the DC power supply 51 and the DC power supply 52 may be a variable DC

power supply. The bias power supply system 50 may include a single DC power supply as the at least one DC power supply.

[0038] The signal generator 70 is configured to generate a pulse control signal for controlling the first switching circuit 61 and the second switching circuit 62. The signal generator 70 may include a single clock generator including an oscillator such as a crystal oscillator, and can generate a pulse control signal synchronized with the clock generator. The signal generator 70 may be configured like processing circuitry 130 described below, or may be configured as a dedicated circuit.

[0039] The pulse control signal generated by the signal generator 70 causes the first electrode BE1 to be alternately connected to the at least one DC power supply and ground, and causes the second electrode BE2 to be alternately connected to the at least one DC power supply and ground. Accordingly, the bias power supply system 50 supplies a sequence of voltage pulses as an electrical bias to each of the first electrode BE1 and the second electrode BE2. The sequence of voltage pulses is supplied to the first electrode BE1 and the second electrode BE2 in order to attract ions from the plasma in the chamber 10 to the substrate W and the edge ring ER.

[0040] In the bias power supply system 50, the first switching circuit 61 and the second switching circuit 62 are controlled by the pulse control signal from the single signal generator 70 to generate the sequence of voltage pulses supplied to the first electrode BE1 and the second electrode BE2. Therefore, a phase difference between a voltage waveform of the substrate W corresponding to the sequence of voltage pulses and a voltage waveform of the edge ring ER corresponding to the

sequence of voltage pulses is reduced. Hence, according to the plasma processing apparatus 1, radial uniformity of plasma processing of the substrate W is improved.

[0041] Hereinafter, reference is made to FIG. 4. FIG. 4 is a diagram illustrating a bias power supply system according to one example embodiment. In one embodiment, the bias power supply system 50 may have the configuration illustrated in FIG. 4. That is, the first switching circuit 61 may include at least one first switching element 611 and at least one second switching element 612. As illustrated in FIG. 4, the first switching circuit 61 may include one first switching element 611 and one second switching element 612.

[0042] The second switching circuit 62 may also include at least one third switching element 623 and at least one fourth switching element 624. As illustrated in FIG. 4, the second switching circuit 62 may include one third switching element 623 and one fourth switching element 624. Each of the at least one first switching element 611, the at least one second switching element 612, the at least one third switching element 623, and the at least one fourth switching element 624 may include a transistor such as a FET.

[0043] The first switching element 611 includes a control terminal 611c. The first switching element 611 further includes a first terminal and a second terminal. The control terminal 611c is connected to the signal generator 70. In one embodiment, the control terminal 611c is connected to an output 70a of the signal generator 70 for the above-described pulse control signal. The first switching element 611 is configured to switch between open and closed states thereof in response

to the pulse control signal applied to the control terminal 611c. That is, the first switching element 611 is configured to switch between conduction between the first terminal and the second terminal thereof and disconnection between these terminals in response to the pulse control signal applied to the control terminal 611c.

[0044] The first switching element 611 is connected between the negative terminal of the DC power supply 51 and a node 61na. The first terminal of the first switching element 611 is connected to the negative terminal of the DC power supply 51, and the second terminal of the first switching element 611 is connected to the node 61na. The node 61na is connected to a node 61nb.

[0045] The second switching element 612 includes a control terminal 612c. The second switching element 612 further includes a first terminal and a second terminal. The control terminal 612c is connected to the signal generator 70. In one embodiment, the control terminal 612c is connected to an output 70b of the signal generator 70 for an inverted signal of the above-described pulse control signal. The second switching element 612 is configured to switch between open and closed states thereof in response to the inverted signal applied to the control terminal 612c. That is, the second switching element 612 is configured to switch between conduction between the first terminal and the second terminal thereof and disconnection between these terminals in response to the inverted signal applied to the control terminal 612c.

[0046] The second switching element 612 is connected between the node 61na and each of the positive terminal of the DC power supply 51 and ground. The first terminal of the second switching element 612 is

connected to the node 61na, and the second terminal of the second switching element 612 is connected to the positive terminal of the DC power supply 51 and ground.

[0047] The first switching circuit 61 may further include a diode 61da and a diode 61db. The anode of the diode 61da is connected to the negative terminal of the DC power supply 51 and the first terminal of the first switching element 611. The cathode of the diode 61da is connected to the node 61nb. The anode of the diode 61db is connected to the node 61nb. The cathode of the diode 61db is connected to the positive terminal of the DC power supply 51, ground, and the second terminal of the second switching element 612. The first switching circuit 61 may further include an inductor 61i, and the inductor 61i may be connected between the node 61na and the node 61nb. The node 61nb is electrically connected to the first electrode BE1. The first electrode BE1 may be electrically connected to the first electrode BE1 via a resistor 61r. A low-pass filter that blocks or attenuates an RF signal such as a source RF signal may be connected between the first electrode BE1 and the output of the first switching circuit 61 (the node 61nb or the end of the resistor 61r on the first electrode BE1 side).

[0048] The third switching element 623 includes a control terminal 623c. The third switching element 623 further includes a first terminal and a second terminal. The control terminal 623c is connected to the signal generator 70. In one embodiment, the control terminal 623c is connected to the output 70a of the signal generator 70 for the above-described pulse control signal. The third switching element 623 is configured to switch between open and closed states thereof in

response to the pulse control signal applied to the control terminal 623c. That is, the third switching element 623 is configured to switch between conduction between the first terminal and the second terminal thereof and disconnection between these terminals in response to the pulse control signal applied to the control terminal 623c.

[0049] The third switching element 623 is connected between the negative terminal of the DC power supply 52 and a node 62na. The first terminal of the third switching element 623 is connected to the negative terminal of the DC power supply 52, and the second terminal of the third switching element 623 is connected to the node 62na. The node 62na is connected to a node 62nb.

[0050] The fourth switching element 624 includes a control terminal 624c. The fourth switching element 624 further includes a first terminal and a second terminal. The control terminal 624c is connected to the signal generator 70. In one embodiment, the control terminal 624c is connected to the output 70b of the signal generator 70 for the inverted signal of the above-described pulse control signal. The fourth switching element 624 is configured to switch between open and closed states thereof in response to the inverted signal applied to the control terminal 624c. That is, the fourth switching element 624 is configured to switch between conduction between the first terminal and the second terminal thereof and disconnection between these terminals in response to the inverted signal applied to the control terminal 624c.

[0051] The fourth switching element 624 is connected between the node 62na and each of the positive terminal of the DC power supply 52 and ground. The first terminal of the fourth switching element 624 is

connected to the node 62na, and the second terminal of the fourth switching element 624 is connected to the positive terminal of the DC power supply 52 and ground.

[0052] The second switching circuit 62 may further include a diode 62da and a diode 62db. The anode of the diode 62da is connected to the negative terminal of the DC power supply 52 and the first terminal of the third switching element 623. The cathode of the diode 62da is connected to the node 62nb. The anode of the diode 62db is connected to the node 62nb. The cathode of the diode 62db is connected to the positive terminal of the DC power supply 52, ground, and the second terminal of the fourth switching element 624. The second switching circuit 62 may further include an inductor 62i, and the inductor 62i may be connected between the node 62na and the node 62nb. The node 62nb is electrically connected to the second electrode BE2. The second electrode BE2 may be electrically connected to the second electrode BE2 via a resistor 62r. A low-pass filter that blocks or attenuates an RF signal such as a source RF signal may be connected between the second electrode BE2 and the output of the second switching circuit 62 (the node 62nb or the end of the resistor 62r on the second electrode BE2 side).

[0053] As illustrated in FIG. 4, the output of the first switching circuit 61 (the node 61nb or the end of the resistor 61r on the first electrode BE1 side) may be connected to the cathode of the diode 62db. In this case, the positive terminal of the DC power supply 52 need not be connected to ground. In this case, the voltage pulse output from the second switching circuit 62 has an output voltage value equal to the sum of the negative output voltage value of the DC power supply 51 and the

negative output voltage value of the DC power supply 52. The output of the first switching circuit 61 (the node 61nb or the end of the resistor 61r on the first electrode BE1 side) need not be connected to the cathode of the diode 62db.

[0054] Hereinafter, reference is made to FIG. 5. FIG. 5 is a timing chart related to a bias power supply system according to one example embodiment. FIG. 5 illustrates the level of the pulse control signal, the level of the inverted signal, the states of the first and third switching elements, the states of the second and fourth switching elements, the output voltage of the first switching circuit 61, and the output voltage of the second switching circuit 62.

[0055] As illustrated in FIG. 5, the signal generator 70 may generate the pulse control signal and the inverted signal such that each of the pulse control signal and the inverted signal alternately transitions between a first level and a second level. The respective first levels of the pulse control signal and the inverted signal may be different from each other. Also, the respective second levels of the pulse control signal and the inverted signal may be different from each other.

[0056] The first switching element 611 and the third switching element 623 are in a closed state (conductive state) when the pulse control signal has the first level L1, and are in an open state (disconnected state) when the pulse control signal has the second level L2. The second switching element 612 and the fourth switching element 624 are in a closed state when the inverted signal has the first level L1, and are in an open state when the inverted signal has the second level L2. Accordingly, as illustrated in FIG. 5, the voltage pulse applied from the first switching

circuit 61 to the first electrode BE1 and the voltage pulse applied from the second switching circuit 62 to the second electrode BE2 are synchronized with each other, and the phase difference therebetween is eliminated.

[0057] In one embodiment, the length of a first electrical path and the length of a second electrical path may be substantially equal to each other. The first electrical path is an electrical path that electrically connects the at least one DC power supply of the bias power supply system 50 (for example, the negative terminal of the DC power supply 51) and the first electrode BE1 to each other. The second electrical path is an electrical path that electrically connects the at least one DC power supply (for example, the negative terminal of the DC power supply 52) and the second electrode BE2 to each other. In this case, the phase difference between the voltage pulse applied from the first switching circuit 61 to the first electrode BE1 and the voltage pulse applied from the second switching circuit 62 to the second electrode BE2 is further reduced.

[0058] In one embodiment, the distance along the vertical direction between the first electrode BE1 and the substrate supporting surface 111a and the distance along the vertical direction between the second electrode BE2 and the ring supporting surface 111b may be substantially equal to each other. In this case, the phase difference between the voltage pulse applied from the first switching circuit 61 to the first electrode BE1 and the voltage pulse applied from the second switching circuit 62 to the second electrode BE2 is further reduced.

[0059] In one embodiment, as described above, the edge region of the

first electrode BE1 and the inner edge region of the second electrode BE2 may be disposed so as to overlap each other in the vertical direction. In this case, a portion of the voltage pulse output from the first switching circuit 61 is coupled to the edge ring ER, and a portion of the voltage pulse output from the second switching circuit 62 is coupled to the substrate W. Thereby, radial uniformity of plasma processing of the substrate W is further improved.

[0060] In one embodiment, the first switching circuit 61 and the second switching circuit 62 may be formed in a single member 65. The member 65 may be a single housing or a single circuit board. That is, the first switching circuit 61 and the second switching circuit 62 may be disposed in a single housing. Alternatively or additionally, the first switching circuit 61 and the second switching circuit 62 may be formed on a single circuit board.

[0061] Hereinafter, a plasma processing method according to one example embodiment will be described with reference to FIG. 6. The plasma processing method illustrated in FIG. 6 (hereinafter referred to as "method MT") can be applied to the plasma processing apparatus 1. In the method MT, each component of the plasma processing apparatus 1 can be controlled by the controller 2. The method MT can also be applied to plasma processing apparatuses other than the plasma processing apparatus 1, for example, plasma processing apparatuses according to various other embodiments described below.

[0062] The method MT starts with operation STa. In operation STa, the substrate W is placed on the substrate supporting surface 111a. The substrate W is disposed on the electrostatic chuck 1111 in a region

surrounded by the edge ring ER. The substrate W is held by the electrostatic chuck 1111.

[0063] In operation STb, a plasma is generated in the chamber 10. In operation STb, gas is supplied from the gas supply 20 into the chamber 10. In operation STb, the pressure in the chamber 10 is reduced to a specified pressure by the exhaust system 40. In operation STb, a plasma is generated from the gas in the chamber 10 by the plasma generator 12. In one embodiment, a source RF signal is supplied from the first RF generator 31a to generate a plasma from the gas in the chamber 10.

[0064] In operation STc, a sequence of voltage pulses is supplied from the bias power supply system 50 to the first electrode BE1 and the second electrode BE2 in order to attract ions from the plasma in the chamber 10 to the substrate W and the edge ring ER. In operation STc, the pulse control signal is applied from the single signal generator 70 to the first switching circuit 61 and the second switching circuit 62 so as to generate the sequence of voltage pulses in the bias power supply system 50.

[0065] Hereinafter, reference is made to FIG. 7. FIG. 7 is a diagram illustrating connections of a plurality of switching elements that can be employed in a bias power supply system according to one example embodiment. The plurality of switching elements SW illustrated in FIG. 7 are connected in series and/or in parallel. A switching element group including the plurality of switching elements SW can be used as one or more of the at least one first switching element 611, the at least one second switching element 612, the at least one third switching element 623, and the at least one fourth switching element 624. When the

plurality of switching elements SW are connected in series, the withstand voltage of the switching element group is increased. When the plurality of switching elements SW are connected in parallel, the allowable current of the switching element group is increased.

[0066] Specifically, the bias power supply system 50 may include a plurality of first switching elements 611 as the at least one first switching element 611. The plurality of first switching elements 611 may be connected in series and/or in parallel between the first electrode BE1 and the at least one DC power supply (for example, the negative terminal of the DC power supply 51), like the plurality of switching elements SW.

[0067] The bias power supply system 50 may also include a plurality of third switching elements 623 as the at least one third switching element 623. The plurality of third switching elements 623 may be connected in series and/or in parallel between the second electrode BE2 and the at least one DC power supply (for example, the negative terminal of the DC power supply 52), like the plurality of switching elements SW.

[0068] The bias power supply system 50 may also include a plurality of second switching elements 612 as the at least one second switching element 612. The plurality of second switching elements 612 may be connected in series and/or in parallel between the first electrode BE1 and ground, like the plurality of switching elements SW.

[0069] The bias power supply system 50 may also include a plurality of fourth switching elements 624 as the at least one fourth switching element 624. The plurality of fourth switching elements 624 may be connected in series and/or in parallel between the second electrode BE2 and ground, like the plurality of switching elements SW.

[0070] Hereinafter, reference is made to FIG. 8. FIG. 8 is a diagram illustrating a substrate support and a power supply in a plasma processing apparatus according to another example embodiment. Hereinafter, the plasma processing apparatus 1A illustrated in FIG. 8 will be described in terms of differences from the plasma processing apparatus 1. In FIG. 8, the DC power supplies 41p, 42p, and 43p, the switches 41s, 42s, and 43s, and the filters 41f, 42f, and 43f are omitted.

[0071] In the plasma processing apparatus 1A, the substrate support 11 further includes a third electrode BE3. The third electrode BE3 extends below the substrate supporting surface 111a and within the first region R1 so as to surround the first electrode BE1. The third electrode BE3 is spaced apart from the first electrode BE1. The third electrode BE3 may be a film formed of a conductive material. The third electrode BE3 may have a substantially annular planar shape. The third electrode BE3 may be disposed such that a center thereof is located on the axis AX. In the plasma processing apparatus 1A, the edge region of the third electrode BE3 and the inner edge region of the second electrode BE2 may be disposed so as to overlap each other in the vertical direction, instead of the edge region of the first electrode BE1.

[0072] The plasma processing apparatus 1A includes a bias power supply system 50A in place of the bias power supply system 50. The bias power supply system 50A further includes a third switching circuit 63. The circuit configuration of the third switching circuit 63 is the same as the circuit configurations of the first switching circuit 61 and the second switching circuit 62. The third switching circuit 63 is electrically connected between each of the at least one DC power supply (for

example, the negative terminal of the DC power supply 53) and ground and the third electrode BE3. The single signal generator 70 generates the above-described pulse control signal to control the third switching circuit 63 so as to alternately connect the third electrode BE3 to the at least one DC power supply (for example, the negative terminal of the DC power supply 53) and ground. The single signal generator 70 may also apply the above-described inverted signal to the third switching circuit 63 for control of the third switching circuit 63 in the same manner as for the first switching circuit 61 and the second switching circuit 62.

[0073] The distance along the vertical direction between the third electrode BE3 and the substrate supporting surface 111a may be the same as the distance along the vertical direction between the first electrode BE1 and the substrate supporting surface 111a. The length of a third electrical path connecting the at least one DC power supply (for example, the negative terminal of the DC power supply 53) and the third electrode BE3 to each other may be substantially the same as the length of each of the above-described first electrical path and second electrical path. The third switching circuit 63 may be disposed in the above-described member 65 together with the first switching circuit 61 and the second switching circuit 62.

[0074] Hereinafter, reference is made to FIG. 9. FIG. 9 is a diagram illustrating a substrate support and a power supply in a plasma processing apparatus according to yet another example embodiment. As illustrated in FIG. 9, in the plasma processing apparatus 1, the second electrode BE2 may extend only within the second region R2. That is, the second electrode BE2 need not overlap the first electrode BE1 in the

vertical direction within the first region R1. Also, in the plasma processing apparatus 1A, the second electrode BE2 may extend only within the second R2. That is, the second electrode BE2 need not overlap the third electrode BE3 in the vertical direction within the first region R1.

[0075] Hereinafter, an example of processing circuitry that can be used as one or more processing circuits in the plasma processing apparatus 1, such as the controller 2 and/or the signal generator 70, will be described. FIG. 10 is a block diagram of processing circuitry for performing computer-based operations described herein. FIG. 10 illustrates processing circuitry 130 that may be used to control any computer-based control processes, descriptions or blocks in flowcharts can be understood as representing modules, segments or portions of code which include one or more executable instructions for implementing specific logical functions or steps in the process, and alternate implementations are included within the scope of the exemplary embodiments of the present advancements in which functions can be executed out of order from that shown or discussed, including substantially concurrently or in reverse order, depending upon the functionality involved, as would be understood by those skilled in the art. The various elements, features, and processes described herein may be used independently of one another or may be combined in various ways. All possible combinations and sub-combinations are intended to fall within the scope of this disclosure.

[0076] In FIG. 10, the processing circuitry 130 includes a CPU 1200 which performs one or more of the control processes described

above/below. The process data and instructions may be stored in memory 1202. These process data and instructions may also be stored on a storage medium disk 1204 such as a hard drive (HDD) or portable storage medium or may be stored remotely. Further, the claimed advancements are not limited by the form of the computer-readable media on which the instructions of the inventive process are stored. For example, the instructions may be stored on CDs, DVDs, in FLASH memory, RAM, ROM, PROM, EPROM, EEPROM, hard disk or any other information processing device with which the processing circuitry 130 communicates, such as a server or computer.

[0077] Further, the claimed advancements may be provided as a utility application, background daemon, or component of an operating system, or combination thereof, executing in conjunction with CPU 1200 and an operating system such as Microsoft Windows, UNIX, Solaris, LINUX, Apple MAC-OS and other systems known to those skilled in the art.

[0078] The hardware elements in order to achieve the processing circuitry 130 may be realized by various circuitry elements. Further, each of the functions of the above described embodiments may be implemented by circuitry, which includes one or more processing circuits. A processing circuit includes a particularly programmed processor, for example, processor (CPU) 1200, as shown in FIG. 10. A processing circuit also includes devices such as an application specific integrated circuit (ASIC) and conventional circuit components arranged to perform the recited functions.

[0079] In FIG. 10, the processing circuitry 130 includes a CPU 1200 which performs the processes described above. The processing circuitry

130 may be a general-purpose computer or a particular, special-purpose machine. In one embodiment, the processing circuitry 130 becomes a particular, special-purpose machine when the processor 1200 is programmed to control the plasma generator 12 and the gas supply 20, or additionally or alternatively, to control the bias power supply system 50.

[0080] Alternatively, or additionally, the CPU 1200 may be implemented on an FPGA, ASIC, PLD or using discrete logic circuits, as one of ordinary skill in the art would recognize. Further, CPU 1200 may be implemented as multiple processors cooperatively working in parallel to perform the instructions of the inventive processes described above.

[0081] The processing circuitry 130 in FIG. 10 also includes a network controller 1206, such as an Intel Ethernet PRO network interface card from Intel Corporation of America, for interfacing with network 1228. As can be appreciated, the network 1228 can be a public network, such as the Internet, or a private network such as a LAN or WAN network, or any combination thereof and can also include PSTN or ISDN sub-networks. The network 1228 can also be wired, such as an Ethernet network, or can be wireless such as a cellular network including EDGE, 3G and 4G wireless cellular systems. The wireless network can also be Wi-Fi, Bluetooth (registered trademark), or any other wireless form of communication that is known.

[0082] The processing circuitry 130 further includes a display controller 1208, such as a graphics card or graphics adaptor for interfacing with display 1210, such as a monitor. A general purpose I/O interface 1212 interfaces with a keyboard and/or mouse 1214 as well as a touch screen panel 1216 on or separate from display 1210. The general purpose I/O

interface also connects to a variety of peripherals 1218 including printers and scanners.

[0083] The storage controller 1224 connects the storage medium disk 1204 with communication bus 1226, which may be an ISA, EISA, VESA, PCI, or similar, for interconnecting all of the components of the processing circuitry 130. A description of the general features and functionality of the display 1210, keyboard and/or mouse 1214, as well as the display controller 1208, storage controller 1224, network controller 1206, sound controller 1220, and general purpose I/O interface 1212 is omitted herein for brevity as these features are known.

[0084] The exemplary circuit elements described in the context of the present disclosure may be replaced with other elements and structured differently than the examples provided herein. Moreover, circuitry configured to perform features described herein may be implemented in multiple circuit units (e.g., chips), or the features may be combined in circuitry on a single chipset.

[0085] The functions and features described herein may also be executed by various distributed components of a system. For example, one or more processors may execute these system functions, wherein the processors are distributed across multiple components communicating in a network. The distributed components may include one or more client and server machines, which may share processing, in addition to various human interface and communication devices (e.g., display monitors, smart phones, tablets, personal digital assistants (PDAs)). The network may be a private network, such as a LAN or WAN, or may be a public network, such as the Internet. Input to the system may be

received via direct user input and received remotely either in real-time or as a batch process. Additionally, some implementations may be performed on modules or hardware not identical to those described. Accordingly, other implementations are within the scope that may be claimed.

[0086] Although various example embodiments have been described above, various additions, omissions, substitutions, and changes may be made without being limited to the example embodiments described above. It is also possible to combine elements in different embodiments to form other embodiments.

[0087] For example, the chuck electrode CE1 may also serve as the first electrode BE1. Alternatively or additionally, one or both of the chuck electrodes CE2 and CE3 may also serve as the second electrode BE2.

[0088] Hereinafter, first and second experimental examples conducted for evaluation of the plasma processing apparatus 1 will be described. In the first experimental example, plasma etching was performed on a film of a sample substrate using the plasma processing apparatus 1 illustrated in FIG. 9. That is, in the first experimental example, a sequence of voltage pulses generated by controlling the first and second switching circuits by the pulse control signal from the single signal generator 70 was supplied to the first electrode BE1 and the second electrode BE2. In the second experimental example, plasma etching was performed on a film of a sample substrate having the same configuration as in the first experimental example using a plasma processing apparatus similar to the plasma processing apparatus 1. However, the plasma processing apparatus used in the second experimental example differed from the

plasma processing apparatus 1 in that the first switching circuit 61 and the second switching circuit 62 were respectively controlled by two pulse control signals from two independent signal generators. That is, in the second experimental example, during plasma etching, a sequence of voltage pulses generated by controlling the first switching circuit 61 by the pulse control signal from one of the two signal generators was supplied to the first electrode BE1. Also, in the second experimental example, during plasma etching, a sequence of voltage pulses generated by controlling the second switching circuit 62 by another pulse control signal from the other of the two signal generators was supplied to the second electrode BE2.

[0089] In each of the first and second experimental examples, the depths of holes formed in the central region and the edge region of the sample substrate were determined. Then, from the depths of the holes formed in the central region and the edge region of the sample substrate, the ratio of the etching rate of the edge region to the etching rate of the central region was determined. Also, the circularity of the upper end openings of the holes formed in each of the central region and the edge region of the sample substrate was determined. The circularity is the ratio of the width of the hole in the direction orthogonal to the radial direction of the substrate to the width of the hole in the radial direction of the substrate.

[0090] In the first experimental example, the ratio of the etching rates was 0.97, and the circularity was 0.949. On the other hand, in the second experimental example, the ratio of the etching rates was 0.76, and the circularity was 0.492. From the first and second experimental examples, it was confirmed that the plasma processing apparatus 1 is capable of

improving radial uniformity of plasma processing of a substrate.

[0091] Here, various example embodiments included in the present disclosure are described in [E1] to [E19] below.

[0092] [E1]

A plasma processing apparatus including:

a chamber;

a substrate support disposed in the chamber, the substrate support including:

a substrate supporting surface;

an edge ring supporting surface surrounding the substrate supporting surface;

a first electrode disposed below the substrate supporting surface; and

a second electrode disposed below the edge ring supporting surface;

a plasma generator configured to generate a plasma from a gas in the chamber; and

a bias power supply system electrically coupled to the first electrode and the second electrode,

wherein the bias power supply system includes:

at least one DC power supply;

a first switching circuit electrically connected between the first electrode and each of the at least one DC power supply and ground;

a second switching circuit electrically connected between the second electrode and each of the at least one DC power

supply and ground; and

a single signal generator configured to generate a pulse control signal to control the first switching circuit to alternately connect the first electrode to the at least one DC power supply and ground, and to control the second switching circuit to alternately connect the second electrode to the at least one DC power supply and ground.

[0093] [E2]

The plasma processing apparatus according to E1, wherein

the first switching circuit includes:

at least one first switching element having a control terminal connected to the signal generator, the at least one first switching element being electrically connected between the first electrode and the at least one DC power supply; and

at least one second switching element having a control terminal connected to the signal generator, the at least one second switching element being electrically connected between the first electrode and ground, and

the second switching circuit includes:

at least one third switching element having a control terminal connected to the signal generator, the at least one third switching element being electrically connected between the second electrode and the at least one DC power supply; and

at least one fourth switching element having a control terminal connected to the signal generator, the at least one fourth switching element being electrically connected between the second electrode and ground.

[0094] [E3]

The plasma processing apparatus according to E2,

wherein the bias power supply system includes:

as the at least one first switching element, a plurality of first switching elements connected in series and/or in parallel between the first electrode and the at least one DC power supply; and

as the at least one third switching element, a plurality of third switching elements connected in series and/or in parallel between the second electrode and the at least one DC power supply.

[0095] [E4]

The plasma processing apparatus according to E2 or E3, wherein

the control terminal of the at least one first switching element and the control terminal of the at least one third switching element are connected to an output of the signal generator for the pulse control signal, and

the control terminal of the at least one second switching element and the control terminal of the at least one fourth switching element are connected to an output of the signal generator for an inverted signal of the pulse control signal.

[0096] [E5]

The plasma processing apparatus according to E4, wherein

the signal generator is configured to generate the pulse control signal and the inverted signal such that each of the pulse control signal and the inverted signal alternately transitions between a first level and a second level,

the at least one first switching element and the at least one third

switching element are configured to be in a closed state when the pulse control signal has the first level and to be in an open state when the pulse control signal has the second level, and

the at least one second switching element and the at least one fourth switching element are configured to be in a closed state when the inverted signal has the first level and to be in an open state when the inverted signal has the second level.

[0097] [E6]

The plasma processing apparatus according to any one of E1 to E5,

wherein a length of an electrical path electrically connecting the at least one DC power supply and the first electrode to each other and a length of an electrical path electrically connecting the at least one DC power supply and the second electrode to each other are substantially equal to each other.

[0098] [E7]

The plasma processing apparatus according to any one of E1 to E6,

wherein the first switching circuit and the second switching circuit are disposed in a single housing or on a single circuit board.

[0099] [E8]

The plasma processing apparatus according to any one of E1 to E6,

wherein the substrate support includes a dielectric portion having the substrate supporting surface and the ring supporting surface, and

a distance along a vertical direction between the first electrode

and the substrate supporting surface and a distance along the vertical direction between the second electrode and the ring supporting surface are substantially equal to each other.

[0100] [E9]

The plasma processing apparatus according to any one of E1 to E8,

wherein an edge region of the first electrode and an inner edge region of the second electrode are disposed so as to overlap each other in a vertical direction.

[0101] [E10]

The plasma processing apparatus according to any one of E1 to E8, wherein

the substrate support includes a third electrode disposed below the substrate supporting surface so as to surround the first electrode,

the bias power supply system further includes a third switching circuit electrically connected between the third electrode and each of the at least one DC power supply and ground, and

the single signal generator is configured to generate the pulse control signal to control the third switching circuit to alternately connect the third electrode to the at least one DC power supply and ground.

[0102] [E11]

The plasma processing apparatus according to any one of E1 to E10,

wherein the first switching circuit is electrically connected between a negative terminal of the at least one DC power supply and the first electrode, and

the second switching circuit is electrically connected between the negative terminal of the at least one DC power supply and the second electrode.

[0103] [E12]

The plasma processing apparatus according to any one of E1 to E12,

wherein the bias power supply system includes a first DC power supply and a second DC power supply as the at least one DC power supply,

the first switching circuit is electrically connected between the first DC power supply and the first electrode, and

the second switching circuit is electrically connected between the second DC power supply and the second electrode.

[0104] [E13]

A bias power supply system including:

at least one DC power supply;

a first switching circuit electrically connected between a first electrode of a substrate support disposed below a substrate supporting surface of the substrate support in a chamber of a plasma processing apparatus and each of the at least one DC power supply and ground;

a second switching circuit electrically connected between a second electrode disposed below a ring supporting surface of the substrate support surrounding the substrate supporting surface and each of the at least one DC power supply and ground; and

a single signal generator configured to generate a pulse control signal to control the first switching circuit to alternately connect the first

electrode to the at least one DC power supply and ground, and to control the second switching circuit to alternately connect the second electrode to the at least one DC power supply and ground.

[0105] [E14]

The bias power supply system according to E13, wherein

the first switching circuit includes:

at least one first switching element having a control terminal connected to the signal generator, the at least one first switching element being electrically connected between the first electrode and the at least one DC power supply; and

at least one second switching element having a control terminal connected to the signal generator, the at least one second switching element being electrically connected between the first electrode and ground, and

the second switching circuit includes:

at least one third switching element having a control terminal connected to the signal generator, the at least one third switching element being electrically connected between the second electrode and the at least one DC power supply; and

at least one fourth switching element having a control terminal connected to the signal generator, the at least one fourth switching element being electrically connected between the second electrode and ground.

[0106] [E15]

The bias power supply system according to E14,

wherein the bias power supply system includes:

as the at least one first switching element, a plurality of first switching elements connected in series and/or in parallel between the first electrode and the at least one DC power supply; and

as the at least one third switching element, a plurality of third switching elements connected in series and/or in parallel between the second electrode and the at least one DC power supply.

[0107] [E16]

The bias power supply system according to E14 or E15, wherein

the control terminal of the at least one first switching element and the control terminal of the at least one third switching element are connected to an output of the signal generator for the pulse control signal, and

the control terminal of the at least one second switching element and the control terminal of the at least one fourth switching element are connected to an output of the signal generator for an inverted signal of the pulse control signal.

[0108] [E17]

The bias power supply system according to claim 16, wherein

the signal generator is configured to generate the pulse control signal and the inverted signal such that each of the pulse control signal and the inverted signal alternately transitions between a first level and a second level,

the at least one first switching element and the at least one third switching element are configured to be in a closed state when the pulse control signal has the first level and to be in an open state when the pulse control signal has the second level, and

the at least one second switching element and the at least one fourth switching element are configured to be in a closed state when the inverted signal has the first level and to be in an open state when the inverted signal has the second level.

[0109] [E18]

The bias power supply system according to any one of E13 to E17,

wherein the first switching circuit and the second switching circuit are disposed in a single housing or on a single circuit board.

[0110] [E19]

A plasma processing method including:

(a) placing a substrate on a substrate supporting surface of a substrate support in a chamber of a plasma processing apparatus, the substrate support including the substrate supporting surface, a ring supporting surface surrounding the substrate support, a first electrode disposed below the substrate supporting surface, and a second electrode disposed below the ring supporting surface;

(b) generating a plasma in the chamber;

(c) supplying a sequence of voltage pulses from a bias power supply system to the first electrode and the second electrode to attract ions from the plasma to the substrate on the substrate supporting surface and an edge ring on the ring supporting surface,

wherein the bias power supply system includes:

at least one DC power supply;

a first switching circuit electrically connected between the first electrode and each of the at least one DC power supply and

ground;

a second switching circuit electrically connected between the second electrode and each of the at least one DC power supply and ground; and

a single signal generator configured to generate a pulse control signal to control the first switching circuit so as to alternately connect the first electrode to the at least one DC power supply and ground, and to control the second switching circuit so as to alternately connect the second electrode to the at least one DC power supply and ground, and

wherein the (c) includes applying the pulse control signal from the single signal generator to the first switching circuit and the second switching circuit to generate the sequence of voltage pulses in the bias power supply system.

[0111] From the foregoing, it will be appreciated that various embodiments of the present disclosure have been described herein for purposes of illustration, and that various modifications may be made without departing from the scope and spirit of the present disclosure. Accordingly, the various embodiments disclosed herein are not intended to be limiting, and the true scope and spirit are indicated by the appended claims.

Reference Signs List

[0112] 1: plasma processing apparatus, 10: chamber, 11: substrate support, 111a: substrate supporting surface, 111b: ring supporting surface, BE1: first electrode, BE2: second electrode, 12: plasma generator, 50: bias power supply system, 51, 52: DC power supply, 61:

first switching circuit, 62: second switching circuit, 70: signal generator.

CLAIMS

[Claim 1]

A plasma processing apparatus comprising:

a chamber;

a substrate support disposed in the chamber, the substrate support comprising:

a substrate supporting surface;

an edge ring supporting surface surrounding the substrate supporting surface;

a first electrode disposed below the substrate supporting surface; and

a second electrode disposed below the edge ring supporting surface;

a plasma generator configured to generate a plasma from a gas in the chamber; and

a bias power supply system electrically coupled to the first electrode and the second electrode,

wherein the bias power supply system comprises:

at least one DC power supply;

a first switching circuit electrically connected between the first electrode and each of the at least one DC power supply and ground;

a second switching circuit electrically connected between the second electrode and each of the at least one DC power supply and ground; and

a single signal generator configured to generate a pulse

control signal to control the first switching circuit to alternately connect the first electrode to the at least one DC power supply and ground, and to control the second switching circuit to alternately connect the second electrode to the at least one DC power supply and ground.

[Claim 2]

The plasma processing apparatus according to claim 1, wherein the first switching circuit comprises:

at least one first switching element having a control terminal connected to the signal generator, the at least one first switching element being electrically connected between the first electrode and the at least one DC power supply; and

at least one second switching element having a control terminal connected to the signal generator, the at least one second switching element being electrically connected between the first electrode and ground, and

the second switching circuit comprises:

at least one third switching element having a control terminal connected to the signal generator, the at least one third switching element being electrically connected between the second electrode and the at least one DC power supply; and

at least one fourth switching element having a control terminal connected to the signal generator, the at least one fourth switching element being electrically connected between the second electrode and ground.

[Claim 3]

The plasma processing apparatus according to claim 2,

wherein the bias power supply system comprises:

as the at least one first switching element, a plurality of first switching elements connected in series and/or in parallel between the first electrode and the at least one DC power supply; and

as the at least one third switching element, a plurality of third switching elements connected in series and/or in parallel between the second electrode and the at least one DC power supply.

[Claim 4]

The plasma processing apparatus according to claim 2, wherein

the control terminal of the at least one first switching element and the control terminal of the at least one third switching element are connected to an output of the signal generator for the pulse control signal, and

the control terminal of the at least one second switching element and the control terminal of the at least one fourth switching element are connected to an output of the signal generator for an inverted signal of the pulse control signal.

[Claim 5]

The plasma processing apparatus according to claim 4, wherein

the signal generator is configured to generate the pulse control signal and the inverted signal such that each of the pulse control signal and the inverted signal alternately transitions between a first level and a second level,

the at least one first switching element and the at least one third switching element are configured to be in a closed state when the pulse control signal has the first level and to be in an open state when the pulse

control signal has the second level, and

the at least one second switching element and the at least one fourth switching element are configured to be in a closed state when the inverted signal has the first level and to be in an open state when the inverted signal has the second level.

[Claim 6]

The plasma processing apparatus according to any one of claims 1 to 5,

wherein a length of an electrical path electrically connecting the at least one DC power supply and the first electrode to each other and a length of an electrical path electrically connecting the at least one DC power supply and the second electrode to each other are substantially equal to each other.

[Claim 7]

The plasma processing apparatus according to any one of claims 1 to 5,

wherein the first switching circuit and the second switching circuit are disposed in a single housing or on a single circuit board.

[Claim 8]

The plasma processing apparatus according to any one of claims 1 to 5,

wherein the substrate support includes a dielectric portion having the substrate supporting surface and the ring supporting surface, and

a distance along a vertical direction between the first electrode and the substrate supporting surface and a distance along the vertical direction between the second electrode and the ring supporting surface

are substantially equal to each other.

[Claim 9]

The plasma processing apparatus according to any one of claims 1 to 5,

wherein an edge region of the first electrode and an inner edge region of the second electrode are disposed so as to overlap each other in a vertical direction.

[Claim 10]

The plasma processing apparatus according to any one of claims 1 to 5, wherein

the substrate support includes a third electrode disposed below the substrate supporting surface so as to surround the first electrode,

the bias power supply system further includes a third switching circuit electrically connected between the third electrode and each of the at least one DC power supply and ground, and

the single signal generator is configured to generate the pulse control signal to control the third switching circuit to alternately connect the third electrode to the at least one DC power supply and ground.

[Claim 11]

The plasma processing apparatus according to any one of claims 1 to 5,

wherein the first switching circuit is electrically connected between a negative terminal of the at least one DC power supply and the first electrode, and

the second switching circuit is electrically connected between the negative terminal of the at least one DC power supply and the second

electrode.

[Claim 12]

The plasma processing apparatus according to any one of claims 1 to 5,

wherein the bias power supply system includes a first DC power supply and a second DC power supply as the at least one DC power supply,

the first switching circuit is electrically connected between the first DC power supply and the first electrode, and

the second switching circuit is electrically connected between the second DC power supply and the second electrode.

[Claim 13]

A bias power supply system comprising:

at least one DC power supply;

a first switching circuit electrically connected between a first electrode of a substrate support disposed below a substrate supporting surface of the substrate support in a chamber of a plasma processing apparatus and each of the at least one DC power supply and ground;

a second switching circuit electrically connected between a second electrode disposed below a ring supporting surface of the substrate support surrounding the substrate supporting surface and each of the at least one DC power supply and ground; and

a single signal generator configured to generate a pulse control signal to control the first switching circuit to alternately connect the first electrode to the at least one DC power supply and ground, and to control the second switching circuit so as to alternately connect the second

electrode to the at least one DC power supply and ground.

[Claim 14]

The bias power supply system according to claim 13, wherein the first switching circuit comprises:

at least one first switching element having a control terminal connected to the signal generator, the at least one first switching element being electrically connected between the first electrode and the at least one DC power supply; and

at least one second switching element having a control terminal connected to the signal generator, the at least one second switching element being electrically connected between the first electrode and ground, and

the second switching circuit comprises:

at least one third switching element having a control terminal connected to the signal generator, the at least one third switching element being electrically connected between the second electrode and the at least one DC power supply; and

at least one fourth switching element having a control terminal connected to the signal generator, the at least one fourth switching element being electrically connected between the second electrode and ground.

[Claim 15]

The bias power supply system according to claim 14,

wherein the bias power supply system comprises:

as the at least one first switching element, a plurality of first switching elements connected in series and/or in parallel between

the first electrode and the at least one DC power supply; and

as the at least one third switching element, a plurality of third switching elements connected in series and/or in parallel between the second electrode and the at least one DC power supply.

[Claim 16]

The bias power supply system according to claim 14, wherein

the control terminal of the at least one first switching element and the control terminal of the at least one third switching element are connected to an output of the signal generator for the pulse control signal, and

the control terminal of the at least one second switching element and the control terminal of the at least one fourth switching element are connected to an output of the signal generator for an inverted signal of the pulse control signal.

[Claim 17]

The bias power supply system according to claim 16, wherein

the signal generator is configured to generate the pulse control signal and the inverted signal such that each of the pulse control signal and the inverted signal alternately transitions between a first level and a second level,

the at least one first switching element and the at least one third switching element are configured to be in a closed state when the pulse control signal has the first level and to be in an open state when the pulse control signal has the second level, and

the at least one second switching element and the at least one fourth switching element are configured to be in a closed state when the

inverted signal has the first level and to be in an open state when the inverted signal has the second level.

[Claim 18]

The bias power supply system according to any one of claims 13 to 17,

wherein the first switching circuit and the second switching circuit are disposed in a single housing or on a single circuit board.

[Claim 19]

A plasma processing method comprising:

(a) placing a substrate on a substrate supporting surface of a substrate support in a chamber of a plasma processing apparatus, the substrate support comprising the substrate supporting surface, a ring supporting surface surrounding the substrate support, a first electrode disposed below the substrate supporting surface, and a second electrode disposed below the ring supporting surface;

(b) generating a plasma in the chamber;

(c) supplying a sequence of voltage pulses from a bias power supply system to the first electrode and the second electrode to attract ions from the plasma to the substrate on the substrate supporting surface and an edge ring on the ring supporting surface,

wherein the bias power supply system comprises:

at least one DC power supply;

a first switching circuit electrically connected between the first electrode and each of the at least one DC power supply and ground;

a second switching circuit electrically connected

between the second electrode and each of the at least one DC power supply and ground; and

a single signal generator configured to generate a pulse control signal to control the first switching circuit to alternately connect the first electrode to the at least one DC power supply and ground, and to control the second switching circuit so as to alternately connect the second electrode to the at least one DC power supply and ground, and

wherein the (c) includes applying the pulse control signal from the single signal generator to the first switching circuit and the second switching circuit to generate the sequence of voltage pulses in the bias power supply system.