4F-SQUARE MEMORY CELL HAVING VERTICAL FLOATING-GATE TRANSISTORS WITH SELF-ALIGNED SHALLOW TRENCH ISOLATION

ABSTRACT

A densely packed array (200) of vertical semiconductor devices and methods of making thereof are disclosed. The array has columns of bitlines and rows of wordlines. The gates of the transistors act as the wordlines (225), while the source or drain regions acts as the bitlines (220). The array has vertical pillars (230), acting as a channel, formed between source (215) and drain (240) regions. The source regions are self-aligned (210) and located below the pillars. The source regions of adjacent bitlines are isolated from each other without increasing the cell size and allowing a minimum area of approximately $4F^2$ to be maintained. The isolated sources allow individual cells to be addressed and written via direct tunneling, in both volatile and non-volatile memory cell (205) configurations. The source may be initially implanted. Alternatively, the source may be diffused below the pillars after forming thereof.

Fig. 8

This Sheet Has Been Replaced



THIS SHEET HAS BEEN REPLACED