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PATENT SPECIFICATION

DRAWINGS ATTACHED

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International Classification: —H 01 c, 1

COMPLETE SPECIFICATION

Miniature semiconductor Devices and Methods of Producing Same

We, TEXAS INSTRUMENTS INCORPORATED, of 13500 North Central Expressway, Dallas, Texas, United States of America, a corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement: —

This invention relates to miniature semiconductor devices and methods of producing same. More particularly, it relates to miniature semiconductor devices fabricated from semiconductor materials wherein two or more circuit elements are contained in a unitary structure of semiconductor material.

One proposal which has been put forward in the field of circuit miniaturization has been to include, within a semiconductor body, some circuit elements of a phase shift oscillator including an alloyed transistor having p-n junctions near opposite surfaces of the semiconductor body and a distributed R-C circuit element integrally connected to the base region of the transistor. The limitations of the proposed structure and steps required for its manufacture do not facilitate production techniques and do not allow the manufacture of unitary structures with a wide variety of circuit elements therein or versatility in the number and kind of circuit elements that may be embodiment in the unitary structure.

Some objects of the present invention are to provide a miniature semiconductor device and method of making same which facilitates production of the device, which allows versatility in the number and kind of circuit elements formed in or on a wafer of semiconductor material and which allows the manufacture of unitary structure with a wide variety of circuit elements therein.

The present invention is a miniature semiconductor device comprising a wafer of single crystal semiconductor material containing a first monocrystalline layer of one type conductivity forming a part of the surface of one major wafer face and a second monocrystalline layer of opposite type conductivity contiguous with said first layer to form therewith a p-n junction lying near said wafer face and extending thereto, said junction defining a first enclosed area on said face, the region immediately underlying said second layer being of said one type conductivity to form with said second layer another p-n junction extending to said face and there defining an enclosed area surrounding said first enclosed area, said wafer having discrete areas therein or thereon closely adjacent said one major wafer face and adapted to provide the electrical properties of two or more circuit elements which or at least two of which are different in kind from one another.

The present invention is also a method of producing a miniature semiconductor device comprising the steps of providing a wafer of single crystal semiconductor material, forming, in or on said wafer, a first monocrystalline layer of conductivity type opposite to that of the region immediately underlying it and forming therewith a p-n junction lying near one major wafer face and extending thereto to define a first enclosed area on said one major wafer face, forming, in or on said wafer, contiguous with said first layer, a second monocrystalline layer of conductivity type opposite to that of said first layer to form therewith another p-n junction extending to said one major face and there defining another enclosed area surrounded by said first

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mentioned enclosed area, and forming, within or on said wafer closely adjacent said one major wafer face, discrete areas adapted to provide the electrical properties of two or more circuit elements which or at least two of which are of a different kind.

The semiconductor device according to the invention generally has the circuit elements formed closely adjacent one major wafer face and to fabricate the device there may be utilized a combination of steps such as diffusion of conductivity type producing ingredients into a semiconductor wafer, masking in order to define predetermined areas of the wafer in which circuit elements are to be formed and mechanical and/or electrical shaping to confine paths for current flow.

Circuit elements with or on the semiconductor wafer may be effectively electrically isolated through the advantageous employment of electrical and/or mechanical shaping.

Shaping includes various ways of obtaining the confined current paths which ways include, as mechanical shaping, the removal of portions of the semiconductor material as by etching, and specialized configuration of the semiconductor material such as long and narrow, "L" shaped, "V" shaped, etc., and which ways further include, as electrical shaping, selective conversion of intrinsic semiconductor material by diffusion of impurities thereinto to provide low resistivity paths for current flow and selective conversion of semiconductor material of one conductivity-type to the opposite conductivity-type wherein the p-n junction thereby formed acts as a barrier to current flow.

The invention will be apparent from the following more complete discussion of the cooperative relationships which exist in the forming, shaping and positioning of the various areas within a wafer of single crystal semiconductor material to produce a miniature semiconductor device susceptible of exploitation in a variety of practical circuit embodiments.

In the accompanying drawings:—

Figures 1 to 5*a* illustrate schematically various circuit components, a number of which may be fabricated in accordance with the present invention in and/or on a wafer of single crystal semiconductor material to be adapted to form at least part of a miniature electrical circuit;

Figure 6*a* illustrates schematically a multivibrator circuit fabricated in accordance with the present invention;

Figure 6*b* shows the wiring diagram for the multivibrator circuit of Figure 6*a* laid out in the same relationship;

Figure 7 illustrates the wiring diagram of the multivibrator circuit of Figure 6*a* in a more conventional presentation;

Figure 8*a* illustrates schematically a phase shift oscillator fabricated in accordance with the present invention;

Figure 8*b* shows the wiring diagram for Figure 8*a* with the components laid out in the same relationship; and

Figure 8*c* portrays the wiring diagram of the phase shift oscillator.

Referring now to the drawings in detail, preferred embodiments of the present invention will now be described in detail in order that a better understanding of the invention and the various forms and embodiments of the invention may be obtained.

Figures 1—5 inclusive illustrate in detail circuit elements which can be formed in and/or a single wafer of semiconductor material in accordance with the present invention. It is noted at this point that the wafer of semiconductor material is of single crystal structure, and can be composed of any suitable semiconductor material. There may be mentioned as examples of suitable materials germanium, silicon, intermetallic alloys such as gallium arsenide, aluminium antimonide, indium antimonide, as well as others.

Referring particularly to Figure 1, there is shown a typical design for a resistor which may be formed in a wafer of single crystal semiconductor material with at least one other circuit element. As noted in Figure 1, the design contemplates utilizing the bulk resistance of a body 10 of semiconductor material of either n- or p-type conductivity. Contacts 11 and 12 are made ohmically to one surface of the body 10, spaced apart a sufficient distance to achieve a desired resistance. As will be apparent to one skilled in the art, ohmic connections are those which exhibit symmetry and linearity in terms of resistance to flow of current therethrough in any available direction. If two resistors are to be connected together, it is not necessary to provide separate terminations for the common point. The resistance may be calculated from

$$R = \rho L/A$$

where L is the active length in centimetres, A is the cross sectional area, and ρ is the resistivity in ohm-cm of the semiconductor material.

In addition or alternatively to the resistor shown in Figure 1, a resistor may be provided as shown in Figure 1*a* formed as part of a wafer of single crystal semiconductor material. In Figure 1*a*, there is shown a body comprising a region 10*a* of p-type semiconductor material and an n-type region 10*b*. Of course, between the region 10*a* and region 10*b* there is a p-n junction which is designated by the numeral 13. Contacts 11*a* and 12*a* are made to the outside surface of the region 10*b*, spaced apart from each other in order to achieve a desired resistance. As in Figure 1, the contacts 11*a* and 12*a* are ohmic contacts to the region 10*b*. A resistor formed

in the manner of Figure 1*a* has several important advantages. First, the p-n junction 13 provides a barrier to current flow from the n-type region 10*b* into the p-type region 10*a* and, thus, the current flow is confined to a path in the n-type region 10*b* between the contacts thereto. The second advantage is that the total resistance value thereof can be controlled to a large degree. The total-resistance value may be controlled by etching very lightly over the entire surface to remove the uppermost portion of the n-type region 10*b*, being very careful not to etch through the p-n junction. The third, and perhaps major, advantage in forming a resistor according to Figure 1*a* is in that, by controlling the doping level or impurity concentration in the n-type region 10*b*, lower and more nearly constant temperature coefficients may be provided for the resistor.

The above description has been in terms of a p-type region 10*a* and an n-type region 10*b* but it is obvious that the region 10*a* could be equally as well of n-type conductivity and the region 10*b* of p-type conductivity.

Capacitor designs may be obtained by utilizing the capacitance of a p-n junction, as shown in Figure 2, wherein is shown a semiconductor body comprising a region 15 of p-type conductivity and an n-type diffused region 16. Ohmic contacts 17 are made to opposite faces of the body 15,16. The capacitance of a diffused junction is given by

$$C = A\,\epsilon \left(\frac{qa}{12\,\epsilon\,V}\right)^{\frac{1}{3}}$$

where A is the area of the junction in square cm, ϵ is the dielectric constant, q is electronic charge, where a is the impurity density gradient and V is the applied voltage.

Instead of the capacitor of Figure 2, capacitance in a body of single crystal semiconductor material may be provided as shown and described in connection with Figure 2*a*, which capacitor is the subject of our co-pending patent application No. 5691/62 (Serial No. 945,737). Figure 2*a* shows a body 15*a* of single crystal semiconductor material, of either n- or p-type conductivity, which constitutes one plate of the capacitor. Evaporated onto the body 15*a* is a layer 18 providing a dielectric layer for the capacitor. It is necessary that the layer 18 have a suitable dielectric constant and be inert when in contact with the semiconductor body 15*a*. Silicon dioxide has been found to be a suitable material for dielectric layer 18 and may be applied by evaporation or thermal oxidation techniques onto body 15*a*. Plate 19 forms the other plate of the capacitor and is provided by evaporating a conductive material onto layer 18. Gold and aluminium have been found to be satisfactory materials for the plate 19. Ohmic contact 17*a* is made to the body of semiconductor material 15*a* and contact to plate 19 may be made by any suitable electrical contact (not shown). Capacitors formed in the manner described in connection with Figure 2*a* have been found to exhibit much more stable characteristics than pure junction capacitors, that is, p-n junction capacitors.

Capacitors produced in the manner of Figure 2 are also diodes, and must therefore be properly polarized in the circuit. Non-polar capacitors may be made by connecting two such areas back-to-back. Although junction capacitors have a marked voltage dependence, such dependence is present to a lesser degree for low voltages in the non-polar configuration.

Resistor and capacitor designs may be combined to form a distributed R-C network. Such is shown in Figure 3, wherein a body comprising a region 20 of p-type conductivity has an n-type conductivity diffused region 21 formed therein. A broad area contact 22 is placed on the diffused region on one face of the body and spaced contacts 23 on the opposite face of the body. These networks are useful for low pass-filters, phase shift networks, coupling elements, etc. Their parameters may be calculated from the equations above. Other configurations of this general type are also possible.

As shown in Figures 4 and 5, transistors and diodes may be formed on or in a single wafer. In Fig. 4, the transistor has a collector region 25, a diffused p-n junction 26, a base layer 27, an emitter contact 28 forming a rectifying connection with base layer 27 and base and collector contacts 29 and 30, respectively. The base layer 27 is formed as a mesa of small cross section. A diode of similar design is shown in Figure 5, and consists of region 35 of one type conductivity, and a mesa region 36 of opposite conductivity-type with a p-n diffused junction formed therebetween and contacts 37 and 48 connected to each region.

Small inductances, suitable for high frequency use, may also be made by shaping the semiconductor as evidenced by Figure 5*a*, which shows a spiral of semiconductor material. It is also possible to prepare photosensitive devices, including photovoltaic cells, photoresistors and solar cells and other like components utilizing the basic design considerations hereinbefore outlined.

Although all of the circuit elements have been described in terms of a single diffused layer, it is quite possible, where practical, to use a double diffused structure. Thus, double diffusion may be employed to form both n-p-n- and p-n-p transistor structures for example. Moreover, any suitable materials can be used for the semiconductor materials,

conductivity producing impurities, and contact materials; and suitable and known processing can be exploited to produce circuit element designs.

Because all of the circuit element designs described above can be formed from a single material, a semiconductor, it is possible by shaping to integrate all of them into a single crystal semiconductor wafer and to process the wafer to provide the proper network and the correct circuit element values.

As will be apparent to one skilled in the art, circuit elements can be classified according to their circuit functions. Thus, circuit elements may be thought of as being either active or passive in nature. Active elements are those which in an impedance network act as current generators; whereas passive elements do not so act, and the term "active element(s)" and "passive element(s)" where used hereinafter and in the claims are to be construed in this sense. Examples of active elements are photovoltaic cells and transistors; and examples of passive elements are resistors, capacitors and inductors. Elements which fall into the general category of diodes and are normally employed as passive elements, may if suitably biased and energized, function in an active nature.

A specific illustration of an electronic circuit embodying the invention is shown in Figure 6*a*. As shown, a thin wafer of single crystal semiconductor material contains a p-n junction formed between the monocrystalline layers, which wafer has been processed and shaped to include discrete areas adapted to provide the electrical properties of circuit elements forming a complete and integrated multivibrator electronic circuit closely adjacent one major wafer face. The regions of the wafer have been marked with symbols representative of the circuit element functions that are performed in the various regions. Figure 6*b* shows a wiring diagram of the various circuit functions in the relationship which they occupy in the wafer of Figure 6*a*. A more conventionally drawn circuit diagram is shown in Figure 7 with the circuit values actually used. The multivibrator circuit shown in Figures 6*a*, 6*b* and 7 will be described as illustrative of the processing techniques required. First, a wafer of single crystal semiconductor material, preferably silicon or germanium, of the proper resistivity is lapped and polished on one side. For this design, 3 ohm-cm p-type germanium was used. The wafer was then subjected to an antimony diffusion process which produced a monocrystalline n-type layer on the surface about 0.7 mils deep. The wafer was then cut to the proper size, 0.200×080 inches, and the unpolished surface lapped to give a wafer thickness of 0.0025 inches.

Gold plated Kovar (Registered Trade Mark) leads 50 were attached by alloying to the wafer in the proper positions. Kovar is a trade name for an iron-nickel-cobalt alloy. Gold was then evaporated through a mask to provide the areas 51—54 which provide ohmic contact with the n layer, such as the transistor base connections and the capacitor contacts. Aluminium was evaporated through a properly shaped mask to provide the transistor emitter areas 56, which form rectifying contacts with the n layer. Alternately a p-type conductivity producing ingredient may be diffused through a properly shaped mask to provide the transistor emitter areas 56. Suitable ohmic contacts may be secured to the emitter areas in the same manner as the securing of contacts 53 and 54 to base areas of transistors T_2 and T_1. When the emitter area is formed either by diffusion or alloying a monocrystalline layer of conductivity type opposite to that of the base region is provided. The monocrystalline layers of the base and emitter regions are contiguous and form therebetween a p-n junction extending to the major wafer face and there denfining an enclosed area of semiconductor material.

In the completed device the p-n junction formed between the collector and base regions also extends to the major wafer face and there defines an enclosed area of semiconductor material surrounding the first mentioned enclosed area.

The wafer was then coated with a photosensitive resist or lacquer, such as Eastman (Registered Trade Mark) Photo Resist, supplied by Eastman Kodak Company, and exposed through a negative to a light. The lacquer image remaining after development was used as a resist for etching the wafer to the proper shape. In particular, this etching forms a slot through the wafer to provide an isolation volume between R_1 and R_2 thereby electrically isolating R_1 and R_2 from each other along at least a major part of their lengths and from the rest of the circuit elements. This etching also shapes all of the resistor areas to the previously calculated configuration. Either chemical etching or electrolytic etching may be used, although electrolytic etching appears to be preferable.

After this step, the photoresist was removed with a solvent, and the areas 60, and such other areas as necessary, were masked by the same photographic process. The wafer was again immersed in etchant, and the n layer completely removed in the exposed areas thereby forming the mesa shapes. A chemical etch is considered preferable. The photoresist was then removed.

Gold wires 70 were then thermally bonded to the appropriate areas to complete the connections, and a final clean-up etch given. Instead of using the gold wires 70 in making electrical connections, connections may be provided in other ways. For example, in accordance with the present invention des-

cribed in our co-pending patent application No. 3836/63 (Serial No. 945738), an insulating and inert material such as silicon oxide may be evaporated onto the semiconductor circuit wafer through a mask either to cover the wafer completely except at the points where electrical contact is to be made thereto, or to cover only selected portions joining the points to be electrically connected. Electrically conducting material such as gold may then be laid down on the insulating material to make the necessary electrical circuit connections.

Although Fig. 6*a* has been described embodying resistors according to Fig. 1, it will be manifest that the resistors may be constructed according to Fig. 1*a*, i.e. diffused resistors may be substituted, where desired and practical, for the bulk resistors illustrated.

After testing, the circuit may be hermetically sealed, if required, for protection against contamination. The finished device was smaller by several orders of magnitude than any others which have previously been proposed. Because the fabrication steps required are quite similar to those now used in manufacturing transistors, and because of the relatively small number of steps required, these devices are inherently inexpensive and reliable, as well as compact.

A further illustration of the present invention is shown in Figures 8*a* to 8*c*. Each area of the single crystal semiconductor wafer has been marked with a symbol for the circuit element which it represents. This unit illustrates the use of resistors, transistors, and a distributed R-C network to form a complete phase shift oscillator.

Specifically, Fig. 8*a* shows three resistance-exhibiting areas R_1, R_2 and R_3, these areas being defined by several tabs or contacts which are located on the semiconductor wafer. The resistor R_1 is defined by the contacts marked "−V" and "output", the resistor R_2 by the contact marked "output" and the contact not marked, and the resistance R_3 by the latter contact and that marked "+V". The layer defined just above the resistor R_2 and lying on the semiconductor wafer includes the dielectric layer for the capacitor C_1 and includes a metallic plate positioned thereon, this resulting in a distributed capacitance element. The transistor Q_1 is located in the semiconductor wafer at the junction of the resistors R_1 and R_2 and has its collector electrode internally connected at the junction of R_1 and R_2. The base electrode of the transistor Q_1 is coupled externally to the junction of the resistors R_2 and R_3, the emitter electrode of the transistor Q_1 is coupled to the source of positive voltage by an external connection, and the capacitor plate C_1 is coupled to the source of positive voltage by an external connection. The end result is the network represented schematically in Fig. 8*c*, which is a complete phase shift oscillator circuit.

It must be emphasized that the two embodiments described above are merely two of innumerable networks which can be fabricated by the techniques of the present invention. There is no limit upon the complexity of configuration of circuits which can be made in this manner, for example any desired cooperative combination of selected circuit elements as hereinbefore described with reference to Figs. 1 to 5*a* may be embodied in a single wafer to form a network and the network may be such that upon the application of electrical power, there is performed within the structure an electrical function equivalent to the function performed by a plural element electrical network. While there is a limit upon the types and values of circuit elements which can be made in a limited space, the invention hereof nevertheless represents a remarkable improvement over the prior art. As evidence of the advance in the art accomplished by the present invention, it is possible using the technique described above to achieve component densities of greater than thirty million per cubic foot as compared with five hundred thousand per cubic foot which is the highest component densities attained prior to this invention.

Reference is additionally made to our copending parent patent application No. 3633/60 (Serial No. 945,734) and copending applications Nos. 27196/63, 27195/63, 27326/63, 27197/63, 32744/63 28004/63, 27198/63, 28005/63, 27540/63 and 27541/63 Serial Nos 945740, 945739, 945743, 945741, 945749, 945747, 945742, 945748, 945744, and 945745. which are also divided out of application 3633/60 (Serial No 945734).

Terms indicative of position, such as "on", "overlying" and underlying", are used in the following claims to define relationship of parts in a form convenient for the purpose, but such terms are not to be construed in any restrictive sense and it will be manifest that the semiconductor devices could be utilised in any desired positional orientation.

WHAT WE CLAIM IS:—

1. A miniature semiconductor device comprising a wafer of single crystal semiconductor material containing a first monocrystalline layer of one type conductivity forming a part of the surface of one major wafer face and a second monocrystalline layer of opposite type conductivity contiguous with said first layer to form therewith a p-n junction lying near said wafer face and extending thereto, said junction defining a first enclosed area on said face, the region immediately underlying said second layer being of said one type conductivity to form with said second layer another p-n junction extending to said face and there defining an enclosed area surrounding said first enclosed area, said wafer having

cribed in our co-pending patent application No. 3836/63 (Serial No. 945738), an insulating and inert material such as silicon oxide may be evaporated onto the semiconductor circuit wafer through a mask either to cover the wafer completely except at the points where electrical contact is to be made thereto, or to cover only selected portions joining the points to be electrically connected. Electrically conducting material such as gold may then be laid down on the insulating material to make the necessary electrical circuit connections.

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After testing, the circuit may be hermetically sealed, if required, for protection against contamination. The finished device was smaller by several orders of magnitude than any others which have previously been proposed. Because the fabrication steps required are quite similar to those now used in manufacturing transistors, and because of the relatively small number of steps required, these devices are inherently inexpensive and reliable, as well as compact.

A further illustration of the present invention is shown in Figures 8*a* to 8*c*. Each area of the single crystal semiconductor wafer has been marked with a symbol for the circuit element which it represents. This unit illustrates the use of resistors, transistors, and a distributed R-C network to form a complete phase shift oscillator.

Specifically, Fig. 8*a* shows three resistance-exhibiting areas R_1, R_2 and R_3, these areas being defined by several tabs or contacts which are located on the semiconductor wafer. The resistor R_1 is defined by the contacts marked "−V" and "output", the resistor R_2 by the contact marked "output" and the contact not marked, and the resistance R_3 by the latter contact and that marked "+V". The layer defined just above the resistor R_3 and lying on the semiconductor wafer includes the dielectric layer for the capacitor C_1 and includes a metallic plate positioned thereon, this resulting in a distributed capacitance element. The transistor Q_1 is located in the semiconductor wafer at the junction of the resistors R_1 and R_2 and has its collector electrode internally connected at the junction of R_1 and R_2. The base electrode of the transistor Q_1 is coupled externally to the junction of the resistors R_2 and R_3, the emitter electrode of the transistor Q_1 is coupled to the source of positive voltage by an external connection, and the capacitor plate C_1 is coupled to the source of positive voltage by an external connection. The end result is the network represented schematically in Fig. 8*c*, which is a complete phase shift oscillator circuit.

It must be emphasized that the two embodiments described above are merely two of innumerable networks which can be fabricated by the techniques of the present invention. There is no limit upon the complexity of configuration of circuits which can be made in this manner, for example any desired cooperative combination of selected circuit elements as hereinbefore described with reference to Figs. 1 to 5*a* may be embodied in a single wafer to form a network and the network may be such that upon the application of electrical power, there is performed within the structure an electrical function equivalent to the function performed by a plural element electrical network. While there is a limit upon the types and values of circuit elements which can be made in a limited space, the invention hereof nevertheless represents a remarkable improvement over the prior art. As evidence of the advance in the art accomplished by the present invention, it is possible using the technique described above to achieve component densities of greater than thirty million per cubic foot as compared with five hundred thousand per cubic foot which is the highest component densities attained prior to this invention.

Reference is additionally made to our copending parent patent application No. 3633/60 (Serial No. 945,734) and copending applications Nos. 27196/63, 27195/63, 27326/63, 27197/63, 32744/63 28004/63, 27198/63, 28005/63, 27540/63 and 27541/63 Serial Nos 945740, 945739, 945743, 945741, 945749, 945747, 945742, 945748, 945744, and 945745. which are also divided out of application 3633/60 (Serial No 945734).

Terms indicative of position, such as "on", "overlying" and underlying", are used in the following claims to define relationship of parts in a form convenient for the purpose, but such terms are not to be construed in any restrictive sense and it will be manifest that the semiconductor devices could be utilised in any desired positional orientation.

WHAT WE CLAIM IS:—

1. A miniature semiconductor device comprising a wafer of single crystal semiconductor material containing a first monocrystalline layer of one type conductivity forming a part of the surface of one major wafer face and a second monocrystalline layer of opposite type conductivity contiguous with said first layer to form therewith a p-n junction lying near said wafer face and extending thereto, said junction defining a first enclosed area on said face, the region immediately underlying said second layer being of said one type conductivity to form with said second layer another p-n junction extending to said face and there defining an enclosed area surrounding said first enclosed area, said wafer having

discrete areas therein or thereon closely adjacent said one major wafer face and adapted to provide the electrical properties of two or more circuit elements which or at least two of which are different in kind from one another.

2. A miniature semiconductor device according to claim 1, wherein one of said discrete areas is adapted to provide the electrical properties of an active circuit element and the other or another of said discrete areas is adapted to provide the electrical properties of a passive circuit element.

3. A miniature semiconductor device according to either preceding claim, wherein said control layer is a diffused layer.

4. A miniature semiconductor device according to claim 1, wherein said discrete areas are adapted to provide the electrical properties of active and passive circuit elements selected from the group consisting of transistors, diodes, resistors, capacitors, inductors, elements displaying both resistance and capacitance, photosensitive devices, and power generating devices, said circuit elements being of a number and kind necessary to form a predetermined electrical network and being positioned in said wafer so that predetermined ones of said elements are interconnected internally through said wafer, and external connectors being secured to said wafer to complete said network.

5. A miniature semiconductor device according to any of claims 1 to 3, including means electrically connecting predetermined ones of said elements.

6. A miniature semiconductor device according to any preceding claim, wherein at least one of said discrete areas provides the electrical properties of either a photosensitive device, a power generating device, or an inductor.

7. A miniature semiconductor device according to any of claims 1 to 5, wherein at least one of said discrete areas provides the electrical properties of a resistor, and a further PN junction constitutes a boundary for said at least one of said discrete areas.

8. A miniature semiconductor device according to any preceding claim, including a plurality of contacts positioned on a major face of the wafer, each of said contacts defining a terminal portion of at least one of said discrete areas.

9. A miniature semiconductor device according to claims 2 and 3, wherein said active circuit element is a transistor, and said passive circuit element is an inductor, capacitor or distributed resistance capacitance element.

10. A miniature semiconductor device according to any preceding claim, wherein selected ones of said discrete areas are isolated from one another through the wafer.

11. A miniature semiconductor device according to any preceding claim wherein said first layer is a diffused layer.

12. A miniature semiconductor device according to claim 1, including a plurality of electrical contacts secured to the wafer on a major face thereof and spaced from one another with at least one of the electrical contacts being on said first monocrystalline layer, and a plurality of electrically conductive leads selected ones of which electrically interconnect predetermined ones of said contacts; said wafer, said discrete areas, said electrical contacts and said conductive leads being so arranged and constructed as to allow, upon the application of electrical power, the performance within the structure of an electrical function equivalent to the function performed by a plural element electrical network.

13. A miniature semiconductor device according to claim 12 and hermetically sealed.

14. A method of producing a miniature semiconductor device comprising the steps of providing a wafer of single crystal semiconductor material, forming, in or on said wafer, a first monocrystalline layer of conductivity type opposite to that of the region immediately underlying it and forming therewith a p-n junction lying near one major wafer face and extending thereto to define a first enclosed area on said one major wafer face, forming, in or on said wafer, contiguous with said first layer, a second monocrystalline layer of conductivity type opposite to that of said first layer to form therewith another p-n junction extending to said one major wafer face and there defining another enclosed area surrounded by said first mentioned enclosed area, and forming, within or on said wafer closely adjacent said one major wafer face, discrete areas adapted to provided the electrical properties of two or more circuit elements which or at least two of which are of a different kind.

15. A method according to claim 14, wherein one of said discrete areas is adapted to provide the electrical properties of an active circuit element and the other or another of said discrete areas is adapted to provide the electrical properties of a passive circuit elements which or at least two of which are of a different kind.

15. A method according to claim 14, wherein one of said discrete areas is adapted to provide the electrical properties of an active circuit element and the other or another of said discrete areas is adapted to provide the electrical properties of a passive circuit element.

16. A method according to claim 14 or 15, wherein said first layer is formed by diffusion.

17. A method according to any of claims 14 to 16, including the step of treating said wafer to obtain electrical isolation between predetermined ones of said discrete areas.

18. A method according to any of claims 14 to 16, including the step of treating said wafer to obtain electrical isolation between predetermined ones of said discrete areas, whereby predetermined ones of said areas retain their internal interconnections, and connecting together predetermined ones of said discrete areas externally of said wafer to form at least part of a circuit.

19. A method according to any of claims 14 to 17, wherein said discrete areas are adapted to provide the electrical properties of active and passive circuit elements selected from the group consisting of transistors, diodes, resistors, capacitors, inductors, elements displaying both resistance and capacitance, photosensitive devices, and power generating devices, said circuit elements being of a number and kind necessary to form a preselected electrical network and being positioned in distinct areas of said wafer so that predetermined ones of said circuit elements are connected together internally of said wafer, and external connectors are secured to said wafer to complete said network.

20. A method according to any of claims 14 to 19, wherein at least one of said discrete areas provides the electrical properties of either a photosensitive device, power generating device, or inductor.

21. A method according to any of claims 14 to 20, wherein at least one of said discrete areas provides the electrical properties of a resistor, and a further PN junction constitutes a boundary for said at least one of said discrete areas.

22. A method according to any of claims 14 to 21, including the step of positioning a plurality of contacts on a major face of the wafer so that each of said contacts defines a terminal portion of at least one of said discrete areas.

25. A semiconductor device when produced by the method claimed in any of claims 14 to 22.

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PATENTS ACT, 1949

SPECIFICATION NO. 945,746

In accordance with the Decision of the Superintending Examiner, acting for the Comptroller-General, dated the 24th day of March 1965 this Specification has been amended under Section 29 in the following manner:-

Page 5, line 2, *for* "3836/63" *read* "27541/63" *for* "945,738" *read* "945,745"

Page 5, line 101, *for* "27541/63" *read* "3836/63" *for* "945,745" *read* "945,738"

Attention is also directed to the following printer's errors:-

Page 6, line 16, *for* "control" *read* "second"

Page 6, *delete* lines "109 to 116"

THE PATENT OFFICE,
4th May 1965

D 37496/12