DETECTION OF CLOCK SIGNAL PERIOD ABNORMALITIES

ABSTRACT OF DISCLOSURE

A clock monitoring circuit (106) is disclosed for detecting that the period of a clock signal has become shorter than a predetermined time interval. The clock monitoring circuit (106) comprises a first and second flip-flop circuits (116,117) that are D-type flip-flop, a delay circuit (115), and a gate circuit (117). The second flip-flop circuit (114) receives as an input signal the output signal of the first flip-flop circuit (116). The output signal of the second flip-flop circuit (114) is delayed a fixed time interval by the delay circuit (115) and then supplied as an input signal to the first flip-flop circuit (116). The delay time of the delay circuit is set to be equal to the previously described predetermined period. The gate circuit (117) receives the output signals of the first and second flip-flop circuits (116, 114), and provides a signal whose logic level when the period of the received clock signal is the predetermined period differs from that when it is shorter than the predetermined period.

Fig.2