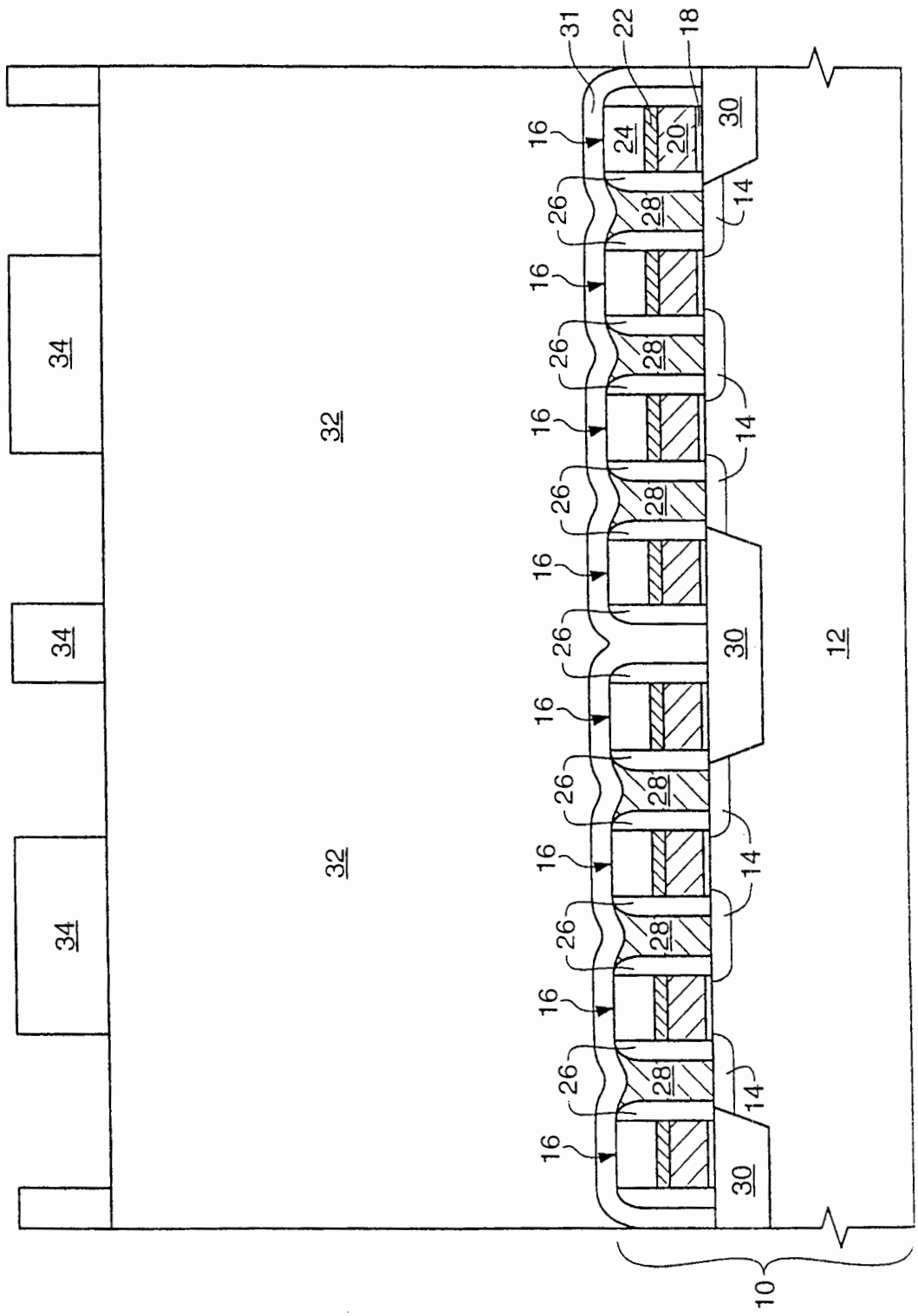


FIG. 1 (PRIOR ART)

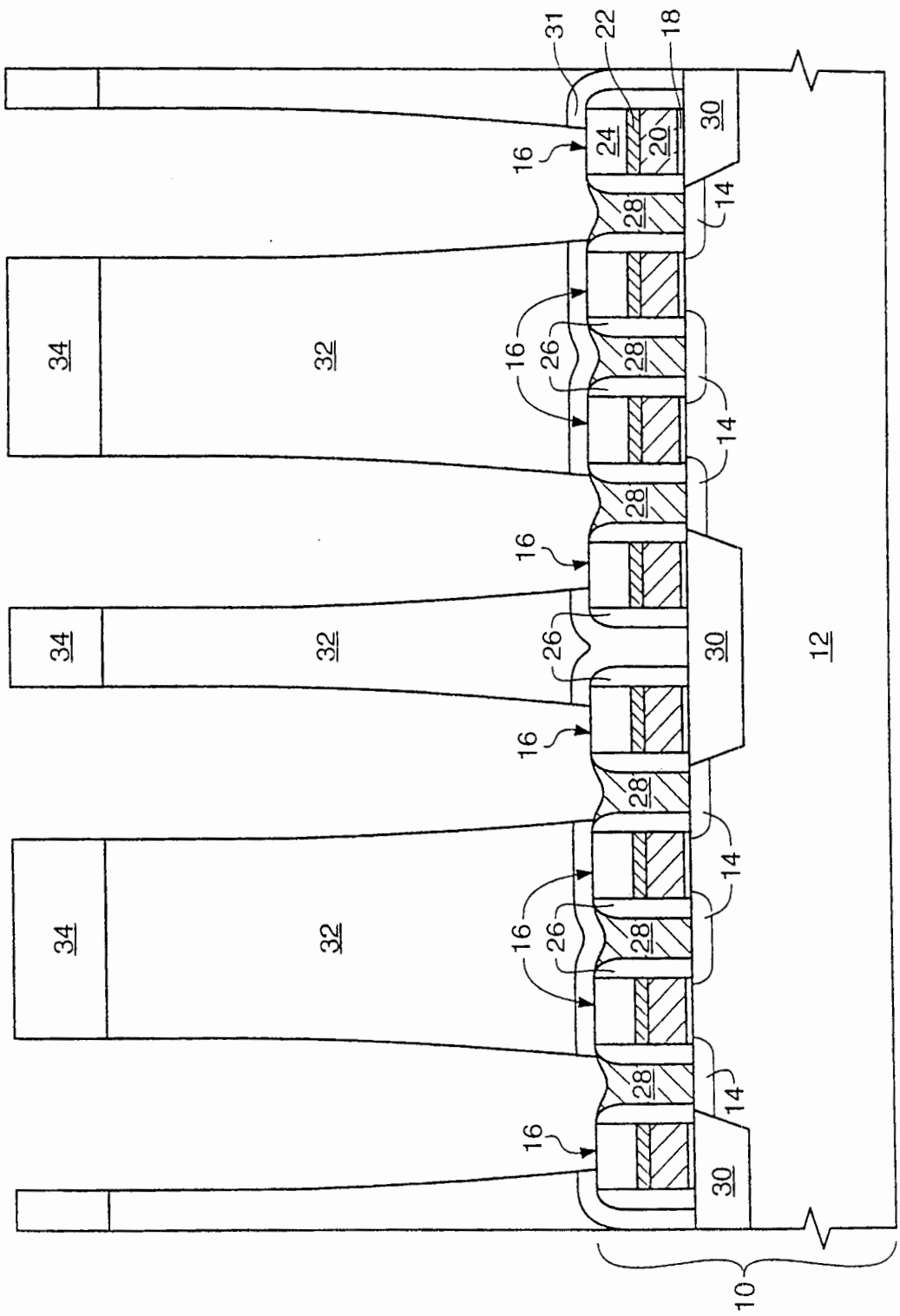


FIG. 2 (PRIOR ART)

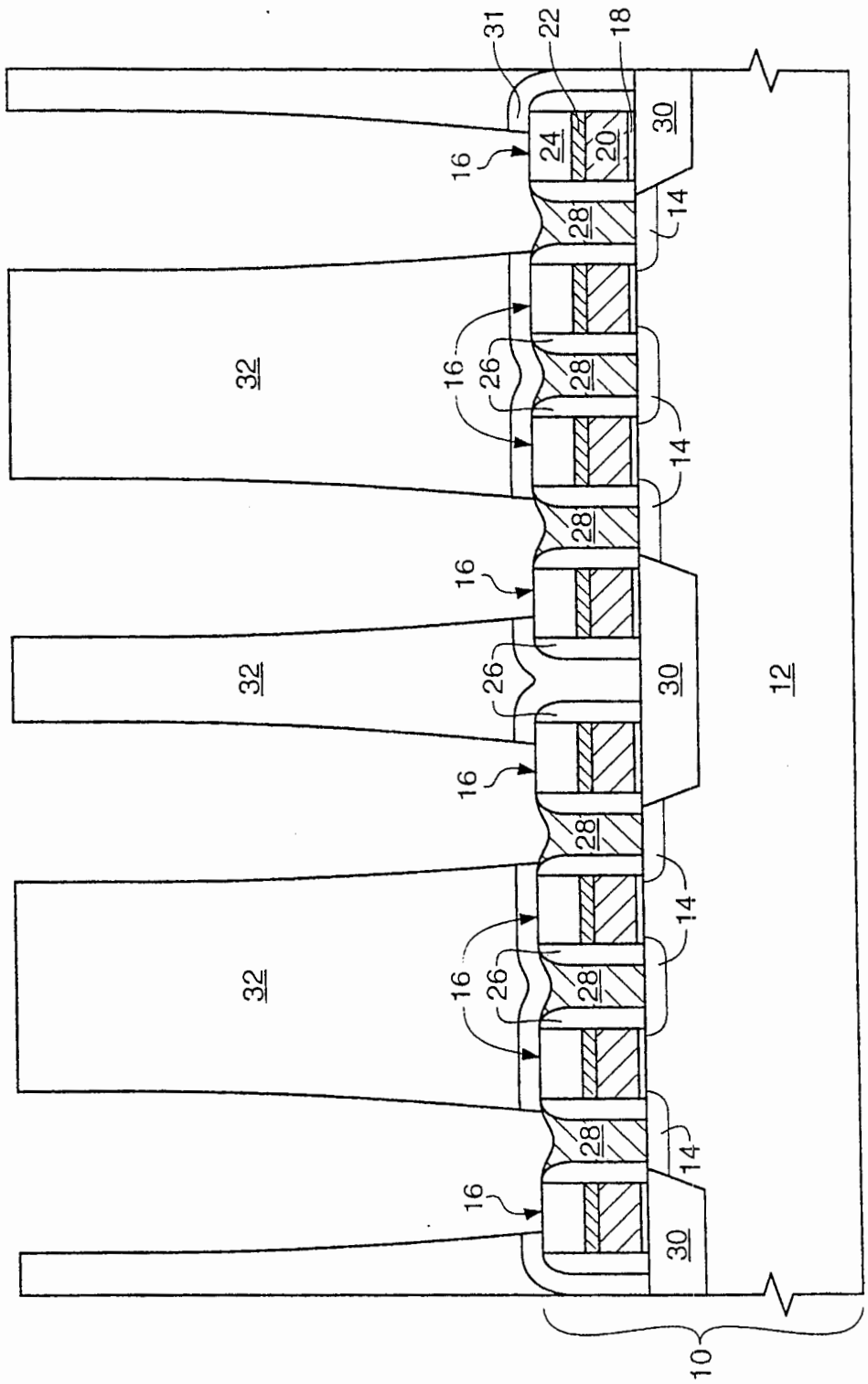


FIG. 3 (PRIOR ART)

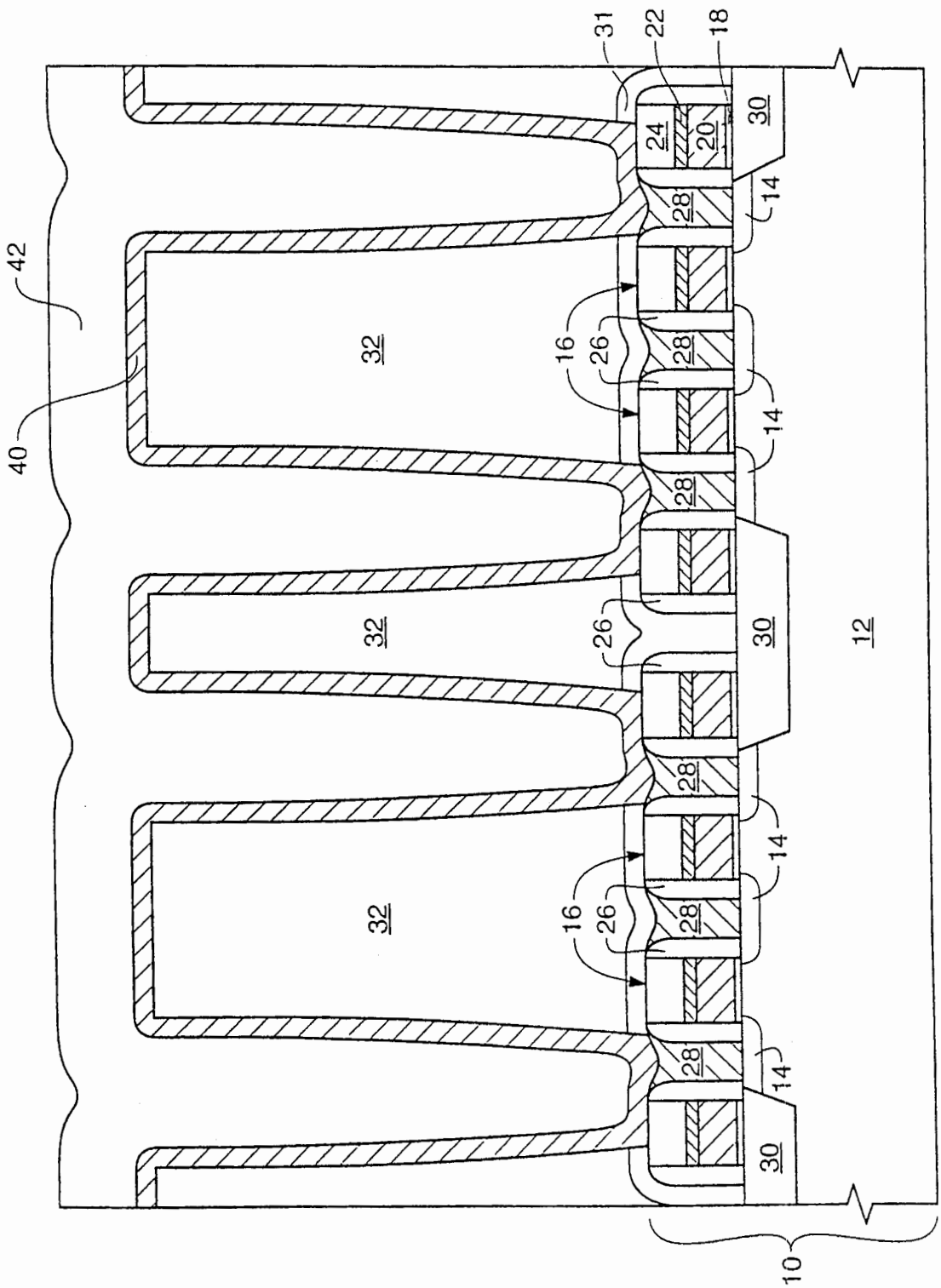


FIG. 4 (PRIOR ART)

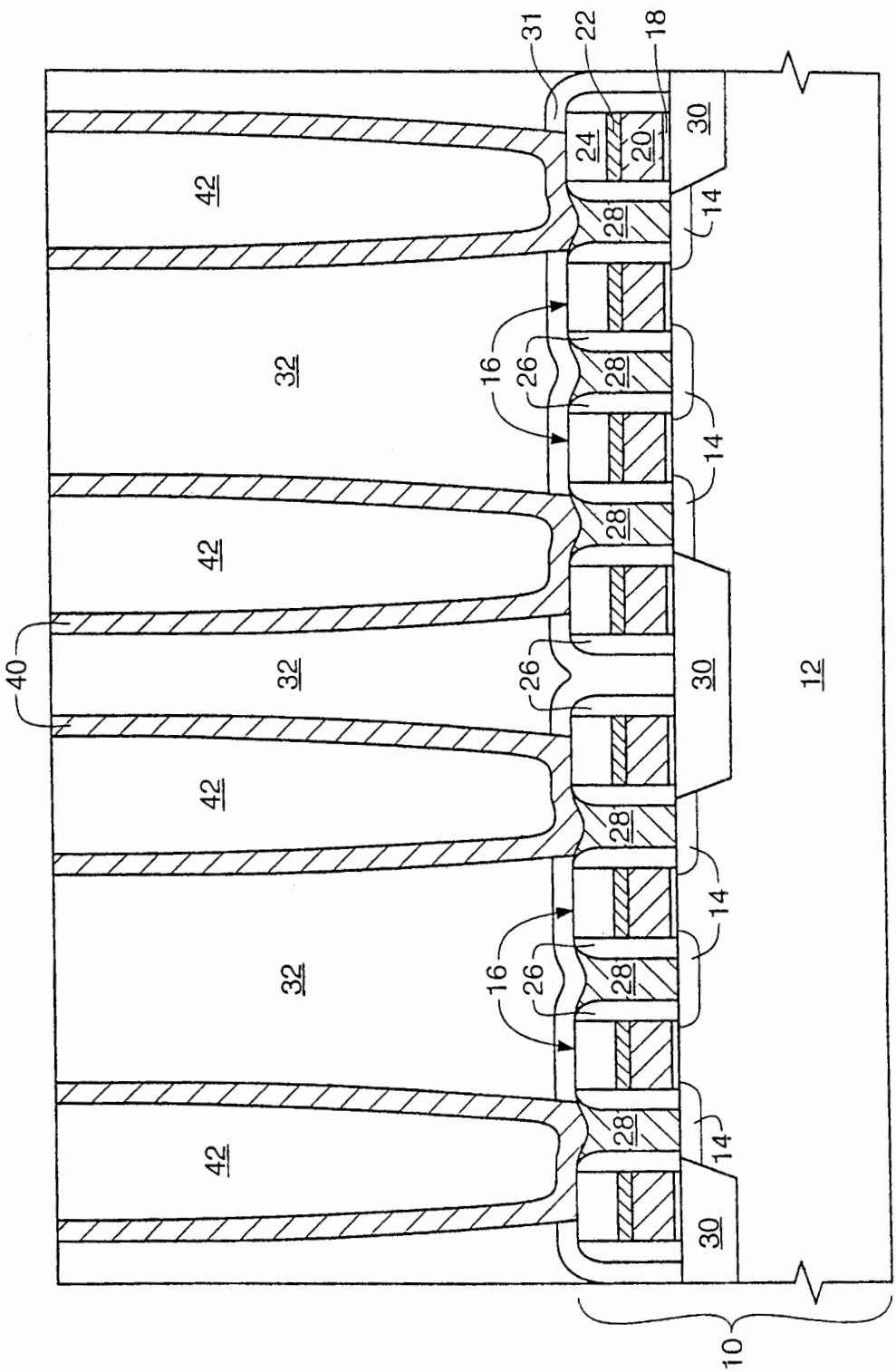


FIG. 5 (PRIOR ART)

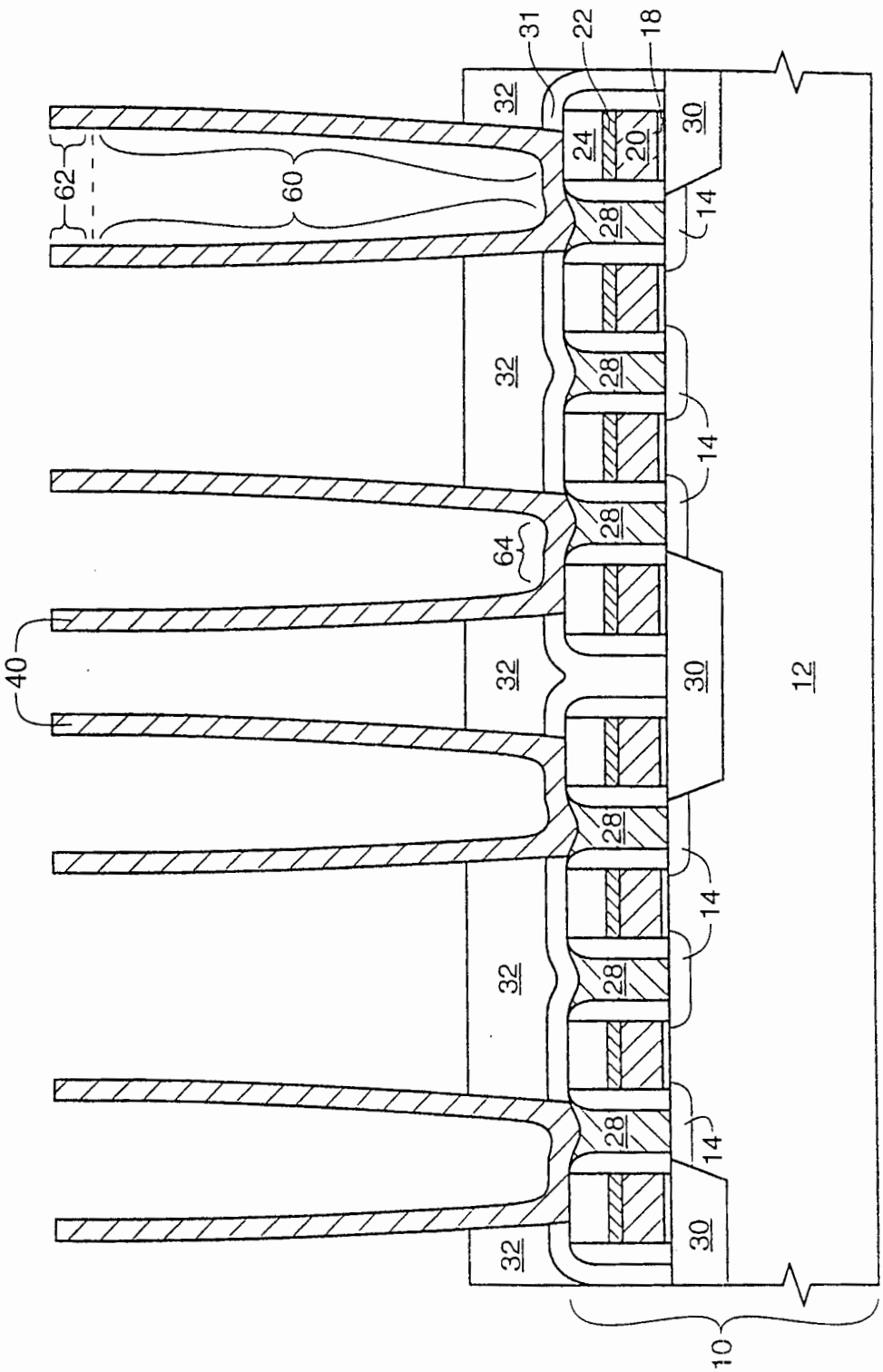


FIG. 6 (PRIOR ART)

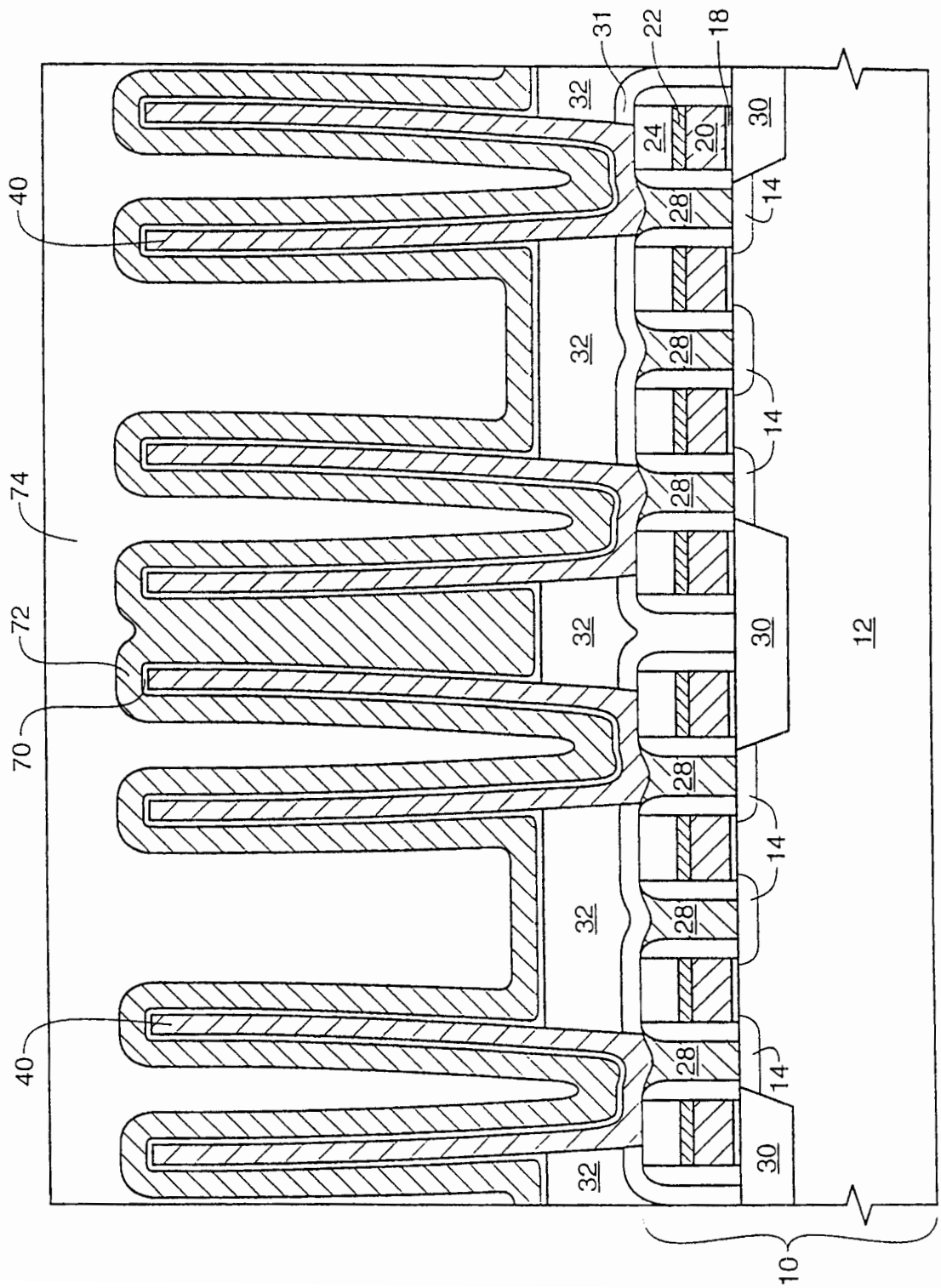


FIG. 7 (PRIOR ART)

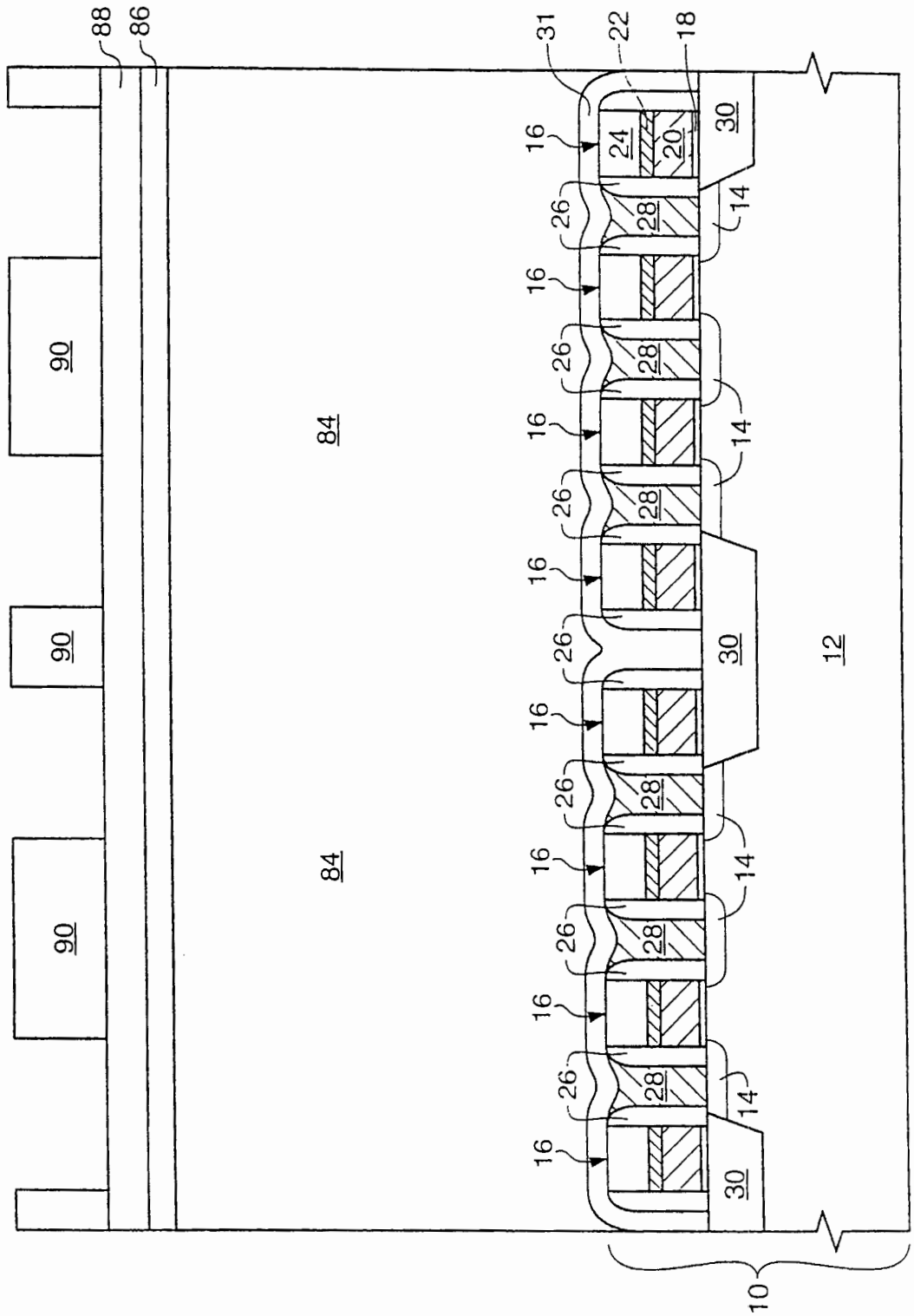


FIG. 8

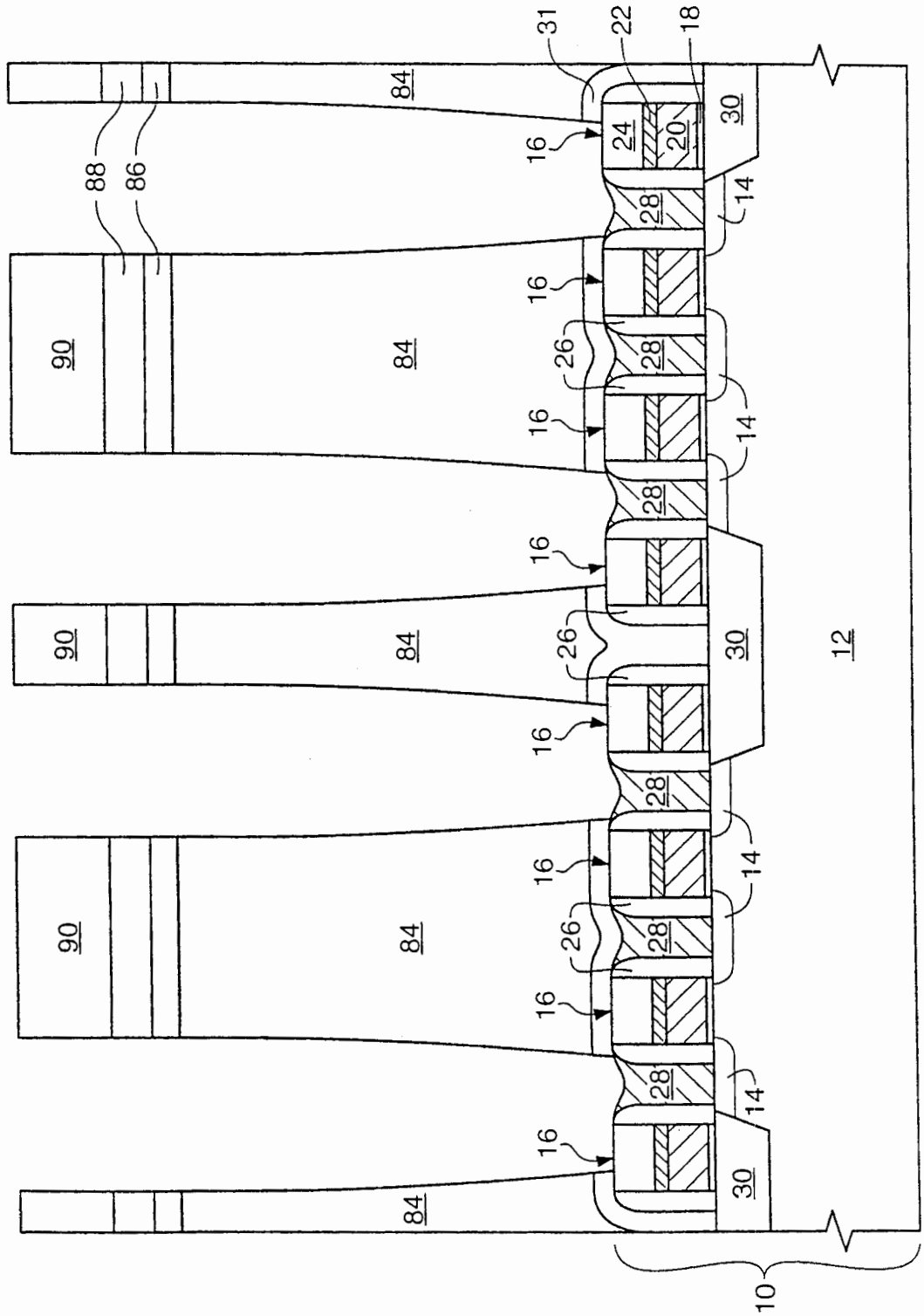


FIG. 9

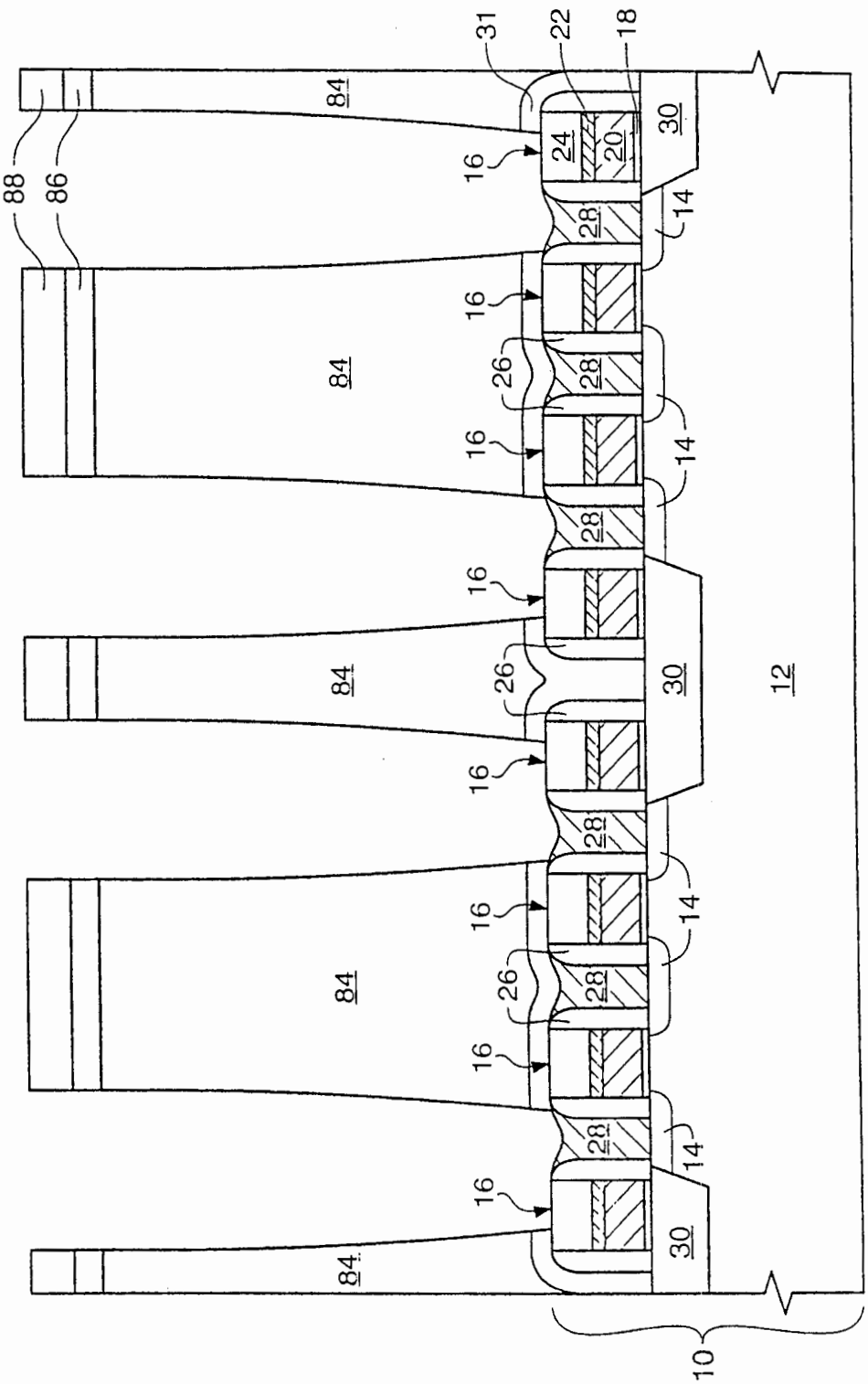


FIG. 10

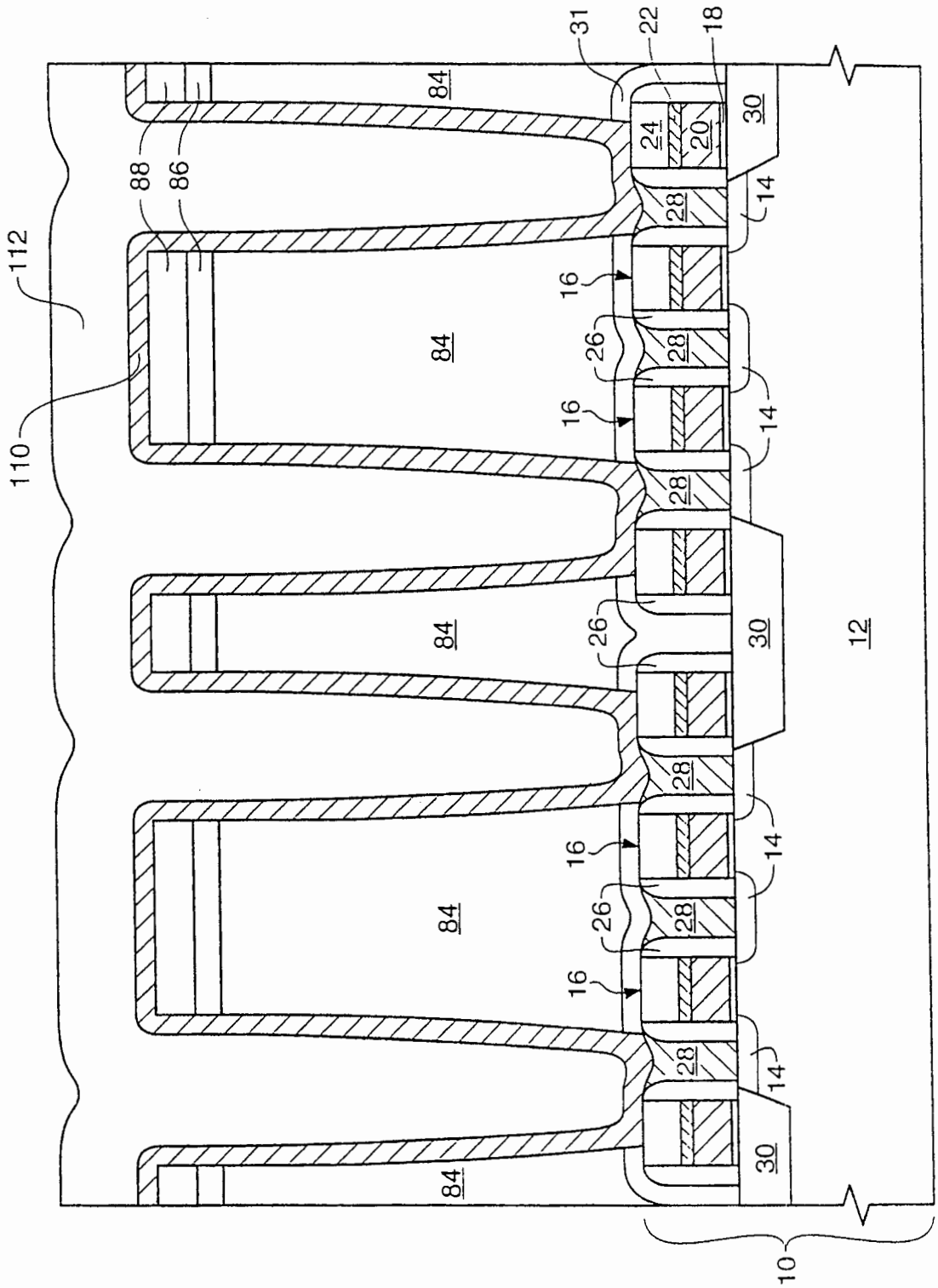


FIG. 11

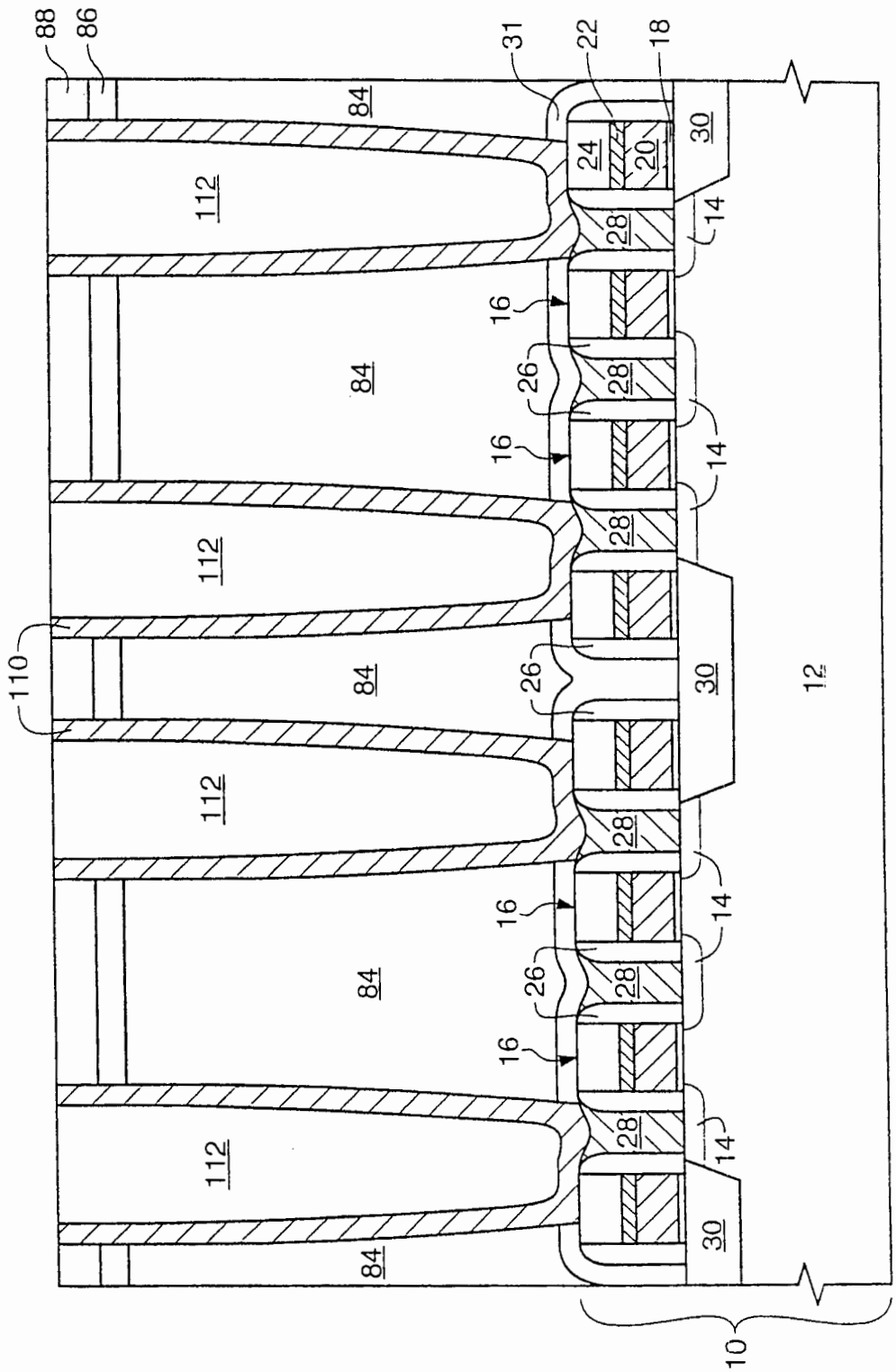


FIG. 12

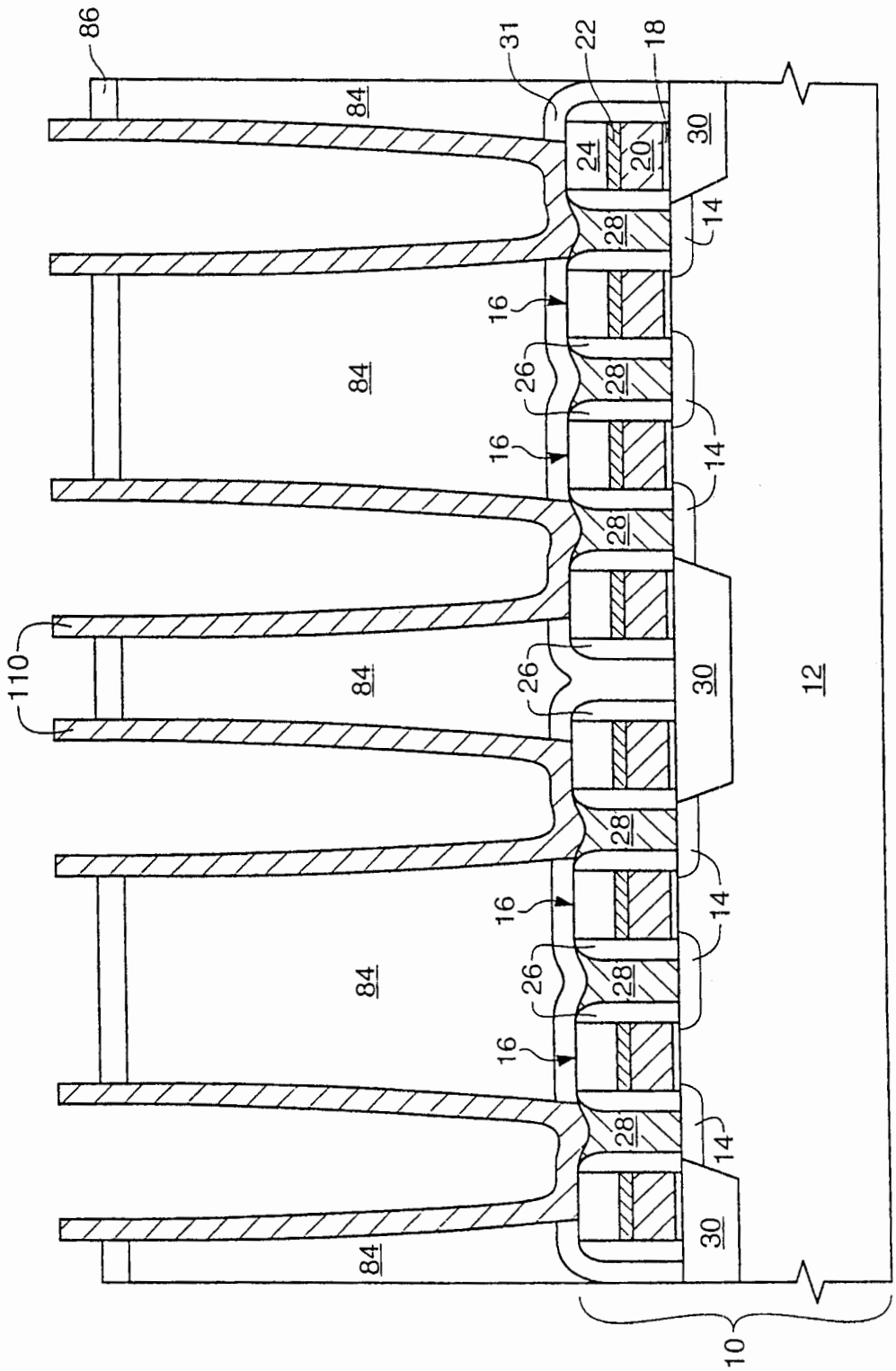


FIG. 13

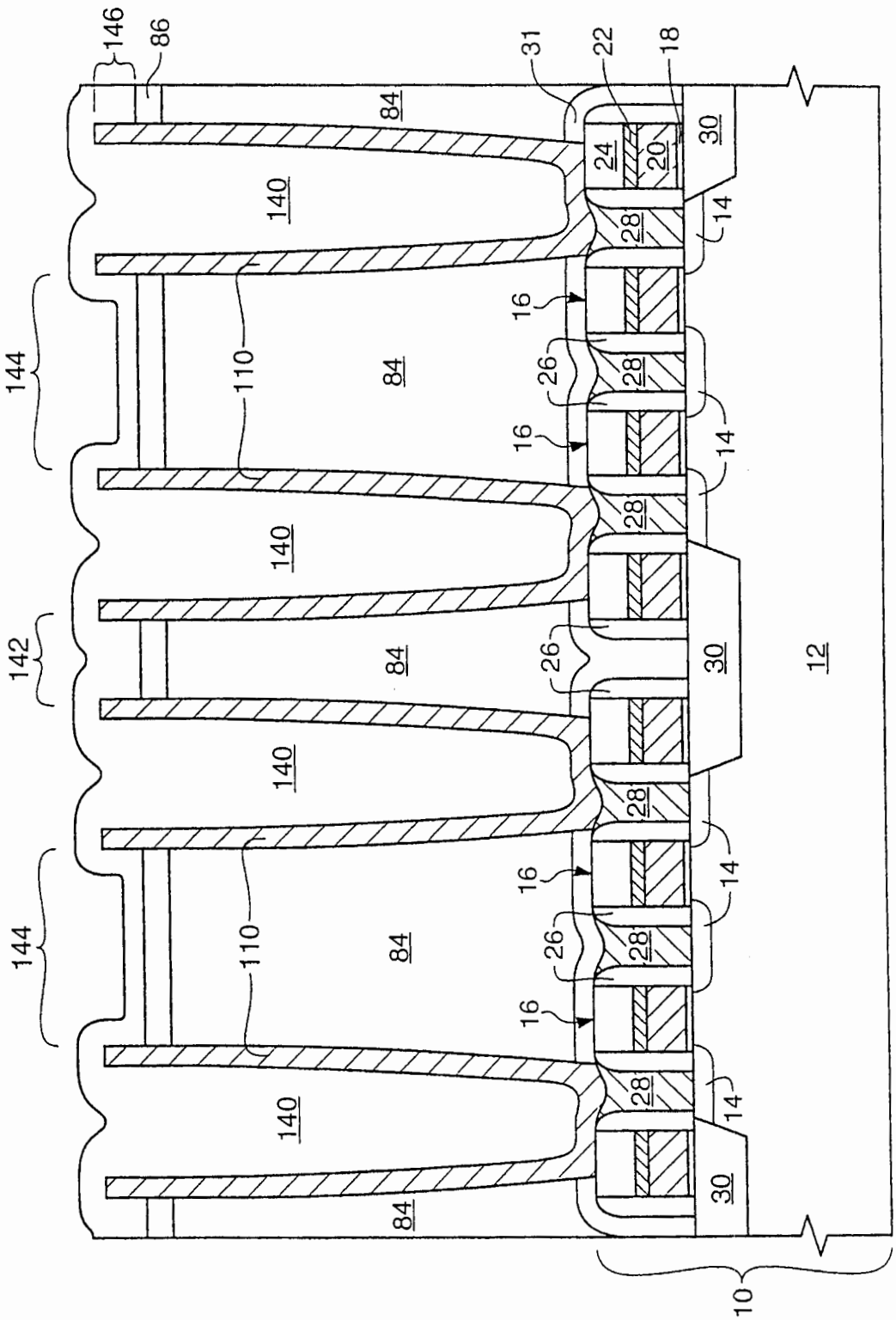


FIG. 14

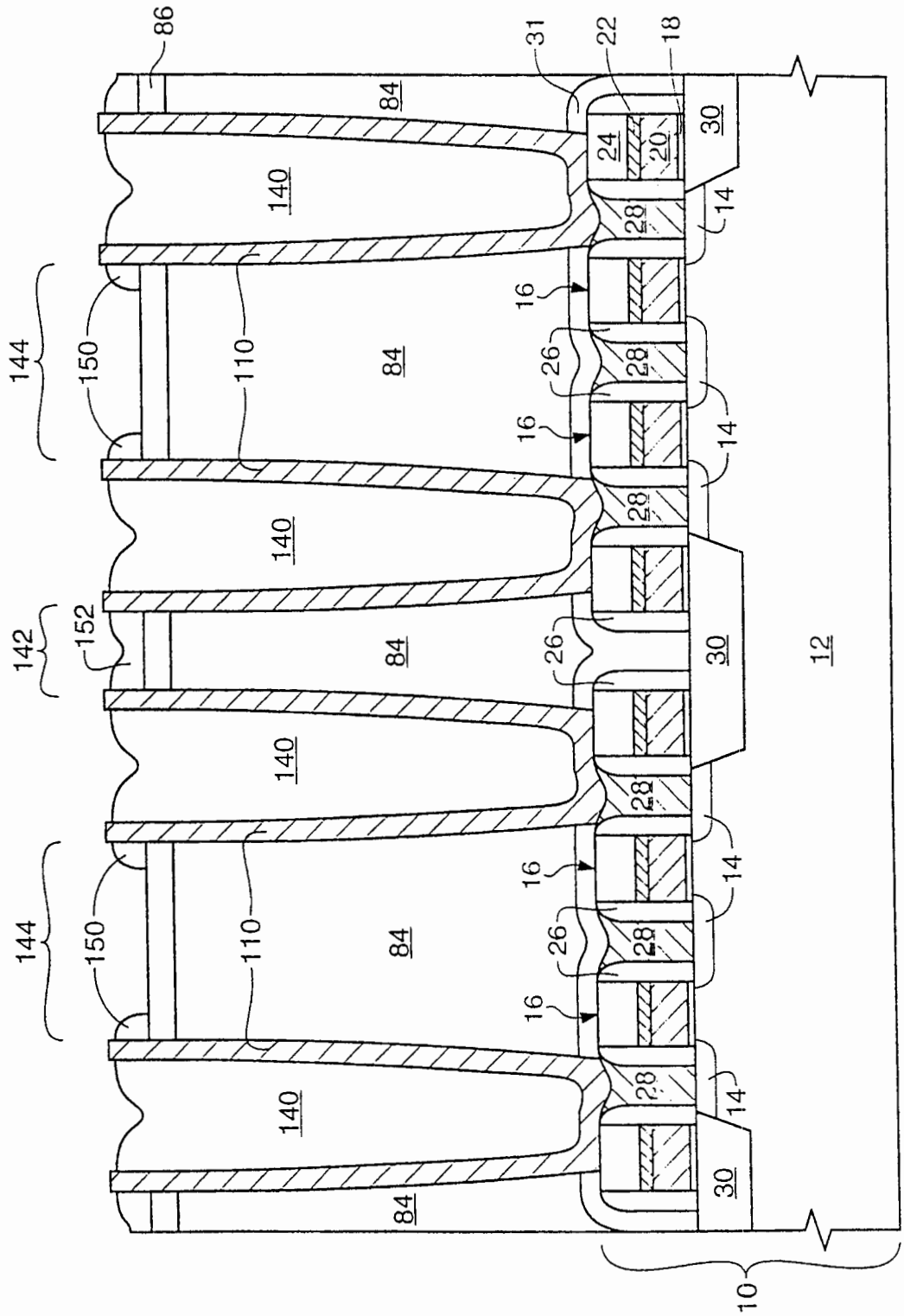


FIG. 15

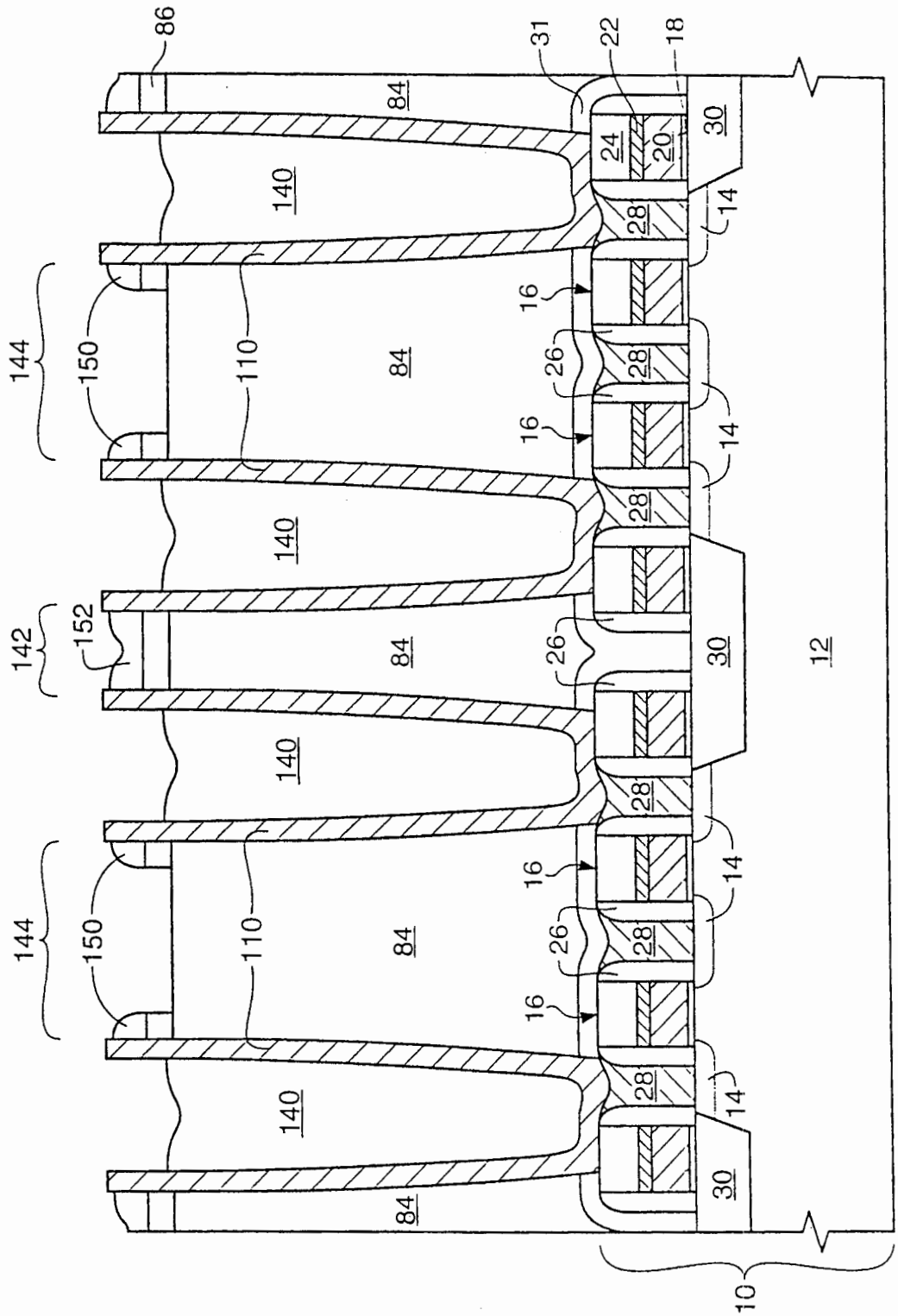


FIG. 16

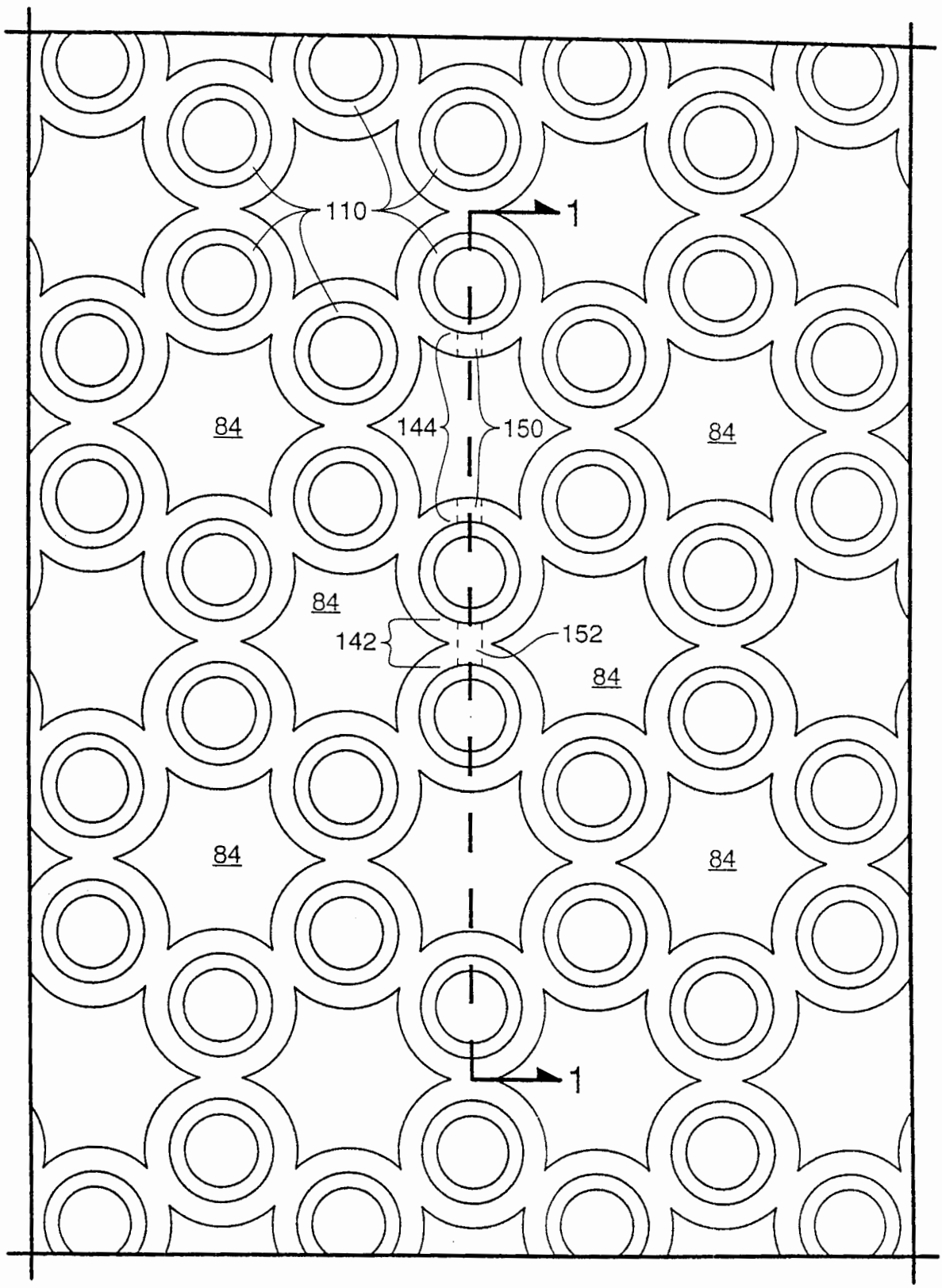


FIG. 17

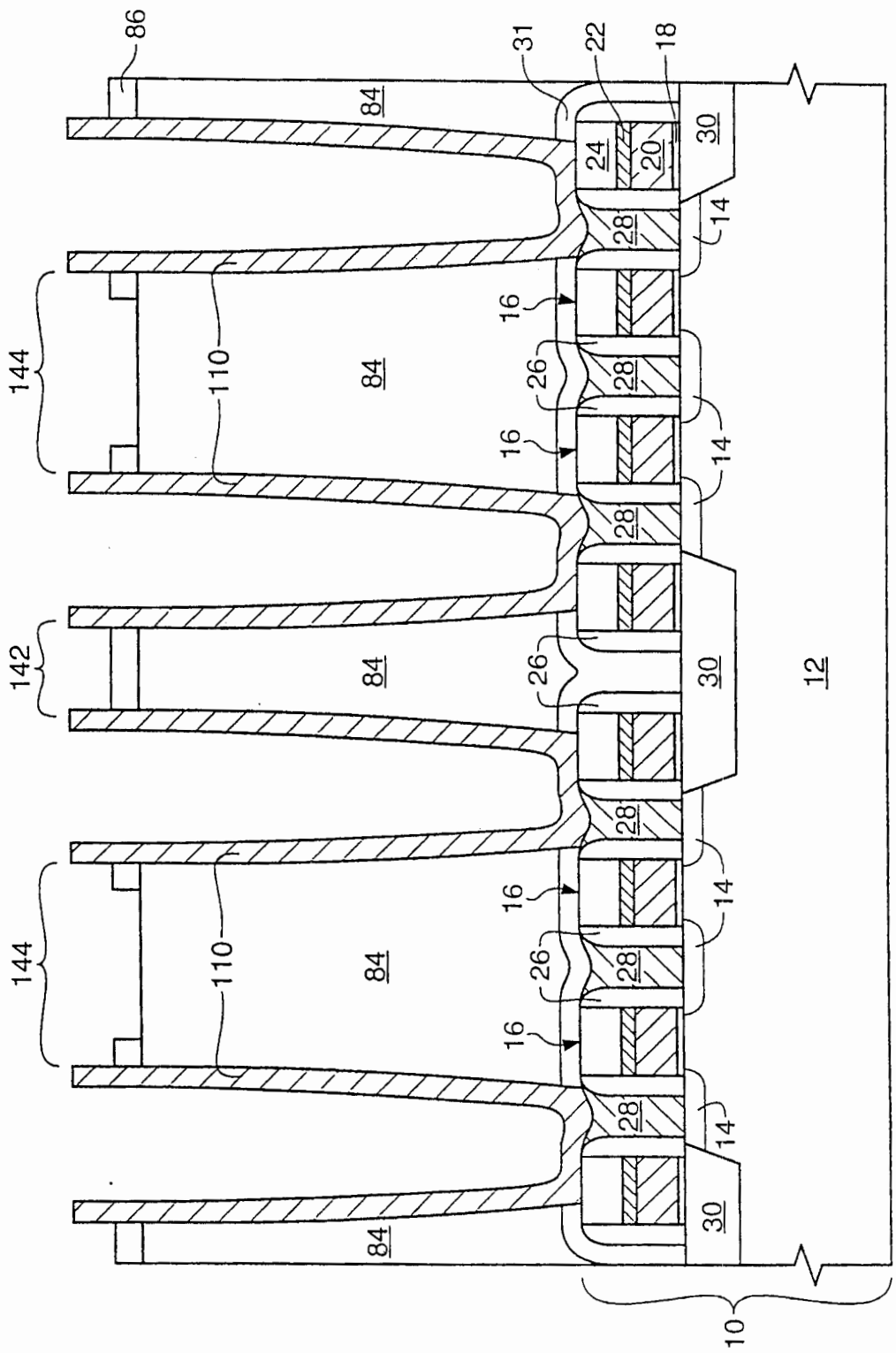


FIG. 18

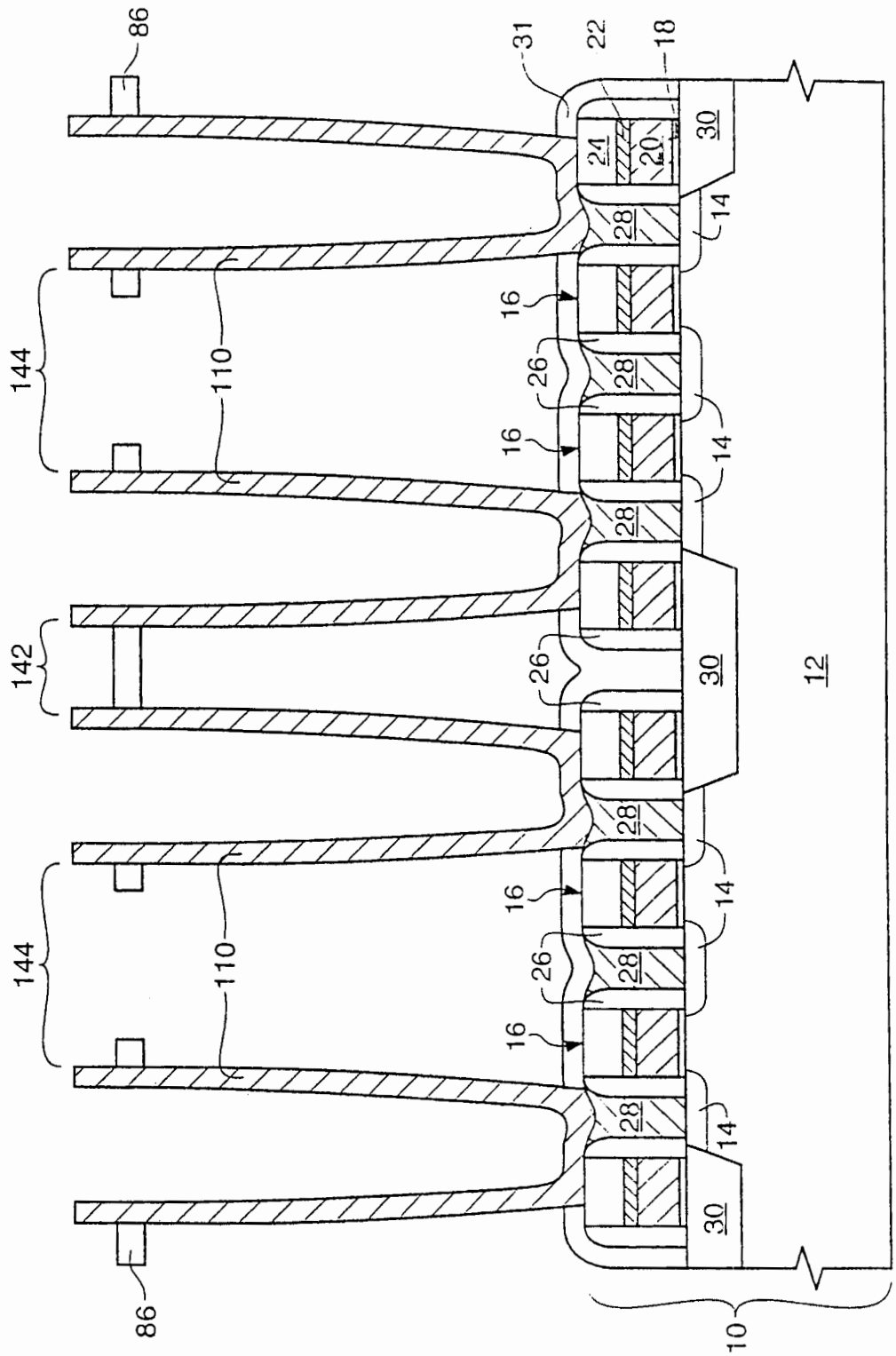


FIG. 19

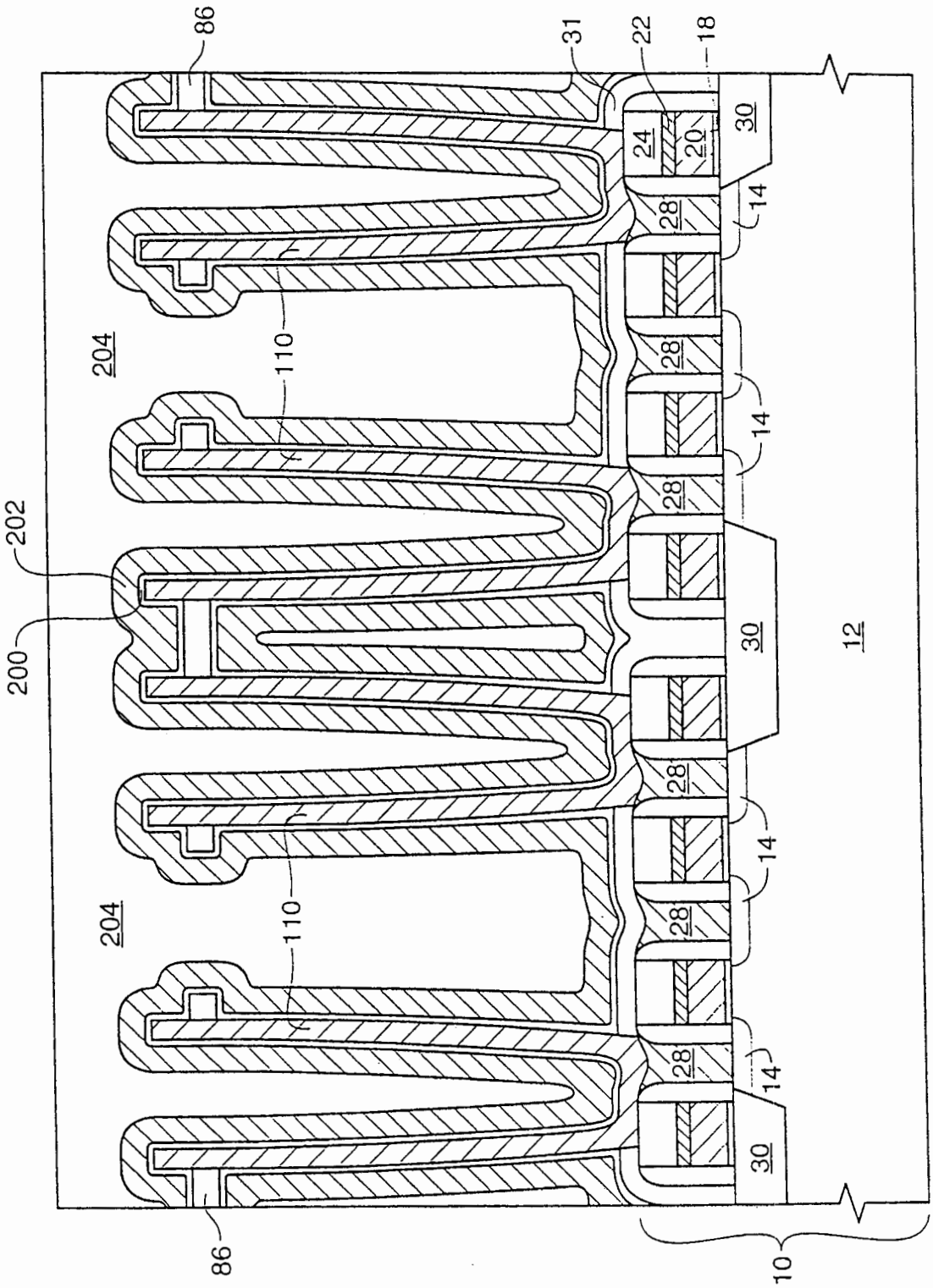


FIG. 20

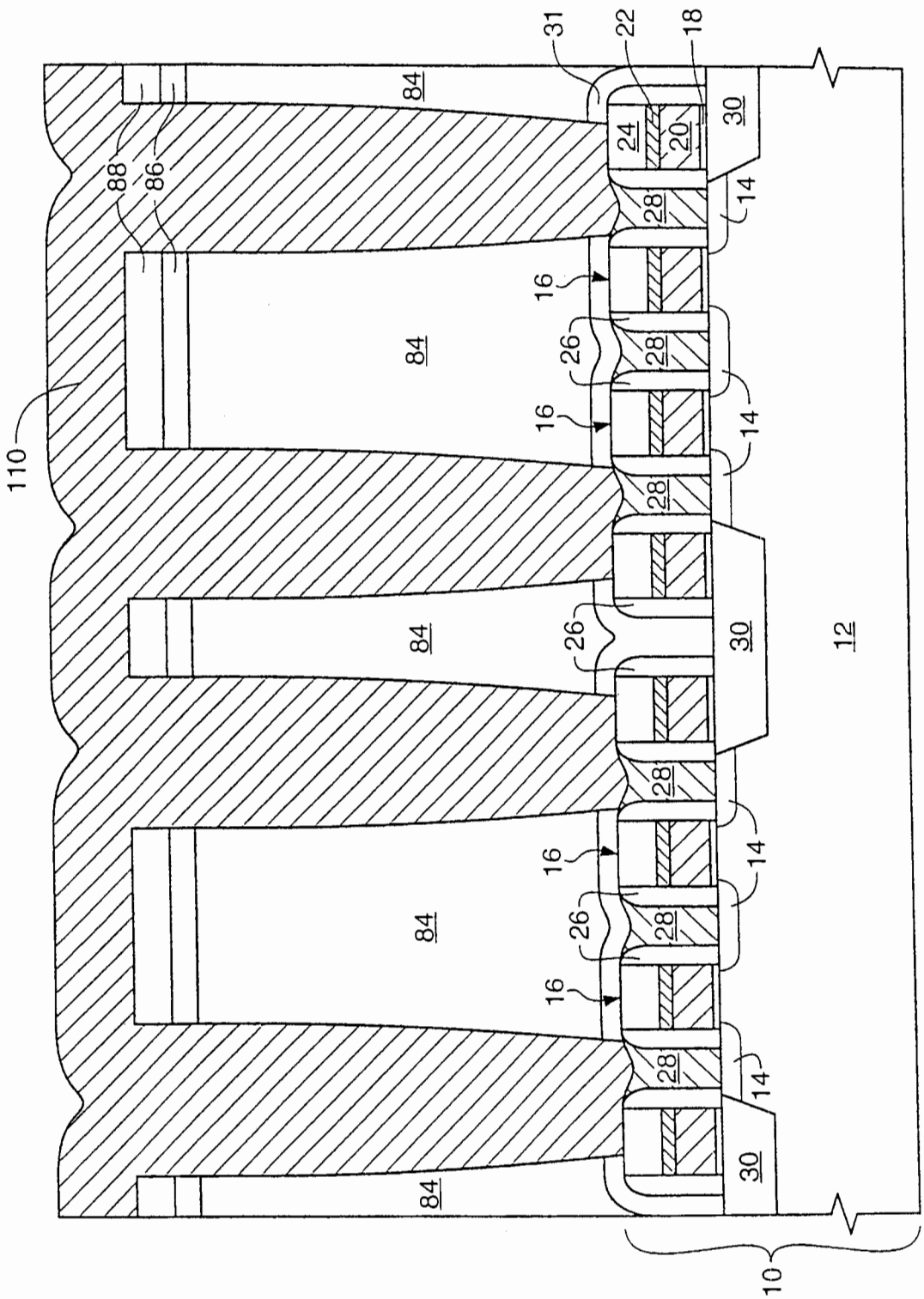


FIG. 21

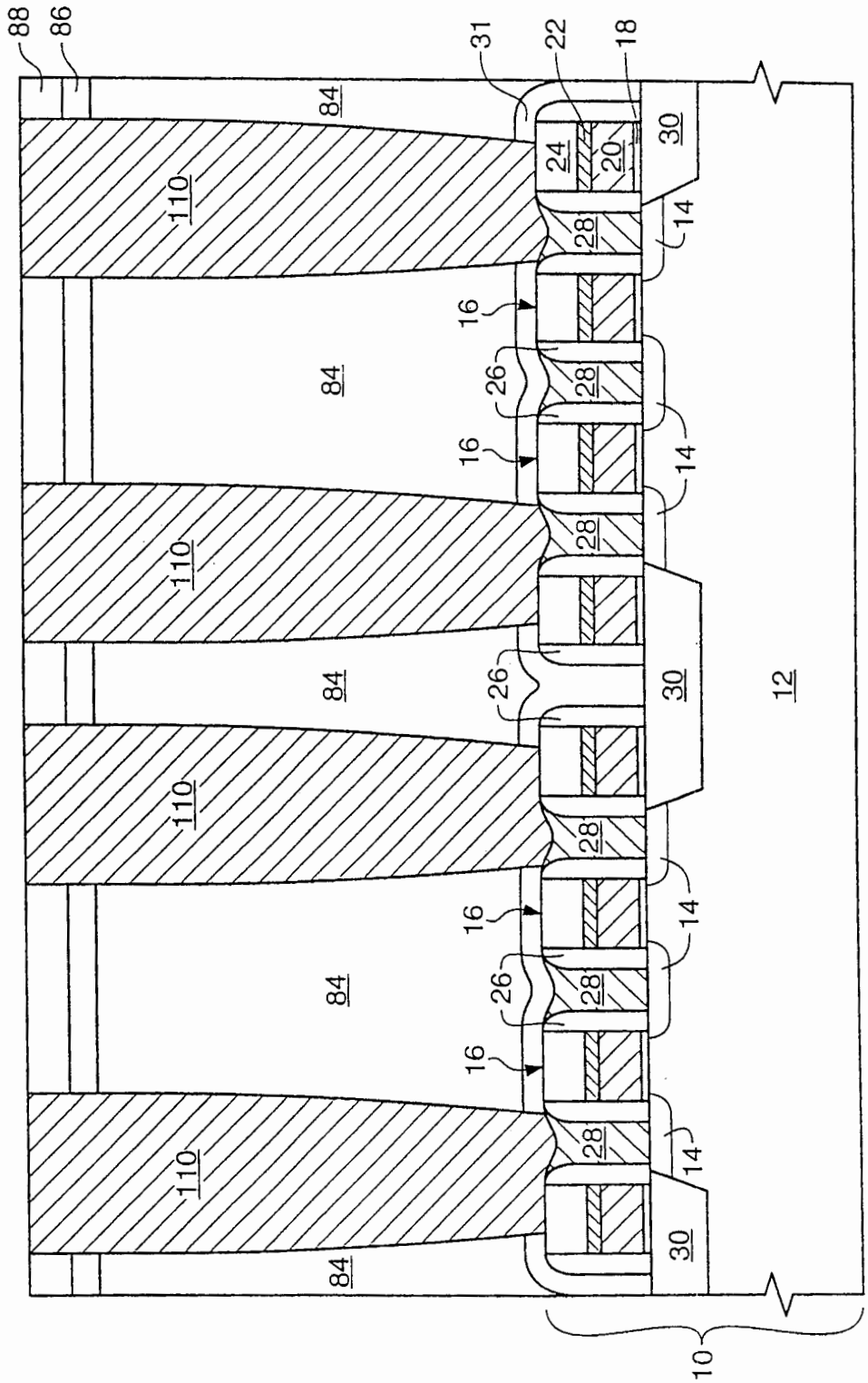


FIG. 22

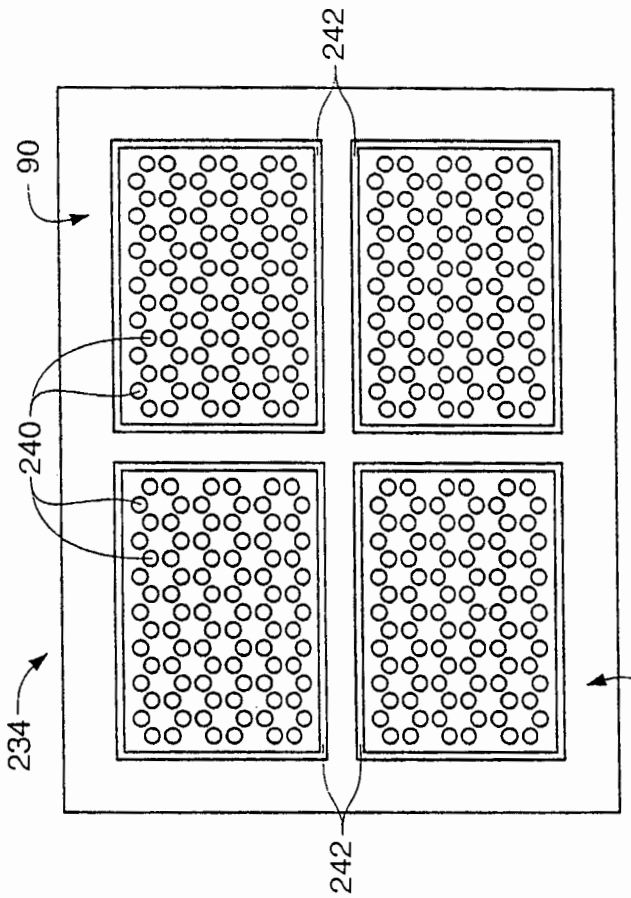


FIG. 24

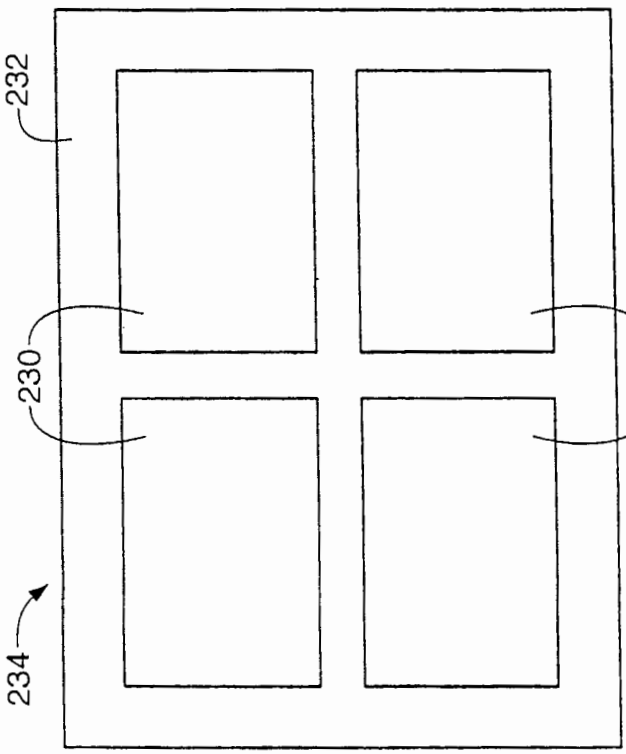


FIG. 23

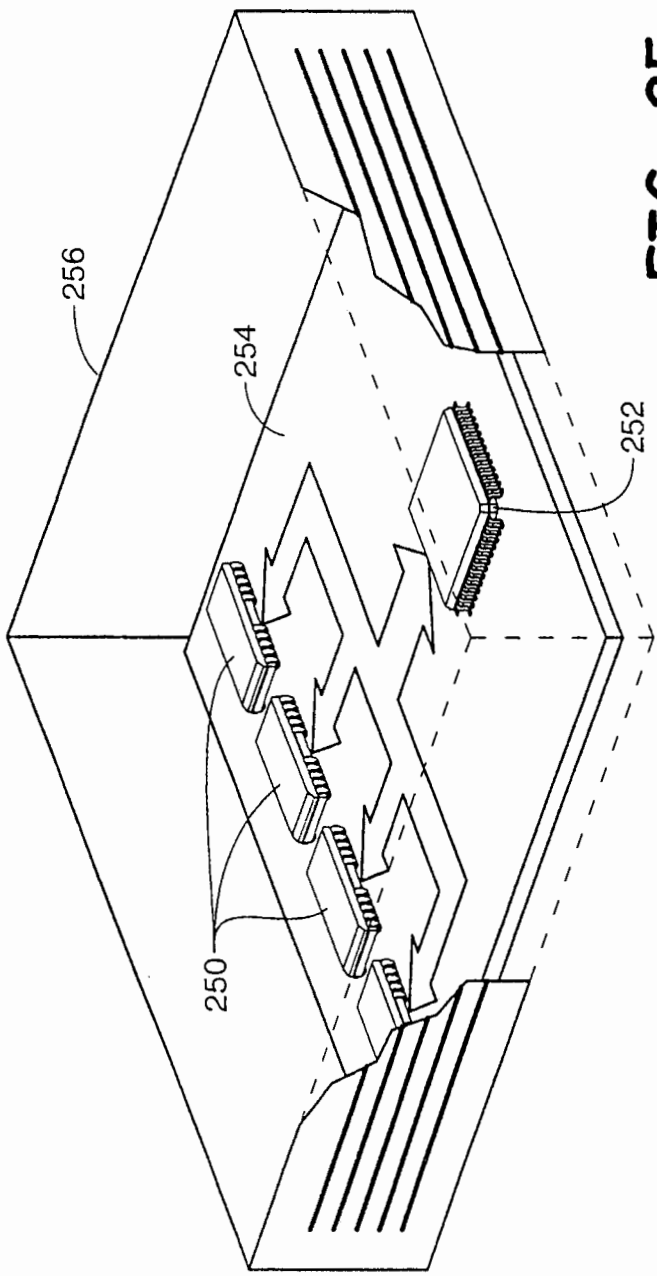


FIG. 25

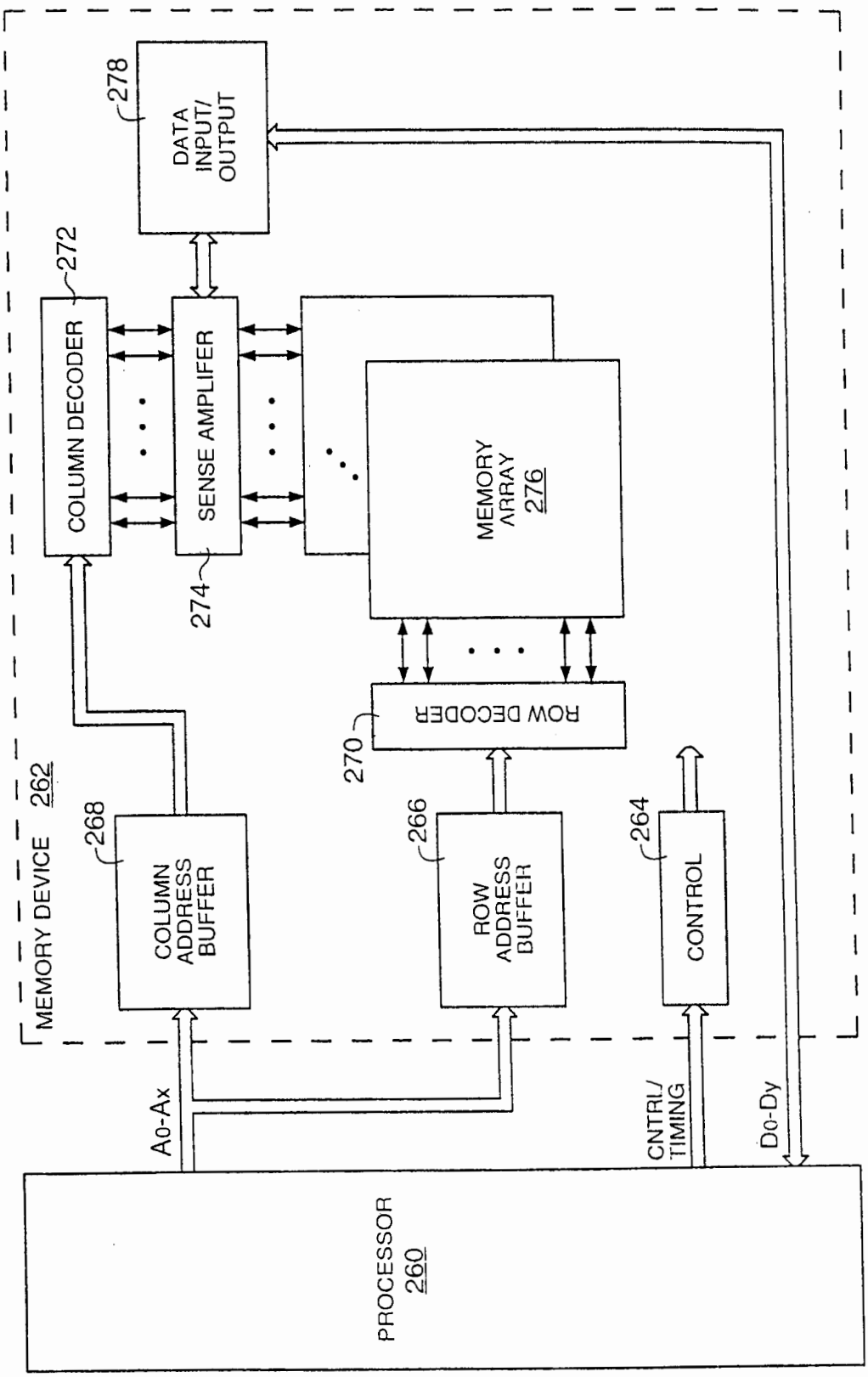

MEMORY DEVICE 262
DATA INPUT/ OUTPUT
278
COLUMN DECODER
272
SENSE AMPLIFER
274
MEMORY ARRAY 276
ROW DECODER
270
COLUMN ADDRESS BUFFER
268
ROW ADDRESS BUFFER
266
CONTROL
264
A0-Ax
CNTRL/ TIMING
D0-Dy
PROCESSOR 260

FIG. 26