What is claimed is:

1. A semiconductor device, comprising a semiconductor device active region, which is characterized in that the semiconductor device further comprises:

an electrode shape controlling layer disposed on the semiconductor device active region, the electrode shape controlling layer containing aluminum, the content of aluminum in all or part of the electrode shape controlling layer being reduced in a direction from bottom to up from the semiconductor device active region in a manner of linear reduction;

an electrode region disposed on the electrode shape controlling layer, the electrode region including a groove extended toward the semiconductor device active region and penetrating through the electrode shape controlling layer longitudinally, all or part of a side surface of the groove having a shape of a straight slope corresponding to the content of aluminum in the electrode shape controlling layer; and

an electrode disposed in the groove in the electrode region entirely or partially, the electrode having a shape matching with the shape of the groove, a bottom portion of the electrode being contacted with the semiconductor device active region.

2. The semiconductor device according to claim 1, characterized in that the electrode shape controlling layer is a semiconductor layer or a first dielectric layer.

3. The semiconductor device according to claim 1, characterized in that the electrode shape controlling layer is a combination of a semiconductor layer and a first dielectric layer, the first dielectric layer is located above the semiconductor layer, the content of aluminum at any position of the semiconductor layer is greater than that at any position of the first dielectric layer.

4. The semiconductor device according to claim 2 or claim 3, characterized in that the first dielectric layer is formed of one of SiN, SiAlN, SiAlGaN, SiAlOx, AlMgON and HfAlOx or a combination thereof.

5. The semiconductor device according to claim 2 or claim 3, characterized in that a semiconductor layer in the semiconductor device active region and the semiconductor layer in the electrode shape controlling layer are formed of one of Group III nitride, silicon, germanium, silicon germanium, III-IV compound and oxide or a combination thereof.

6. The semiconductor device according to claim 1, characterized in that the content of aluminum in all of the electrode shape controlling layer is reduced in the direction

from bottom to up from the semiconductor device active region in a manner of initial linear reduction and then remaining unchanged.

7. The semiconductor device according to claim 1, characterized in that the groove in the electrode shape controlling layer is extended into the semiconductor device active region.

8. The semiconductor device according to claim 1, characterized in that a second dielectric layer is deposited on all or part of inner walls of the groove in the electrode shape controlling layer and a surface of the electrode shape controlling layer, the electrode is located on the second dielectric layer entirely or partially.

9. The semiconductor device according to claim 8, characterized in that the second dielectric layer is formed of one of $Al_2O_3$, AlON, SiN, SiON, $SiO_2$, HfAlOx, $HfO_2$ or a combination thereof.

10. The semiconductor device according to claim 1, characterized in that the semiconductor device is a diode, the electrode is an anode electrode or a cathode electrode of the diode.

11. The semiconductor device according to claim 1, characterized in that the semiconductor device is a transistor, the electrode is one of a source electrode, a drain electrode and a gate electrode of the transistor.

12. The semiconductor device according to claim 1, characterized in that the semiconductor device active region comprises one of a high electron mobility transistor having an aluminum gallium nitride/gallium nitride heterojunction structure, a high electron mobility transistor having an aluminum gallium indium nitrogen/gallium nitride heterojunction structure, a high electron mobility transistor having a nitride aluminum/gallium nitride heterojunction structure, a gallium nitride MOSFET, a multi quantum well device having indium gallium nitride/gallium nitride, a light emitting diode made of p-type nitride, a UV-LED, a photodetector, a hydrogen generator, a solar cell, an LDMOS, a UMOSFET, a diode, a Schottky diode and an avalanche breakdown diode.

13. A method of manufacturing a semiconductor device, comprising:

S1. providing a semiconductor device active region;

which is characterized in that the method further comprises:

S2. forming an electrode shape controlling layer on the semiconductor device active region, the electrode shape controlling layer containing aluminum, the content of aluminum in all or part of the electrode shape controlling layer being reduced in a

direction from bottom to up from the semiconductor device active region in a manner of linear reduction;

S3. disposing an electrode region on the electrode shape controlling layer; forming a groove extended toward the semiconductor device active region and penetrating through the electrode shape controlling layer longitudinally in the electrode region, all or part of a side surface of the groove having a shape of a straight slope corresponding to the content of aluminum in the electrode shape controlling layer; and

S4. forming an electrode in the groove in the electrode region, the electrode being disposed in the groove in the electrode region entirely or partially, the electrode having a shape matching with the shape of the groove, a bottom portion of the electrode being contacted with the semiconductor device active region.

14. The method of manufacturing a semiconductor device according to claim 13, characterized in that steps S3 and S4 comprise:

S31. applying a first mask layer on the electrode shape controlling layer, and exposing the electrode region through photolithography;

S32. etching the electrode region so as to form the groove extended to the semiconductor device active region;

S33. removing the first mask layer;

S41. applying a second mask layer on the electrode shape controlling layer, exposing the electrode region through photolithography; and

S42. depositing the electrode, removing the second mask layer to form the electrode.

15. The method of manufacturing a semiconductor device according to claim 13, characterized in that in step S2, the electrode shape controlling layer is a semiconductor layer or a first dielectric layer.

16. The method of manufacturing a semiconductor device according to claim 13, characterized in that in step S2, the electrode shape controlling layer is a combination of a semiconductor layer and a first dielectric layer, the first dielectric layer is located above the semiconductor layer, the content of aluminum at any position of the semiconductor layer is greater than that at any position of the first dielectric layer.

17. The method of manufacturing a semiconductor device according to claim 15 or claim 16, characterized in that the first dielectric layer is formed of one of SiN, SiAlN, SiAlGaN, SiAlOx, AlMgON and HfAlOx or a combination thereof.

18. The method of manufacturing a semiconductor device according to claim 15 or

claim 16, characterized in that the first dielectric layer is grown with one of MOCVD, PECVD, LPCVD, MBE, CVD and GCIB.

19. The method of manufacturing a semiconductor device according to claim 13, characterized in that before step S4, the method further comprises:

depositing a second dielectric layer on all or part of inner walls of the groove in the electrode shape controlling layer and a surface of the electrode shape controlling layer.

20. The method of manufacturing a semiconductor device according to claim 19, characterized in that the second dielectric layer is formed of one of $Al_2O_3$, AlON, SiN, SiON, $SiO_2$, HfAlOx, $HfO_2$ or a combination thereof.

21. The method of manufacturing a semiconductor device according to claim 13, characterized in that the content of aluminum in all of the electrode shape controlling layer is reduced in the direction from bottom to up from the semiconductor device active region in a manner of initial linear reduction and then remaining unchanged.

22. The method of manufacturing a semiconductor device according to claim 13, characterized in that the groove in the electrode shape controlling layer is extended into the semiconductor device active region.

23. A semiconductor device, comprising a semiconductor device active region, which is characterized in that the semiconductor device further comprises:

an electrode shape controlling layer disposed on the semiconductor device active region, the electrode shape controlling layer containing aluminum, the content of aluminum in all or part of the electrode shape controlling layer being reduced in a direction from bottom to up from the semiconductor device active region in a manner of decelerating reduction;

an electrode region disposed on the electrode shape controlling layer, the electrode region including a groove extended toward the semiconductor device active region and penetrating through the electrode shape controlling layer longitudinally, all or part of a side surface of the groove having a shape of a concave slope protruded away from a central line of the groove, the shape corresponding to the content of aluminum in the electrode shape controlling layer; and

an electrode disposed in the groove in the electrode region entirely or partially, the electrode having a shape matching with the shape of the groove, a bottom portion of the electrode being contacted with the semiconductor device active region.

24. The semiconductor device according to claim 23, characterized in that the

electrode shape controlling layer is a semiconductor layer or a first dielectric layer.

25. The semiconductor device according to claim 23, characterized in that the electrode shape controlling layer is a combination of a semiconductor layer and a first dielectric layer, the first dielectric layer is located above the semiconductor layer, the content of aluminum at any position of the semiconductor layer is greater than that at any position of the first dielectric layer.

26. The semiconductor device according to claim 24 or claim 25, characterized in that the first dielectric layer is formed of one of SiN, SiAlN, SiAlGaN, SiAlOx, AlMgON and HfAlOx or a combination thereof.

27. The semiconductor device according to claim 24 or claim 25, characterized in that a semiconductor layer in the semiconductor device active region and the semiconductor layer in the electrode shape controlling layer are formed of one of Group III nitride, silicon, germanium, silicon germanium, III-IV compound and oxide or a combination thereof.

28. The semiconductor device according to claim 23, characterized in that the content of aluminum in all of the electrode shape controlling layer is reduced in the direction from bottom to up from the semiconductor device active region in a manner of initial decelerating reduction and then remaining unchanged.

29. The semiconductor device according to claim 23, characterized in that the groove in the electrode shape controlling layer is extended into the semiconductor device active region.

30. The semiconductor device according to claim 23, characterized in that a second dielectric layer is deposited on all or part of inner walls of the groove in the electrode shape controlling layer and a surface of the electrode shape controlling layer, the electrode is located on the second dielectric layer entirely or partially.

31. The semiconductor device according to claim 30, characterized in that the second dielectric layer is formed of one of $Al_2O_3$, AlON, SiN, SiON, $SiO_2$, HfAlOx, $HfO_2$ or a combination thereof.

32. The semiconductor device according to claim 23, characterized in that the semiconductor device is a diode, the electrode is an anode electrode or a cathode electrode of the diode.

33. The semiconductor device according to claim 23, characterized in that the semiconductor device is a transistor, the electrode is one of a source electrode, a drain

electrode and a gate electrode of the transistor.

34. The semiconductor device according to claim 23, characterized in that the semiconductor device active region comprises one of a high electron mobility transistor having an aluminum gallium nitride/gallium nitride heterojunction structure, a high electron mobility transistor having an aluminum gallium indium nitrogen/gallium nitride heterojunction structure, a high electron mobility transistor having a nitride aluminum/gallium nitride heterojunction structure, a gallium nitride MOSFET, a multi quantum well device having indium gallium nitride/gallium nitride, a light emitting diode made of p-type nitride, a UV-LED, a photodetector, a hydrogen generator, a solar cell, an LDMOS, a UMOSFET, a diode, a Schottky diode and an avalanche breakdown diode.

35. A method of manufacturing a semiconductor device, comprising:

S1. providing a semiconductor device active region;

which is characterized in that the method further comprises:

S2. forming an electrode shape controlling layer on the semiconductor device active region, the electrode shape controlling layer containing aluminum, the content of aluminum in all or part of the electrode shape controlling layer being reduced in a direction from bottom to up from the semiconductor device active region in a manner of decelerating reduction;

S3. disposing an electrode region on the electrode shape controlling layer; forming a groove extended toward the semiconductor device active region and penetrating through the electrode shape controlling layer longitudinally in the electrode region, all or part of a side surface of the groove having a shape of a concave slope protruded away from a central line of the groove, the shape corresponding to the content of aluminum in the electrode shape controlling layer; and

S4. forming an electrode in the groove in the electrode region, the electrode being disposed in the groove in the electrode region entirely or partially, the electrode having a shape matching with the shape of the groove, a bottom portion of the electrode being contacted with the semiconductor device active region.

36. The method of manufacturing a semiconductor device according to claim 35, characterized in that steps S3 and S4 comprise:

S31. applying a first mask layer on the electrode shape controlling layer, and exposing the electrode region through photolithography;

S32. etching the electrode region so as to form the groove extended to the

semiconductor device active region;

S33. removing the first mask layer;

S41. applying a second mask layer on the electrode shape controlling layer, exposing the electrode region through photolithography; and

S42. depositing the electrode, removing the second mask layer to form the electrode.

37. The method of manufacturing a semiconductor device according to claim 35, characterized in that in step S2, the electrode shape controlling layer is a semiconductor layer or a first dielectric layer.

38. The method of manufacturing a semiconductor device according to claim 35, characterized in that in step S2, the electrode shape controlling layer is a combination of a semiconductor layer and a first dielectric layer, the first dielectric layer is located above the semiconductor layer, the content of aluminum at any position of the semiconductor layer is greater than that at any position of the first dielectric layer.

39. The method of manufacturing a semiconductor device according to claim 37 or claim 38, characterized in that the first dielectric layer is formed of one of SiN, SiAlN, SiAlGaN, SiAlOx, AlMgON and HfAlOx or a combination thereof.

40. The method of manufacturing a semiconductor device according to claim 37 or claim 38, characterized in that the first dielectric layer is grown with one of MOCVD, PECVD, LPCVD, MBE, CVD and GCIB.

41. The method of manufacturing a semiconductor device according to claim 35, characterized in that before step S4, the method further comprises:

depositing a second dielectric layer on all or part of inner walls of the groove in the electrode shape controlling layer and a surface of the electrode shape controlling layer.

42. The method of manufacturing a semiconductor device according to claim 41, characterized in that the second dielectric layer is formed of one of $Al_2O_3$, AlON, SiN, SiON, $SiO_2$, HfAlOx, $HfO_2$ or a combination thereof.

43. The method of manufacturing a semiconductor device according to claim 35, characterized in that the content of aluminum in all of the electrode shape controlling layer is reduced in the direction from bottom to up from the semiconductor device active region in a manner of initial decelerating reduction and then remaining unchanged.

44. The method of manufacturing a semiconductor device according to claim 35, characterized in that the groove in the electrode shape controlling layer is extended into the semiconductor device active region.

45. A semiconductor device, comprising a semiconductor device active region, which is characterized in that the semiconductor device further comprises:

an electrode shape controlling layer disposed on the semiconductor device active region, the electrode shape controlling layer containing aluminum, the content of aluminum in all or part of the electrode shape controlling layer being reduced in a direction from bottom to up from the semiconductor device active region in a manner of accelerating reduction;

an electrode region disposed on the electrode shape controlling layer, the electrode region including a groove extended toward the semiconductor device active region and penetrating through the electrode shape controlling layer longitudinally, all or part of a side surface of the groove having a shape of a convex slope protruded toward the central line of the groove, the shape corresponding to the content of aluminum in the electrode shape controlling layer; and

an electrode disposed in the groove in the electrode region entirely or partially, the electrode having a shape matching with the shape of the groove, a bottom portion of the electrode being contacted with the semiconductor device active region.

46. The semiconductor device according to claim 45, characterized in that the electrode shape controlling layer is a semiconductor layer or a first dielectric layer.

47. The semiconductor device according to claim 45, characterized in that the electrode shape controlling layer is a combination of a semiconductor layer and a first dielectric layer, the first dielectric layer is located above the semiconductor layer, the content of aluminum at any position of the semiconductor layer is greater than that at any position of the first dielectric layer.

48. The semiconductor device according to claim 46 or claim 47, characterized in that the first dielectric layer is formed of one of SiN, SiAlN, SiAlGaN, SiAlOx, AlMgON and HfAlOx or a combination thereof.

49. The semiconductor device according to claim 46 or claim 47, characterized in that a semiconductor layer in the semiconductor device active region and the semiconductor layer in the electrode shape controlling layer are formed of one of Group III nitride, silicon, germanium, silicon germanium, III-IV compound and oxide or a combination thereof.

50. The semiconductor device according to claim 45, characterized in that the content of aluminum in all of the electrode shape controlling layer is reduced in the

direction from bottom to up from the semiconductor device active region in a manner of initial accelerating reduction and then remaining unchanged.

51. The semiconductor device according to claim 45, characterized in that the groove in the electrode shape controlling layer is extended into the semiconductor device active region.

52. The semiconductor device according to claim 45, characterized in that a second dielectric layer is deposited on all or part of inner walls of the groove in the electrode shape controlling layer and a surface of the electrode shape controlling layer, the electrode is located on the second dielectric layer entirely or partially.

53. The semiconductor device according to claim 52, characterized in that the second dielectric layer is formed of one of $Al_2O_3$, AlON, SiN, SiON, $SiO_2$, HfAlOx, $HfO_2$ or a combination thereof.

54. The semiconductor device according to claim 45, characterized in that the semiconductor device is a diode, the electrode is an anode electrode or a cathode electrode of the diode.

55. The semiconductor device according to claim 45, characterized in that the semiconductor device is a transistor, the electrode is one of a source electrode, a drain electrode and a gate electrode of the transistor.

56. The semiconductor device according to claim 45, characterized in that the semiconductor device active region comprises one of a high electron mobility transistor having an aluminum gallium nitride/gallium nitride heterojunction structure, a high electron mobility transistor having an aluminum gallium indium nitrogen/gallium nitride heterojunction structure, a high electron mobility transistor having a nitride aluminum/gallium nitride heterojunction structure, a gallium nitride MOSFET, a multi quantum well device having indium gallium nitride/gallium nitride, a light emitting diode made of p-type nitride, a UV-LED, a photodetector, a hydrogen generator, a solar cell, an LDMOS, a UMOSFET, a diode, a Schottky diode and an avalanche breakdown diode.

57. A method of manufacturing a semiconductor device, comprising:

S1. providing a semiconductor device active region;

which is characterized in that the method further comprises:

S2. forming an electrode shape controlling layer on the semiconductor device active region, the electrode shape controlling layer containing aluminum, the content of aluminum in all or part of the electrode shape controlling layer being reduced in a

direction from bottom to up from the semiconductor device active region in a manner of accelerating reduction;

S3. disposing an electrode region on the electrode shape controlling layer; forming a groove extended toward the semiconductor device active region and penetrating through the electrode shape controlling layer longitudinally in the electrode region, all or part of a side surface of the groove having a shape of a convex slope protruded toward the central line of the groove, the shape corresponding to the content of aluminum in the electrode shape controlling layer; and

S4. forming an electrode in the groove in the electrode region, the electrode being disposed in the groove in the electrode region entirely or partially, the electrode having a shape matching with the shape of the groove, a bottom portion of the electrode being contacted with the semiconductor device active region.

58. The method of manufacturing a semiconductor device according to claim 57, characterized in that steps S3 and S4 comprise:

S31. applying a first mask layer on the electrode shape controlling layer, and exposing the electrode region through photolithography;

S32. etching the electrode region so as to form the groove extended to the semiconductor device active region;

S33. removing the first mask layer;

S41. applying a second mask layer on the electrode shape controlling layer, exposing the electrode region through photolithography; and

S42. depositing the electrode, removing the second mask layer to form the electrode.

59. The method of manufacturing a semiconductor device according to claim 57, characterized in that in step S2, the electrode shape controlling layer is a semiconductor layer or a first dielectric layer.

60. The method of manufacturing a semiconductor device according to claim 57, characterized in that in step S2, the electrode shape controlling layer is a combination of a semiconductor layer and a first dielectric layer, the first dielectric layer is located above the semiconductor layer, the content of aluminum at any position of the semiconductor layer is greater than that at any position of the first dielectric layer.

61. The method of manufacturing a semiconductor device according to claim 59 or claim 60, characterized in that the first dielectric layer is formed of one of SiN, SiAlN, SiAlGaN, SiAlOx, AlMgON and HfAlOx or a combination thereof.

62. The method of manufacturing a semiconductor device according to claim 59 or claim 60, characterized in that the first dielectric layer is grown with one of MOCVD, PECVD, LPCVD, MBE, CVD and GCIB.

63. The method of manufacturing a semiconductor device according to claim 57, characterized in that before step S4, the method further comprises:

depositing a second dielectric layer on all or part of inner walls of the groove in the electrode shape controlling layer and a surface of the electrode shape controlling layer.

64. The method of manufacturing a semiconductor device according to claim 63, characterized in that the second dielectric layer is formed of one of $Al_2O_3$, AlON, SiN, SiON, $SiO_2$, HfAlOx, $HfO_2$ or a combination thereof.

65. The method of manufacturing a semiconductor device according to claim 57, characterized in that the content of aluminum in all of the electrode shape controlling layer is reduced in the direction from bottom to up from the semiconductor device active region in a manner of initial accelerating reduction and then remaining unchanged.

66. The method of manufacturing a semiconductor device according to claim 57, characterized in that the groove in the electrode shape controlling layer is extended into the semiconductor device active region.