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P.; 13305 Tichester Court, Austin, TX 78729 (US).
OVERKAMP, Gregory, A.; P.O. Box 163442, Austin,
TX 78716 (US).

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(74) Agent: **HARRIS, Scott, C.**; Fish & Richardson PC, 4350
La Jolla Village Drive, Suite 500, San Diego, CA 92122
(US).

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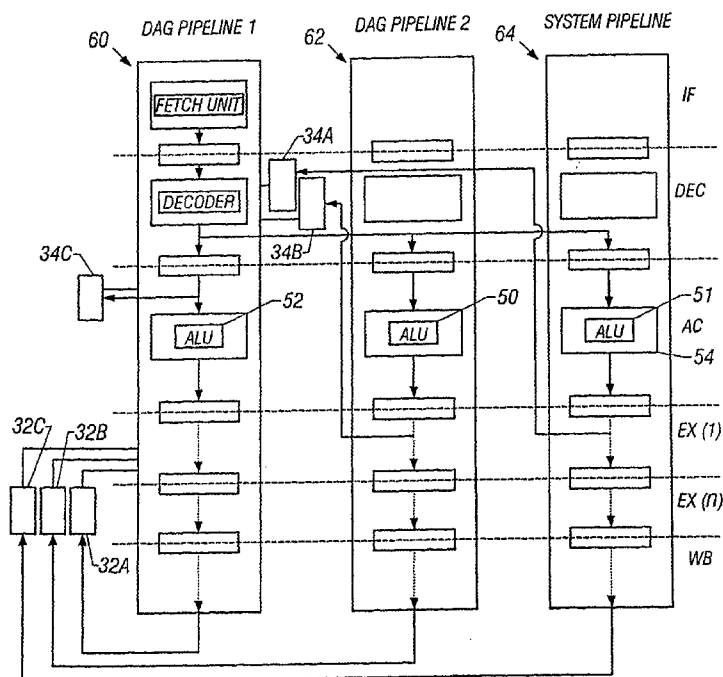
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(71) Applicants: **INTEL CORPORATION** [US/US]; 2200
Mission College Boulevard, Santa Clara, CA 95052 (US).
ANALOG DEVICES, INC. [US/US]; One Technology
Way, P.O. Box 9106, Norwood, MA 02062-9106 (US).

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(72) Inventors: **INOUE, Ryo**; 10521 Redmond Road, Austin,
TX 78739 (US). **SINGH, Ravi, P.**; 12349 Metric Boule-
vard, #829, Austin, TX 78758 (US). **ROTH, Charles**,

(54) Title: METHOD AND APPARATUS FOR PROCESSING PROGRAM LOOPS IN PARALLEL



(57) Abstract: In one embodiment, a programmable processor is adapted to support hardware loops. The processor may include hardware such as a first set of registers, a second set registers, a first pipeline, and a second pipeline. Furthermore, the processor may include a control unit adapted to efficiently implement the hardware when performing a hardware loop.



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