(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
4 September 2003 (04.09.2003)

PCT

(10) International Publication Number
WO 03/073356 A1

(51) International Patent Classification[7]: G06F 19/00

(21) International Application Number: PCT/US03/05845

(22) International Filing Date: 24 February 2003 (24.02.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

60/360,036	26 February 2002 (26.02.2002)	US
10/371,736	20 February 2003 (20.02.2003)	US

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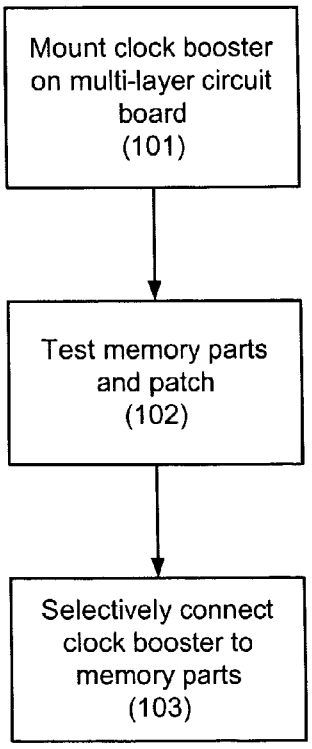
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(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE,

[Continued on next page]

(54) Title: METHOD AND APPARATUS FOR IMPLEMENTING A SELECTIVELY OPERABLE CLOCK BOOSTER FOR DDR



(57) Abstract: A method of fabricating a memory module according to one embodiment, a clock booster is mounted on a multi-layer circuit bard (101). The clock booster may be any apparatus that receives a clock input, and output one or more clock signals capable of driving a multiplicity of logic parts without clock distortion. In a preferred embodiment, a phase-locked loop circuit may be used as a clock booster. The test and patching (102) allows a fully-functional memory part adds, it is desirable to only connect the clock signal to those memory parts that are utilized. This may be accomplished using any number of switching mechanisms to connect or disconnect a clock signal to a memory part. In a preferred embodiment, a clock patching network may be used to selectively connect or disconnect outputs of a clock booster to the memory parts (103).

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ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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